A CMOS Active Pixel Image Sensor 
with In-pixel CDS for High-Speed Cameras 

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ABSTRACT 

This paper presents a high-speed CMOS image sensor whose frame rate exceeds 2000 frames/s. The pixel includes a photodiode, a charge-transfer amplifier, and circuitry for correlated double sampling (CDS) and global electronic shuttering. Reset noise, which is a major random noise factor, is reduced by the CDS combined with the charge-transfer amplifier. The total number of devices in the pixel is 11 transistors and 2 MOS capacitors. Test circuits were fabricated using a 0.25\(\mu\)m CMOS process. The sensitivity of the 20 \(\times\) 20\(\mu\)m\(^2\) pixel using the floating diffusion capacitor of 6.2fF and the photodiode area of 15 \(\times\) 12.7\(\mu\)m\(^2\) is 34V/\text{lux-sec}. At 1000 frames/sec, noise level is 2.43mV rms (dark). The noise level and the sensitivity are greatly improved compared with a 3Tr. type APS implemented with the same technology and a previous version of the APS with in-pixel CDS. 

Keywords: High-speed image sensors, CMOS image sensors, active pixel sensors, CDS, noise.

1. INTRODUCTION 

Application of high-speed videography extends over various discipline fields such as optical measurement including fluorescence analysis where density measurement has great importance, motion analysis including capture of fast-moving subjects and signal processing for real time tracking. Cameras for these application markets generally require output of still image with low noise, high grayscale and high sensitivity.

Currently, CCD and CMOS are the main technologies available for image sensor devices for high-speed recording [1]-[5]. In view of the higher fill factor, high-speed readout, availability of on-chip ADC, capability to incorporate various processing functions, possibility for higher resolution, smaller chip size and lower cost, the CMOS technology is believed to have an advantage over the CCD.

In the photoelectric conversion cell of CMOS image sensor, a 3-transistor pixel circuitry is generally favored. However, the greatest challenge in the high-speed image sensor is the high reset noise level due to the larger photocell area and the difficulty of reducing random noise by the global shutter.

This paper discusses the result of an experimental CMOS image sensor ñ design and evaluation - for high-speed recording with electronic shutter and correlated double sampling (CDS) function incorporated in the pixel area for reducing random noise and fixed pattern noise. In addition, this paper describes the comparison made between this sensor and conventional 3-transistor pixel circuitry.

2. IMAGE SENSOR DEVICE AND CIRCUITS 

Fig. 1 shows an example of structure of a high-speed image sensor. The whole sensor is roughly divided into three major parts of the pixel array, the vertical scanner to drive the sensor, and the readout circuit to amplify image signals, to remove noise and to obtain digital data. This paper targets an image sensor with 2000 frames per second (fps) and image resolution of 512 \(\times\) 512 pixels. It was also a target that this sensor is to be fabricated in standard CMOS manufacturing process. This paper focuses on the pixel circuitry and its evaluation.

Fig. 2 shows the block diagram of the pixel circuitry used in the evaluation.

Fig. 3 shows the principle of operation of the sensor unit. We used a charge-transfer amplifier pixel consisting of four transistors. In-pixel charge transfer amplifiers are usually used for active pixel sensors (APS) with a buried photodiode [6][7][8], and a photogate [9]. It is very effective for low-noise high-sensitivity image sensors if the perfect charge...
transfer can be achieved. In the pixel circuit shown in Fig. 2, however, special considerations are necessary to reduce the image lag, and non-linearity [10].

The operation of this circuit is: a) light falls on the pixels, b) Photo electrons, accumulated in the floating diffusion (FD), are cleared, during which time, the reset voltage is retained in S/H within the pixel. c) The photoelectron charge transmitted from photodiode to the floating diffusion. d) Transfer gate Tx is closed and the voltage in the floating diffusion is sampled at S/H. e) The photodiode are reset to the photodiode reset voltage, otherwise they cause image lag when the electron charge is transferred through the pixel via the transfer gate Tx. f) The excessive reset charge is drained, while keeping the transfer gate TX at a predetermined level, to determine the reset level of the photodiode.

By simultaneously effecting all these activities during every framing time over the entire array of pixels, the function of global shuttering is attained.

In addition to the above, S/H and CDS circuits are added to the S/H and CDS units, respectively, in the rear stage.

2.1. Evaluation Circuit

Fig. 4 shows the high-speed image sensor pixel circuitry proposed in this paper. The circuit consists of one photodiode, eleven transistors, two capacitors for S/H and two column output buffers.

Fig. 5 shows the control signals used in the above circuit. Sampling of signals takes place at C_{SISH} capacitors by checking the signal voltage after the reset voltage of the floating diffusion, accumulated in the C_{SCHR} capacitor, is transferred. Reading of pixel information is carried out by selecting one pixel line each at a time with the SW_{SEL} switch.

The CDS function is activated by short-circuiting the SW_{SHR} switch of the differential buffer input at the time of the pixel signal readout. Actually, CDS performs its function by detecting the difference between the signal and reset voltages on the fixed pattern noise (caused by variation of the reset transistor R) and the reset noise in the voltage detection node.
As discussed in the above, electronic shuttering with uniform exposure has been made possible by effecting in-pixel charge transfer and in-pixel S/H simultaneously over the entire array of pixels. Moreover, CDS including pixels and readout amplifier has been made possible.

This circuit was made using 0.25 μm CMOS process. The designed parameters were 100 fF of photodiode capacitance and 6.2 fF of floating diffusion capacitance. The calculated conversion gain is 25.8 μV/e-. The capacitance of the two S/H circuits is 40 fF.

![Fig. 3 Operation of the charge transfer amplifier part](image)

![Fig. 4 Equivalent schematic of Type1 pixel](image)

![Fig. 5 Timing chart of Type1 pixel circuit](image)
2.2. Circuitry for Comparison

Fig. 6 shows the circuit of our designed image sensor (Type 2) made for comparison purposes. The comparison circuit consists of one photodiode, eight transistors, one CDS, one S/H capacitor and one column output buffer. The signal flows from the sensor unit sending out the reset and signal voltages to the serially connected CDS and S/H in sequence.

Fig. 7 shows the control signal of the comparison circuit. CDS is carried out with sufficient C_{CDS} capacitance by finding the difference between the signal and reset voltages on the fixed pattern noise caused by variation of transistor R and the reset noise at the voltage detection node. As shown here, electronic shuttering has been made possible by effecting in-pixel charge transfer and in-pixel S/H simultaneously over the entire array of pixels.

This circuit makes possible to form a pixel with eight transistors, but, the drawback of it is that the output signal amplitude is determined by the capacitance ratio between C_{CDS} and C_{S/H}, which is expressed by the following equation:

$$V_2 = V_1 \left( \frac{C_{CDS}}{C_{CDS} + C_{S/H}} \right)$$  \hspace{1cm} (1)

where \(V_1\) and \(V_2\) are voltage swing at the nodes shown in Fig. 6. Moreover, considering the \(kT/C\) noise in the S/H capacitance and SW_{S/H}, the \(C_{CDS}\) capacitance must be increased, which will inevitably reduce the aperture ratio of the photodiode.

This circuit was made using the 0.6 \(\mu\)m CMOS process. The design parameters are 40 fF for the photodiode capacitance and 10fF for the floating diffusion capacitance. As a result, the conversion gain is calculated 16 \(\mu\)V/e\(^{-}\). The S/H and C_{CDS} capacitance were set 20 fF and 60 fF, respectively.

3. EXPERIMENTAL RESULTS

The data obtained through test of the proposed image sensor is shown in Table 1. For comparison purposes, corresponding data for a 3-Tr pixel circuitry with rolling shutter is added.

The pixel pitch is 20 x 20 \(\mu\)m through all circuits. The aperture ratio of the photodiode for Type 1, Type 2 and 3-Tr is 48\%, 30\% and 56\% respectively. The sensor type is line, area and line, and the amplification at readout amplifier is x 1, x 4 and x1, for Type1, Type2 and 3Tr respectively. The amplification of Type 2 was made larger than the others in view of the division of the signal amplitude by CDS.
Fig. 8 shows an image shot with 1 msec exposure. Type 1, because it is a line sensor, scans the subject to form a picture of Fig. 8(a). No considerable random noise is seen in either of the photos. The photo clearly shows that the experimental image sensor performs without problem. Fig. 8(b) is taken with the Type2 image sensor of 256 x 256 array.

Fig. 9 shows the input/output characteristic of the Type 1 and Type 2 sensors. The x-axis is the amount of light fallen on the sensor surface, the y-axis the output voltage from the sensor. In this measurement, a halogen light source was used and the sensors were added with a IR filter on them.

Table 2 shows the summary of the sensitivity and noise. Type 1 sensor has a sensitivity of 34.5 V/lux-sec, the highest of all and 3 times that of Type 2 and 8 times of 3-Tr. As to random noise, Type 2 showed the highest value of 2.52 Vrms, 4 percent higher than Type 1 and as much as 6.6 times that of the 3-Tr sensor. To standardize the random noise of Type 2 and 3-Tr sensors with the sensitivity of Type 1 as the base, the noise level of Type 2 is now 3.2 times that of Type 1 and 1.2 times with the 3-Tr sensor.

Although the above standardized noise level contains the noise factor of the readout amplifier, it can be safely said the noise level of Type 1 sensor is considerably lower than Type 2.

Now, we make a theoretical estimation on the sensitivity and noise level of 3-Tr sensor modifies to a high-speed pixel circuit as shown in Fig. 10, with its aperture ratio standardized based on the ratio of Type 1. The S/H and CDS circuits remain the same as those for Type 1.

The output sensitivity, because of the lowered aperture ratio, is increased to 1.17 times, which is decreased to 0.94 times by the added source follower resulting in a 4.0V/lux-sec output. The noise voltage of the 3-Tr output, as it was measured, should increase to 1.171/2 times because the conversion gain decreases and the photodiode gets smaller. This noise is denoted to be $V_{n,3Tr}$. Furthermore, $kT/C$ noise of the two S/H circuits, $V_{n,SHS}$, $V_{n,SHR}$ are added. With the source follower gain of 0.8, the resulting noise voltage of Fig. 10 is given by

$$V_{n, sensor} = 0.8 \sqrt{V_{n,3Tr}^2 + V_{n,SHS}^2 + V_{n,SHR}^2}$$

If $C_{SHS} = C_{SHR} = 40 \, \text{ff}$, the noise voltage is estimated to be $0.49 \, \text{mVrms}$.

The calculated value compared with Type1 is shown in Table 3. The converted noise is estimated 1.7 times that of Type 1. With a 3-Tr sensor in this form, it is imagined the only way to improve the sensitivity is to use a readout amplifier. The standardized noise level can be regarded as a criterion for determining the practical value of an image sensor as shown in the above.

In the pixel of Fig. 10, the additional noise due to the readout circuits must be taken into account because of the low sensitivity. Therefore, the advantage in noise level of the Type1 is higher than the result of Table 3.

4. CONCLUSION

Through this experiment, we have had knowledge in CDS for CMOS image sensors for high-speed video cameras. Also, we have found that there is a great possibility of increasing the number of transistors to form a pixel, by using an advanced CMOS process, resulting in a decreased FD capacity. This can increase the aperture ratio, which makes us believe the advantage of the differential output scheme for image sensors over the other techniques.

As the result of all the above, we were able to increase the sensitivity of image sensor with differential output 3 times as high as before, and the dynamic range by 7dB. It was also found that our image sensor would show a dynamic range 2dB wider than the 3-Tr sensor with rolling shutter, assuming both have the same sensitivity.

As presented in the above, our proposed pixel circuitry with differential output was found to have much better performance in sensitivity and noise level in black level than 3-Tr sensor or a sensor with in-pixel CDS. The above predicts that there is a possibility that a high-speed CMOS image sensor with a wider dynamic range, while assuring high-speed recording capability, will be implemented in the future.
Table 1 Specification of 3 types of pixel circuits

<table>
<thead>
<tr>
<th></th>
<th>Type1</th>
<th>Type2</th>
<th>3 Tr. pixel rolling shutter</th>
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<tr>
<td>CMOS process [µm]</td>
<td>0.25</td>
<td>0.6</td>
<td>0.25</td>
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<tr>
<td>Pixel pitch [µm]</td>
<td>20 x 20</td>
<td>20 x 20</td>
<td>20 x 20</td>
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<tr>
<td>Fill factor [%]</td>
<td>48</td>
<td>30</td>
<td>56</td>
</tr>
<tr>
<td>Device counts</td>
<td>11 Tr.</td>
<td>8 Tr.</td>
<td>3 Tr.</td>
</tr>
<tr>
<td>number of pixels</td>
<td>256 x 1</td>
<td>256 x 256</td>
<td>256 x 1</td>
</tr>
<tr>
<td>column amplifier gain</td>
<td>1 x</td>
<td>4 x</td>
<td>1 x</td>
</tr>
</tbody>
</table>

Fig. 8 Sample images: (a) TYPE1 pixel, line sensor; and (b) TYPE2 pixel, area sensor

![Sample images](image1.png)

Fig. 9 Sensor sensitivity

![Sensor sensitivity graph](image2.png)
Table 2 Comparison of sensitivity and noise

<table>
<thead>
<tr>
<th></th>
<th>Type1</th>
<th>Type2</th>
<th>3 Tr. pixel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity [V/lux-sec]</td>
<td>34.5</td>
<td>11.1</td>
<td>4.3</td>
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<tr>
<td>Random noise [mVrms]</td>
<td>2.43</td>
<td>2.52</td>
<td>0.38</td>
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<td>Noise ratio</td>
<td>1</td>
<td>3.2</td>
<td>1.2</td>
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Exposure time: 1msec

![3-Tr. pixel circuits with global shutter](image)

Table 3: Comparison of Type1 and 3-Tr. pixel with global shutter

<table>
<thead>
<tr>
<th></th>
<th>Type1</th>
<th>3 Tr. pixel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity [V/lux-sec]</td>
<td>34.5</td>
<td>4.0</td>
</tr>
<tr>
<td>Random noise [mVrms]</td>
<td>2.43</td>
<td>0.61</td>
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<td>Noise ratio</td>
<td>1</td>
<td>1.7</td>
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</tbody>
</table>

Exposure time: 1msec

REFERENCES


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