An Energy-Recovery Sustaining Driver with Discharge Current Compensation for AC Plasma Display Panel

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Abstract—A novel driver with discharge current compensation is proposed to drive an ac plasma display panel (PDP). This proposed circuit uses resonance between the inductor and the ac PDP to avoid abrupt charging/discharging. The four switches of the full bridge are all operated with zero-voltage-switching turn-on. In addition, an 8-in ac PDP equipped with the proposed driving circuit, operating at 100 kHz, is investigated. With the discharge current compensation, the experimental results show that the proposed driver can maintain the ac PDP to light at lower voltage (129 V).

Index Terms—Current compensation, energy recovery, plasma display panel.

I. INTRODUCTION

PLASMA DISPLAY is known for its features of light weight, thinness, wide viewing angle, long lifetime, and high contrast, which is especially suitable for HDTV, as shown in Fig. 1. Fig. 1 is a sectional view showing an example of a structure of one discharge cell in an ac plasma display panel (PDP). An ac PDP display is composed of front and rear glass substrates. The separation between the two opposing substrates is about 100–130 μm and the space between them is filled typically with a gas mixture of Ne and Xe. The pressure of the gas is approximately 400–500 torr. The front glass substrate has a first electrode (X electrode) and a second electrode (Y electrode) which operate as sustaining electrodes. The X and Y electrodes are coated with bus electrodes, dielectric layer, and MgO layer in sequence. The MgO protects the dielectric from plasma damage and also aids the plasma in sustaining a discharge through secondary electron emission from its surface. In addition, equivalent capacitor exists between the X and Y electrodes [1], [2]. On the surface of the rear glass substrate opposed to the front glass substrate, a third electrode operating as address electrode (A electrode) is formed to be orthogonal to the X and Y electrodes. Address electrodes are covered with three phosphors of red, green, and blue. In operation, an ac voltage sufficiently high will ionize the gas to create the plasma. Then, the ultraviolet light from the plasma excites the phosphor to create the color image.

Most ac PDPs utilize the address-display-separation (ADS) driving scheme, as shown in Fig. 2 [3], [4]. All X electrodes are bussed together and connected to a sustain driver. On the other hand, the Y electrodes are connected to a sustain driver through several scan ICs. One TV field is divided into 8 subfields (SFs), and each consists of a reset period, an address period, and a display period. In the reset period, a high voltage (usually larger than 340 V) is provided to turn on all the cells in order to obtain an identical initial condition for all the cells. In the address period, the Y electrodes receive scan pulses, together with data pulses on the address electrodes, to control wall charges in appropriate cells according to the image to be displayed. In the following display period, the sustain discharges take place between the electrodes X1–Y1, X2–Y2, X3–Y3, etc. Furthermore, gray scales are expressed by using the binary-coded light-emission-period method. The display periods are filled with trains of constant width and constant period pulses and their lengths are arranged according to the binary sequence, 1 : 2 : 4 : 8 : 16 : 32 : 64 : 128. Therefore, gray levels of 28 for each color (R, G, B) can be expressed with an 8-bit sequence.

The ac PDPs provide inherent memory characteristic, as explained in Fig. 3 [5], [6]. In general, the ac sustain square pulses,
whose voltage $V_S$ is smaller than breakdown voltage $V_{bd}$, cannot initiate a discharge, as shown in Fig. 3(a). If data pulses $V_d$, as shown in Fig. 2, are applied to the address electrodes, while scan pulses $-V_S$ are sequentially applied to each $Y$ electrode, the voltage $(V_d + V_y)$ is higher than $V_{bd}$ and a discharge ignites, as shown in Fig. 3(b). Charges, called wall charges (or wall voltage $V_{wall}$), deposit on the dielectric layer and reduce the effective voltage across the gap. Then, the discharge ceases after a short time, as shown in Fig. 3(c). When the polarity of the sustain pulse is reversed, the potential difference across the gap becomes larger than $V_{bd}$ by an amount determined by the wall charges, and a new discharge of different polarity occurs, as shown in Fig. 3(d). The buildup of wall charges again terminates the discharge, as shown in Fig. 3(e). The next discharge starts as the polarity of the sustain pulse is reversed.

If the sustain circuit abruptly charges and discharges the panel, stored capacitive energy will be lost. Several drivers have been proposed in recent years to recover most of this energy [7]–[15]. The basic idea is to charge and discharge the panel capacitance through an inductor instead of through the lossy resistance of a switch. Furthermore, the sustain driver must drive the panel capacitance at a frequency of typically 100 kHz.
and supply plasma discharge current spikes of up to 19 A when all pixels are in the on state for an 8-in plasma panel. One prior approach is discussed in the following section and the influence of the large plasma discharge current (19 A for an 8-in panel) on the driver is also investigated.

II. PRIOR APPROACH

Fig. 4 shows an energy-recovery circuit and its driving waveforms for ac PDPs [7]–[9]. Considering only the left-side circuit, the intrinsic panel capacitance $C_p$ and the energy recovery capacitance $C_{SSS1}$ (which are series connected by an external inductor $L_1$). The driver utilizes the series resonance among $C_p$, $L_1$, and $C_{SSS1}$ to charge or discharge the intrinsic panel capacitance $C_p$. The charging operation and subsequent discharging operation of the panel $C_p$ are divided into four time durations: $T_1$, $T_2$, $T_3$, and $T_4$, as shown in Fig. 4(b).

Before $T_1$, only the switches $M_3$ and $M_4$ are in the on state and the others are in the off state. The voltage $V_p$ is equal to zero.

During $T_1$, the switch $M_3$ is turned off and then the switch $M_5$ is turned on. An equivalent LC circuit as illustrated in Fig. 5 is formed. The voltage of the capacitance $C_{SSS1}$ is equal to $V_S/2$ in the steady state [7]. The panel voltage $V_p$ will be charged to $V_S$ at the end of $T_1$.

After $V_p$ is raised to $V_S$, the switch $M_1$ is turned on and then the switch $M_5$ is turned off. Namely, during $T_2$, $V_S$ is supplied from the power source through the switch $M_1$ to the panel. In other words, the voltage $V_S$ applied to the panel capacitor $C_p$ is sustained for the time duration $T_2$.

During $T_3$, the panel capacitance $C_p$ is discharged. The switch $M_1$ is turned off and then the switch $M_6$ is turned on. The discharging current of the capacitor $C_p$ begins to flow through the inductor $L_2$, the diode $D_2$, and the switch $M_6$ into the capacitor $C_{SSS1}$. The capacitor $C_{SSS1}$ is charged. The panel capacitor $C_p$ discharges until the voltage $V_p$ drops to zero voltage.

When the voltage $V_p$ is reduced to zero, the switch $M_3$ is turned on and then the switch $M_6$ is turned off. That is, during $T_4$, the ground potential is supplied through the switch $M_3$ to the panel. The zero voltage applied to the panel capacitor $C_p$ is sustained for the time duration $T_4$.

As described above, the charge/discharge currents flow through the inductor $L_1$, the LC resonance operation appears, and thereby the energy recovery effect can be obtained. In other words, the energy discharged from the energy recovery capacitance $C_{SSS1}$ is used to charge the intrinsic panel capacitance $C_p$ through the switch $M_5$ and the diode $D_1$, and the energy discharged from the capacitance $C_p$ can also be temporarily stored in the capacitance $C_{SSS1}$. Therefore, most energy is recovered and high efficiency is achieved.

During $T_1$, when the intrinsic panel capacitance is charged to exceed the firing voltage $V_f$ [$V_f + V_w = V_{ad}$, as shown in Fig. 4(b)], the gas in the plasma display panel would start to discharge. However, there is an interval (about 100–200 ns) between the instant $V_p$ reaches $V_f$ and the gas starts to discharge. Generally, the inductance $L_1$ or $L_2$ is small enough, and the voltage $V_p$ can be quickly charged to $V_S$ before the gas starts to discharge. In such condition, although the series resonance finishes completely, the large discharge current going through the on resistance of the switches $M_1$ and $M_4$ or $M_2$ and $M_3$ would cause voltage notch across the panel. We utilize the prior circuit in Fig. 4(a) to drive an 8-in ac PDP. The experimental arrangement and waveforms are shown in Fig. 6. The test pattern is the white image. In other words, all pixels are in the on state. As shown in Fig. 6(b), the current $I_p$, which goes through the panel, has several spikes. The smaller ones are the displacement currents to charge and discharge the panel capacitance $C_p$. The larger ones are the plasma discharge currents needed for the gas to discharge. However, when the plasma discharge occurs, the large discharge current goes through the switches $M_4$ and $M_1$ or $M_2$ and $M_3$, and causes voltage drops on the switches $M_4$ and $M_1$, indicated by the circle in Fig. 6(b). In addition, as the voltage decreases, so does the accumulated amount of wall charge. The problem of voltage notch appears in all prior arts.
Fig. 6. Experiment of the prior circuit. (a) Experimental arrangement. (b) Voltage $V_p$ and current $I_p$ across the 8-in ac PDP (time: $\mu$s/div).

Fig. 7. Proposed circuit. (a) Circuit structure. (b) Driving waveforms.
In this paper, a novel driver with discharge current compensation is proposed. The operation principles of the proposed driver are analyzed in the following section. Then, the same 8-in PDP equipped with the proposed driving circuit is investigated to verify the theoretical analysis.

III. PROPOSED CIRCUIT

A. Principle of Operation

Fig. 7(a) is the embodiment of the proposed driver for ac PDPs, where \( D_1 \sim D_6 \) are the body diodes of MOSFETs \( M_1 \sim M_6 \) from source to drain. The capacitors \( C_1 \sim C_4 \) are parasitic components of the switches \( M_1 \sim M_4 \). Moreover, the diodes \( D_7 \) and \( D_8 \) are used to prevent high voltage across \( M_5 \) and \( M_6 \), which results from the resonance between the inductors \( L_1 \), \( L_2 \) and the parasitic capacitance of the other parts [15].

Before the panel is charged or discharged, the switches \( M_1 \) and \( M_4 \) are turned on. After a predetermined period of time, the switch \( M_3 \) is turned on, and the current \( I_{L_1} \) of the inductor \( L_1 \) is increased linearly until no less than the plasma discharge current. Then, turn off the switches \( M_1 \) and \( M_4 \), and a resonance is brought about by the parallel resonance between the panel capacitance \( C_p \) and the inductor \( L_1 \) through the diode \( D_9 \) and the switch \( M_5 \). With this arrangement, the abrupt charging/discharging operation of the panel capacitance is avoided. The plasma discharge current is provided by the inductor current \( I_{L_1} \). The large discharge current would not flow through the switches \( M_1 \) and \( M_4 \), and the voltage notch across the on resistance of the switches \( M_1 \) and \( M_4 \) would not appear.

When the voltage \( V_p \) reaches \( -V_S \), the switches \( M_2 \) and \( M_3 \) are turned on with zero-voltage switching (ZVS). At this time, the current \( I_{L_1} \) of the inductor \( L_1 \) is decreased linearly with slope \( -V_S/L_1 \). When the current \( I_{L_1} \) decreases to zero, turn off the switch \( M_5 \). The operation of the adjacent half of period is similar to that described above.
In the proposed circuit, there is no sudden voltage drop in the driving waveform $V_p$ when the panel discharges. It will attract more wall charge to deposit on the dielectric layer of the electrodes. In other words, the wall voltage is larger, and it helps the panel maintain to light at lower voltage.

### B. Equivalent Circuit Analysis

Shown in Fig. 7(b) are the driving waveforms of the proposed circuit. One period of the driving operations is divided into two half cycles, $t_0 \sim t_6$ and $t_6 \sim t_{12}$. Because the operation principles of the two half cycles are symmetric, only the first half cycle is explained as follows.

**Stage 1 ($t < t < t_0$):** The panel capacitance $C_p$ is connected between the power source $V_S$ and GND with the switches $M_1$ and $M_4$ turning on.

**Stage 2 ($t_0 < t < t_1$):** At $t_0$, the switch $M_5$ is turned on. At this time, the voltage across $L_1$ is $V_S$ and the current $I_{L_1}$ of the inductor $L_1$ begins to increase linearly with slope $V_S/L_1$.

**Stage 3 ($t_1 < t < t_2$):** At $t_1$, the switch $M_4$ is turned off and the inductor current $I_{L_1}$ starts to charge $C_4$ and discharge $C_2$ and $C_p$ at the same time, as shown in Fig. 8(a). When $V_S$ increases to $V_S$, $D_2$ becomes conductive and $I_{L_1}$ will go through $D_2$. Then, the switch $M_2$ is turned on with ZVS at $t_2$.

**Stage 4 ($t_2 < t < t_3$):** As shown in Fig. 8(b), with the switches $M_3$ and $M_2$ conducting, the voltage $V_p$ across the panel is equal to zero. In addition, the voltage across $L_1$ is zero so that the inductor current $I_{L_1}$ keeps constant and circulates through $L_1$, $D_3$, $M_5$, $D_2$, and $M_4$.

**Stage 5 ($t_3 < t < t_4$):** At $t_3$, the switch $M_1$ is turned off and the inductor current $I_{L_1}$ starts to charge $C_1$ and discharge $C_3$ and $C_p$ at the same time, as shown in Fig. 8(c). When $V_X$ decreases to zero, $D_3$ becomes conductive and $I_{L_1}$ will go through $D_3$. Then, the switch $M_3$ is turned on with ZVS at $t_4$.

**Stage 6 ($t_4 < t < t_5$):** As shown in Fig. 8(d), with the switches $M_3$ and $M_2$ conducting, the voltage $V_p$ across the panel is equal to $-V_S$. An interval (about 100 ~ 200 ns) after $t_4$, the plasma starts to discharge. At the same time, the large discharge current is provided by the inductor current $I_{L_1}$ and is not provided by the power supply $V_S$ through the switches $M_2$ and $M_3$. Thus, there are no voltage drops across the on resistance of the switches $M_2$ and $M_3$. In other words, the voltage $V_p$ across the panel keeps $-V_S$ during the plasma discharge. In addition, the voltage across the inductor $L_1$ is equal to $-V_S$ during this period. Therefore, the inductor current $I_{L_1}$ begins to decrease linearly with slope $-V_S/L_1$ and the energy stored in $L_1$ is recovered back to the power supply $V_S$ through $D_3$, $L_1$, $D_3$, $M_5$, $D_2$, and $D_2$. When $I_{L_1}$ becomes zero, $D_2$ and $D_3$ will be turned off naturally without the problem of reverse recovery. Then turn off the switch $M_5$.

**Stage 7 ($t_5 < t < t_6$):** The panel capacitance $C_p$ is connected between the GND and power source $V_S$ with the switches $M_2$ and $M_3$ turning on. The voltage $V_p$ of the panel is equal to $-V_S$.

Circuit operations of $t_0 \sim t_{12}$ are similar to that of $t_0 \sim t_6$. Subsequently, the operations from $t_0$ to $t_{12}$ are repeated.
C. Design Considerations

In this proposed circuit, the inductor current $I_{L1}$ or $I_{L2}$ is mainly used to provide the large discharge current. So the discharge current must be measured first. In the experiment, the discharge current spike is about 19 A when all pixels are in the on state for an 8-in diagonal display panel, as shown in Fig. 6(b). During the periods ($t_0$–$t_4$) and ($t_6$–$t_7$), the voltage $V_S$ charges the inductor $L_1$ and $L_2$, respectively. Therefore, the inductor current $I_{L1}$ and $I_{L2}$ increases linearly with slope $V_S/L_1$ and $V_S/L_2$. The charging equations of the inductor $L_1$ and $L_2$ are as follows:

\[ V_S = L_1 \times \frac{I_{L1,\text{max}}}{t_4 - t_0} \]  
\[ V_S = L_2 \times \frac{I_{L2,\text{max}}}{t_6 - t_5} \]  

where $I_{L1,\text{max}}$ and $I_{L2,\text{max}}$, shown in Fig. 7(b), are the maximum currents of the inductors $L_1$ and $L_2$. The current $I_{L1,\text{max}}$ and $I_{L2,\text{max}}$ should be no less than the plasma discharge current, and we select the current $I_{L1,\text{max}}$ and $I_{L2,\text{max}}$ equal to 20 A. Furthermore, the inductor $L_1$ and $L_2$ need the same interval to charge and discharge. In other words, the interval ($t_4 - t_0$) is equal to ($t_5 - t_4$), and the interval ($t_7 - t_6$) is equal to ($t_6 - t_1$), as shown in Fig. 7(b). In addition, they must satisfy the following equations:

\[ (t_1 - t_0) + (t_{11} - t_{10}) \leq (t_{13} - t_{10}) \]  
\[ (t_5 - t_4) + (t_7 - t_6) \leq (t_7 - t_5) \]  

In the experiment, the frequency of the sustain pulse is 100 kHz and its duty is about 36%. Therefore, it is satisfied that the interval ($t_4 - t_0$) and ($t_7 - t_6$) are equal to 1. Then, from (3) and (4), we can determine that the values of $L_1$ and $L_2$ are 8 $\mu$H when $V_S$ is equal to 160 V.

IV. EXPERIMENTAL RESULTS

Fig. 9 is the experimental arrangement of the proposed circuit with its associated parameters. The ac plasma display panel under test is 8-in diagonally, which is the same as the one in Fig. 6(a). All $X$ electrodes are bussed together and connected to one leg of the proposed circuit. All $Y$ electrodes are also bussed together and connected to the other leg of the proposed circuit. In addition, all address electrodes are shorted together and connected to ground. Moreover, the frequency of the sustain pulses is 100 kHz. The test pattern is the white image, that is, all pixels are in the on state.

Fig. 10 shows the experimental waveforms of the proposed circuit. The waveforms are in good agreement with those in Fig. 7(b). With the discharge current compensation from $I_{L1}$ and $I_{L2}$, the notch of the voltage $V_p$ across the panel disappears. It is also observed that the resonance between the panel capacitance $C_p$ and inductor $L_1$ or $L_2$ results in the soft transition of $V_p$.

Fig. 11 shows that ZVS of the switches $M_1$–$M_4$ is achieved. Fig. 11(a) shows that the switch $M_1$ is turned on after $V_{ds, M_1}$ drops to 0 V. Similarly, Fig. 11(b)–(d) shows that $M_2$–$M_4$ are turned on with ZVS, respectively.
Comparing the lowest operation voltage of the proposed circuit with that of the prior circuit in Fig. 6(a), we find that the proposed circuit can maintain the panel to display the white image at 129 V. However, the prior circuit cannot maintain the panel to light when the sustain voltage is lower than 134 V. In general, the operational margin of the sustain voltage (\(V_{S_{\text{max}}} - V_{S_{\text{min}}}\)) is about 30 V. To reduce the sustain voltage by 5 V means that the operational margin is improved by 16.7%. This is because the problem of the voltage notch is solved by the discharge current compensation. In addition, this solution improves the accumulation of wall charge but also maintain the operational margin of the sustain voltage (\(V_{S_{\text{max}}} - V_{S_{\text{min}}}\)).

V. CONCLUSION

A novel driver for an ac PDP has been proposed in this paper. It utilizes inductors to resonate with the equivalent intrinsic capacitance of an ac PDP. The abrupt charging/discharging operation can be avoided, and all four switches of the full bridge are operated with ZVS turn-on. In particular, the proposed discharge current compensation could solve the problem of sudden voltage drop during gas discharge. This solution cannot only improve the accumulation of wall charge but also maintain the panel to light at lower sustain voltage than all prior arts.

REFERENCES


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