What Is Write Caching, and Why Would I Enable It in My SSD?

“Caching” generally refers to pairing a high-speed storage medium with a lower-speed storage medium to accelerate overall system performance. In the case of an SSD, the cache is DRAM that sits between the host and the NAND, as shown in Figure 1.

There are two types of cache: read cache and write cache. The same physical devices can be used for both; only the direction/flow of the data is reversed. For SSDs, the cache is the DRAM on the SSD main board.

This brief provides an overview of the differences in SSD behavior when write cache is enabled versus disabled, with an emphasis on the following points:
- The way data moves from the host to the drive
- The differences in communication flow between write cache enabled versus write cache disabled
- The potential risk in enabling write cache

Communications: Transmit, Receive, and “ACK”

As data moves between two locations in any system, a communication flow occurs. There are three main steps to any data-movement sequence:
- Transmit: the action of sending data
- Receive: the action of receiving the data
- Acknowledge (“ACK”): the notification from the receiver to the transmitter that the data was successfully communicated

These steps occur in sequence: Transmit > Receive > Acknowledge.

Figure 1: SSD cache model
SSD Elements: Transmitters and Receivers

For the scope of this document, we will assume that the transmitter is the host system and that the receiver is the SSD. This corresponds to a “write” command in which the host writes (transmits) data to the SSD (the receiver). The communications channel between the two is the host/drive interface. This can be SAS, SATA, FibreChannel, or any other drive interface.

Write Traffic Flow: Cache Enabled

When a host-to-SSD write occurs, data flows from the host, through the host:drive interface, to the SSD. Write cache enabled means that the SSD tells the host, “I have the data; please continue processing” as soon as the data reaches the DRAM buffer on the SSD. The data is moved from the DRAM buffer into the NAND opportunistically—that is, the SSD firmware controls this process and moves the data.

Write Traffic Flow: Cache Disabled

When a host-to-SSD write occurs, data flows from the host, through the host/drive interface, to the SSD. This process is the same when write cache is enabled, but the sequence of communication is different.

Potential Risk: Data Loss on Sudden Power Loss

Although enabling write cache can substantially improve performance, it does increase the risk of data loss if the system power fails suddenly and unexpectedly.

Why? Because when write cache is enabled, the drive “tells” the host that it “has the data” as soon as the data reaches the SSD DRAM buffer. The DRAM buffer is volatile (that is, it loses its contents when the power is removed). When the host receives the “ACK” message, the host assumes that the data is on the drive (and it is, but only on the drive’s DRAM) and will continue processing. If power is lost before the firmware moves the data from DRAM to NAND, the data is lost—but the host is completely unaware.

Generally speaking, this is an acceptable risk in client systems. Enterprise systems, however, typically run with write cache disabled for the extra assurance that the data is more secure, that the host “knows” for certain when the data is in the NAND, and that the host knows how to handle sudden power losses (typically, by executing a write retry).
## Write Traffic Flow: Cache Enabled

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<tr>
<th>Steps</th>
<th>Dialogue</th>
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| 1 | The host transmits data through the drive interface (SATA) to the SSD.  
Host to SSD: “...I'm sending you data; let me know when you have it...” |
| 2 | The data moves from the host, through the drive interface, and into the DRAM buffer on the SSD.  
Note: Data always goes to the DRAM buffer on the SSD first—never straight to the NAND. |
| 3 | The SSD then tells the host that it has a copy of the transmitted data and that the host is free to continue processing.  
SSD to host: “...OK, I have the data...” |

**Figure 2:** The host transmits data to the SSD's DRAM buffer.  

**Figure 3:** The data moves through the SATA interface and is received in the DRAM buffer.  

**Figure 4:** The DRAM buffer immediately sends the host an acknowledgement of the data's arrival.
### Write Traffic Flow: Cache Disabled

<table>
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<th>Steps</th>
<th>Dialogue</th>
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| 1     | The first step in the traffic flow when write cache is disabled is the same as when it is enabled: the host transmits data through the drive interface (SATA) to the SSD.  
Host to SSD: “…I’m sending you data; let me know when you have it…”  
**Figure 6:** The host transmits data to the SSD’s DRAM buffer. |
| 2     | The data moves from the host, through the drive interface, and into the DRAM buffer on the SSD.  
Note: Data always goes to the DRAM buffer on the SSD first—never straight to the NAND.  
**Figure 7:** The data moves through the SATA interface and is received in the DRAM buffer. |
Conclusion

Enabling the write cache on any target adjusts how that target interacts with the host during data transmission and reception. With the cache enabled, the target acknowledges reception of data sooner, but because that data is stored (temporarily) in volatile DRAM, the data is potentially at risk due to sudden power loss. With the cache disabled, that acknowledgement does not occur until the data has been successfully programmed into the NAND.

While enabling the write cache on the SSD may improve performance in certain workloads, doing so requires an understanding of the resultant operations and the potential risks. For many hosts, the benefits far outweigh any associated risks (some of which can be mitigated by the use of an uninterruptable power supply [UPS]), while for others it does not. Because both the benefits and the potential risks are both platform- and workload-dependent, designers should give careful consideration to deciding whether to enable the write cache.

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