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Novel Approaches to Low Leakage and Area Efficient VLSI Design

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***Abstract*-- The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Thinner gate oxides have led to an increase in gate leakage current. Today leakage power has become an increasingly important issue in processor hardware and software design. With the main component of leakage, the sub-threshold current, exponentially increasing with decreasing device dimensions, leakage commands an ever increasing share in the processor power consumption. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. According to the International Technology Roadmap for Semiconductors (ITRS) [1], leakage power dissipation may eventually dominate total power consumption as technology feature sizes shrink. While there are several process technology and circuit-level solutions to reduce leakage in processors, we propose novel approaches for reducing both leakage and dynamic power with minimum possible area and delay trade off.**

I. INTRODUCTION

For the most recent CMOS feature sizes (e.g., 90nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers.

International technology roadmap for semiconductors (ITRS) [1] reports that leakage power dissipation may come to dominate total power consumption. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching, and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18µ technology and above) the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to 0.09µ and 0.065µ, static power has become a great challenge for current and future technologies.

There are many reasons for which power losses occur in CMOS circuit. Figure 1 shows different types of leakage components. They are:

1. Sub-threshold leakage (weak inversion current)
2. Gate oxide leakage (Tunneling current)
3. Channel punch through
4. Drain induced barrier lowering

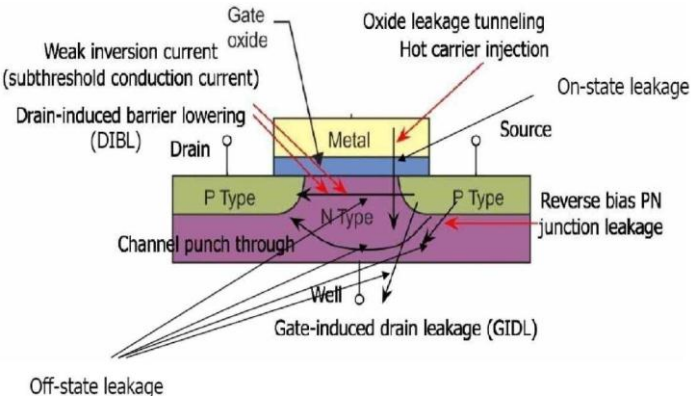

Figure 1: Leakage power components in CMOS 1

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One of the main reasons causing the leakage power increase is increase of sub-threshold leakage power. The Sub-threshold conduction or the sub-threshold leakage or the sub-threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The sub-threshold region is often referred to as the weak inversion region. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases which increases the sub-threshold leakage power. Next the gate oxide leakage, the gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance. But as the gate oxide is made thinner the barrier voltage of the oxide changes. For the positive gate voltage thus some positive charges get stuck in the oxide. Therefore, current flows through the oxide. This is also known as tunneling current.

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

Drain induced barrier lowering or DIBL is referred to the reduction of threshold voltage of the transistor at higher drain voltages. The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrode charges: the gate, the source and the drain.

As drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, an effect equivalent to lowering the threshold voltage of the device.

II. Design Criteria

For widely using of CMOS technology is basically for consuming less power. But as the technology feature size s hrink sub-threshold leakage current is increases as the decrease of threshold voltage. In this design criterion it focuses on sub threshold leakage power consumption and it also focuses on body biasing effect and stack effect. Finally we explain the switching power and delay tradeoff of generic CMOS circuit.

2.1 Leakage Power

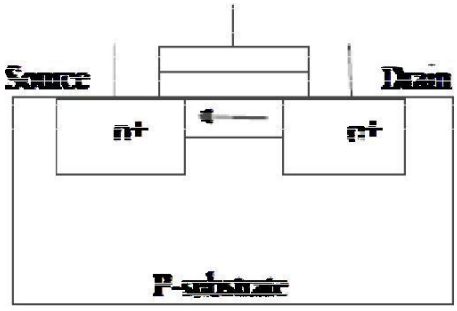

Figure 2.1(a): Sub-threshold Leakage of an NMOS

In 0.18u and above technology dynamic power is the dominant factor but 0.13u and below static power is another dominant factor for power consumption n. One of the main contributors for the static power consumption is sub-threshold leak age current which is shown in the Figure 2.1(a) i.e., the drain to source current when the gate voltage is smaller than the threshold voltage. As the technology feature size shrink sub-threshold leakage current is increases exponentially as the decrease of threshold voltage.

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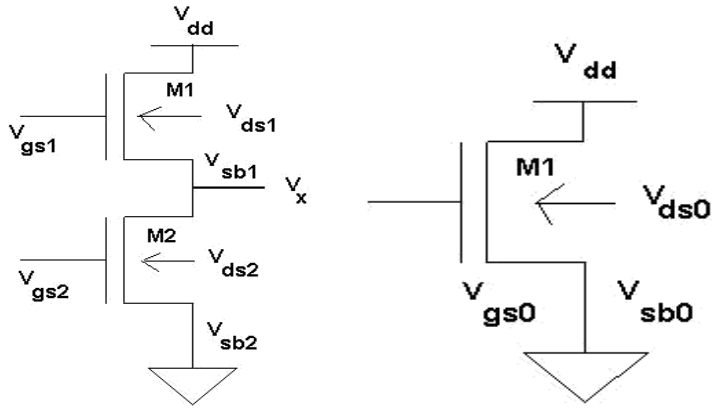

Figure 2.1(b): (i) Single Transistor **(ii) Stacked transistor**

Stacking transistor can reduce sub-threshold leakage [2]. So it is called stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power.

2.2 SRAM cell leakage path

In this section, we explain the major sub-threshold leakage components in a 6-T SRAM cell. The sub-threshold leakage current in an SRAM cell is typically categorized into two kinds [4] as shown in Figure 2.3, (i) cell leakage current that flows from Vdd to Gnd internal to the cell and (ii) bitline leakage current that flows from bitline (or bitline') to Gnd.

Although an SRAM cell has two bitline (BL) leakage paths, the bitlin e leakage current and bitline' (BL') leakage current differs according to the value stored in the SRAM bit. If an SRAM cell holds '1' as shown in Figure 2.3, the bitline leakage current passing through N3 and N2 is effectively suppressed due to two reasons. First, after precharging bitline and bitline' both to '1,' the source voltage and the drain voltage of N3 are the same, and thus potentially no current flo ws through N3. Second, two stacked and turn ed off transistors (N2 and N3) induce the stack effect.

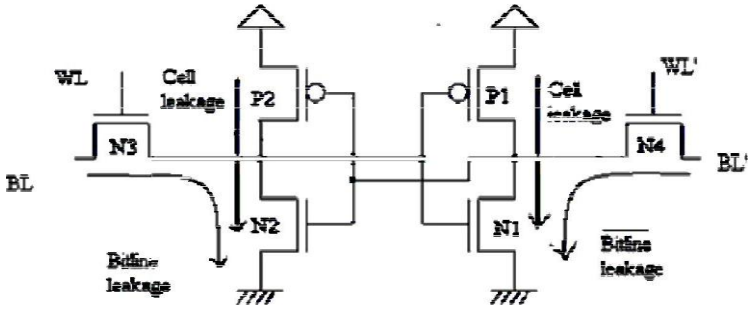

Figure 2.3: SRAM cell leakage paths

Meanwhile, for this case where the SRAM bit holds value '1', a large bitline' leakage current flows passing through N4 and N1. If, on the other hand, the SRAM cell holds '0,' a large bitline leakage current flows while bitline' leakage current is suppressed.

Meanwhile, for this case where the SRAM bit holds value '1', a large bitline' leakage current flows passing through N4 and N1. If, on the other hand, the SRAM cell holds '0', a large bitline leakage current flows while bitline' leakage current is suppressed.

III. PROPOSED METHODS

In this section, we introduce our new leakage power reduction techniques. At first we will discuss the structure of the techniques then we will show the operations of these techniques.

3.1Forced sleep method

We introduce our new leakage power reduction technique. In this technique we use the concept of the forced stack technique and the sleep transistor technique.

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Though this new method has a delay penalty greater than the forced stack and sleep transistor technique, this technique is far better than any prior approach known to us. The forced sleep method can achieve ultra-low leakage power consumption.

3.1.1 Structure of forced sleep Method

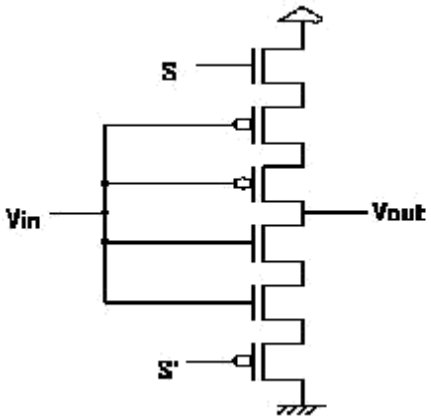

Figure 4.1: Structure of forced sleep Method

The forced sleep method has a structure merging the forced stack technique and the sleep transistor technique. Figure 3.1 shows a forced sleep inverter. The forced sleep inverter in Figure 4.1 uses W/L = 3 for the pmos transistors and W/L = 1.5 for the nmos transistors, while a conventional inverter with the same input capacitance would use W/L = 6 for the pull-up transistor and W/L = 3 for the pull-down transistor (assuming μn = 2μp). Then sleep transistors are added in series to each set of two stacked transistors. We use two sleep transistors here, the nmos sleep transistor with Vdd and the pmos sleep transistor with ground. Conventionally the nmos transistor is connected to ground because it is very efficient passing ground voltage and the pmos transistor is connected to Vdd because it is efficient passing Vdd [15]. In forced sleep method we just reverse the connection. That's why we have some delay penalty in our method.

We use same W/L for all the pmos and nmos transistors in this method. However, changing the sleep transistor width may provide additional tradeoffs between delay, power and area.

3.1.2 Operation of forced sleep method

Now we explain how the forced sleep works during active mode and during sleep mode. Also, we explain leakage power saving using forced sleep structure. The sleep transistors of forced sleep method operate similar to the sleep transistors used in the sleep transistor technique in which sleep transistors are turned on during active mode and turned off during sleep mode. Figure 4.1 depicts the forced sleep operation using a forced sleep inverter. During active mode (Figure 4.1), S = 1 and S' =0 are asserted, and thus all sleep transistors are turned on. As we said before that the nmos transistor is connected in Vdd. But it is not efficient in passing Vdd. So when the input is low output voltage is reduced to Vdd – Vth [15]. The drain terminal of the nmos sleep transistor is connected to Vdd. It is getting always a high voltage which is greater than the source terminal voltage of this nmos sleep transistor. Current Ids will flow through the transistor and the stacked transistors also. This nmos sleep transistor has its own internal resistance for which the leakage current will be less than that of a forced stack inverter circuit when the input voltage is low. The pmos is connected to ground. When the input signal is high voltage the output is 0-Vth . The source terminal voltage is higher than the drain terminal voltage of the pmos sleep transistor. Current Ids will flow through the transistors. For an internal resistance of the pmos sleep transistor the leakage current will be much less than any other approaches.

During sleep mode (Figure 4.1), S = 0 and S' =1 are asserted, and so both of the sleep transistors are turned off. The leakage reduction of forced sleep structure occurs in two ways. First, leakage power is suppressed by the two sleep transistors which are not efficient in passing Vdd (nmos) and ground (pmos) potential. They will be in pure sleep mode at sleep mode operation. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the forced sleep technique achieves ultra-low leakage power consumption during sleep mode. The price for this, however, is increased delay.

3.2 Stacked sleep approach

This is another new leakage reduction technique. In this technique the sleep transistors are getting stacked. That's why we call it ''Stacked sleep'' approach.

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3.2.1 Structure of Stacked sleep approach

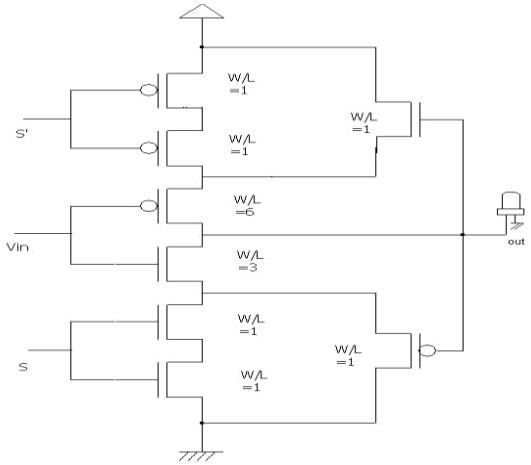

Figure 4.2: Structure of Stacked sleep approach

This technique uses two stacked sleep transistor in V_{dd} and two stacked sleep transistor in ground. So, leakage reduction in this technique occurs in two ways. First, the stack effect [16] of sleep transistors and second, the sleep transistor effect. It is well known that pmos transistors are not efficient at passing GND; similarly, it is well known that nmos transistors are not efficient at passing V_{dd}. But this stacked sleep technique uses pmos transistor in GND and nmos transistor in V_{dd} for maintaining the exact logic state during sleep mode.

This stacked sleep transistor uses aspect ratio W/L=3 for nmos transistor and W/L=6 for pmos transistor in the main inverter portion. For the stacked sleep transistor this technique uses aspect ratio W/L=1 for both the nmos and pmos transistors. The extra two transistors of the design for maintaining the logic state during sleep mode also use aspect ratio W/L=1.

3.2.2 Operation of stacked sleep approach

Let us to maintain a value of '1' in sleep mode. During sleep mode S=0 and S'=1 are asserted. Assume that the '1' value has already been calculated. The stacked sleep approach uses this output value of '1' and an nmos transistor connected to V_{dd} to maintain output value equal to '1' when in sleep mode. As shown in the figure, an additional nmos transistor placed in parallel to the pull up sleep transistors connects V_{dd} to the pull up network. When in sleep mode this nmos transistor is the only source of V_{dd} to the pull up network since the sleep transistors are turned off.

Similarly to maintain a value of '0' in sleep mode, assume that the '0' value has already been calculated, the stacked sleep approach uses this output value of '0' and a pmos transistor connected to GND to maintain output value equal to '0' when in sleep mode. Figure 4.2 shows an additional pmos transistor placed in parallel to the pull down sleep transistors. When in sleep mode, this pmos transistor is the only source of GND to the pull down network since the sleep transistors are turned off.

33 Variable body biasing technique

This is another new leakage reduction technique, which we call the ''Variable body biasing'' technique.

3.3.1 Structure of variable body biasing technique

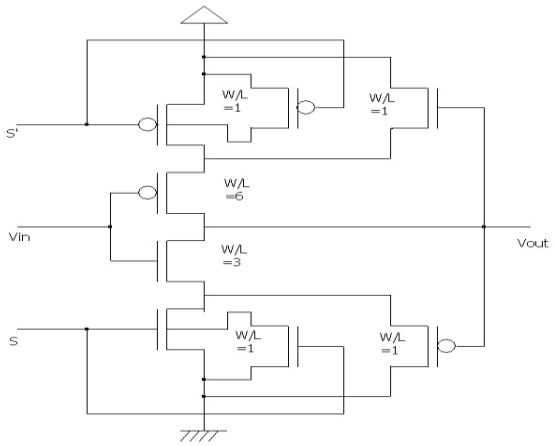

Figure 4.3: Structure of variable body biasing technique

This technique in figure 4.3 uses two parallel connected sleep transistors in V_{dd} and two parallel connected sleep transistors in GND. The source of one of the pmos sleep transistor is connected to the body of other pmos sleep transistor for having so called body biasing effect. Similarly the source of one of the nmos sleep transistor is connected to the body of other nmos sleep transistor for having the same effect as for pmos sleep transistors. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the variable body biasing effect. It is well known that pmos transistors are not efficient at passing GND; similarly, it is well known that nmos transistors are not efficient at passing V_{dd}. But this variable body biasing technique uses pmos transistor in GND and nmos transistor in V_{dd}, both are in paralleled to the sleep transistors, for maintaining exact logic state during sleep mode.

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This technique uses aspect ratio W/L=3 for nmos transistor and W/L=6 for pmos transistor in the main inverter portion. For the sleep transistors this technique uses aspect ratio W/L=1 for both the nmos and pmos transistors. The extra two transistors of the design for maintaining the logic state during sleep mode also use aspect ratio W/L=1. Due to the minimum aspect ratio the sub-threshold current reduces.

3.3.2 Operation of Variable body biasing technique

During active mode S=1 and S'=0 is asserted. Then the entire sleep transistors are ON and the inverter is in active mode. For different input signal desired output signal is caught. During sleep mode or inactive mode S=0 and S'=1 is asserted. Then the entire sleep transistor is turned OFF. Since the sources of the nmos and pmos sleep transistors are connected to the body of similar transistor as shown in figure 4.3, the threshold voltage of the sleep transistors increases due to the body biasing effect [17] during sleep mode. This increase of threshold voltage of the transistors reduces the leakage current. That's why the static power consumption is also lowers. This variable body biasing technique also has two extra transistors in parallel to the sleep transistors. The purpose of this extra transistor is to save data during inactive mode of the circuit.

Let us to save the value '1' in sleep mode. Assume that the '1' value has already been calculated. This technique uses this output value of '1' and an nmos transistor connected to V_{dd} to maintain output value equal to '1' when in sleep mode. When in sleep mode this nmos transistor is the only source of V_{dd} to the pull up network since the sleep transistors are turned off. Similarly to maintain a value of '0' in sleep mode, assume that the '0' value has already been calculated, this technique uses this output value of '0' and a pmos transistor connected to GND to maintain output value equal to '0' when in sleep mode. When in sleep mode, this pmos transistor is the only source of GND to the pull down network since the sleep transistors are turned off.

IV. Applying Proposed Methods

Forced sleep approach, Stack sleep approach and Variable body biasing techniques can successfully be implemented in logic design. To verify this statement here these methods are applied in 2 ways.

1. A chain of 4 inverters
2. SRAM cell

4.1 Application in logic circuit

A chain of four inverters is chosen as a logic circuit.

4.1.1 Forced sleep method using a chain of 4 inverters

A chain of four inverters is chosen because an inverter is the most basic logic circuit in CMOS technology. Figure 5.1.1 depicts a chain of four inverters using forced sleep method. We size the transistor of the inverter to have equal rise and fall times in each state. In this method we use aspect ratio W/L = 1.5 for all the nmos transistors and W/L = 3 for all the pmos transistors.

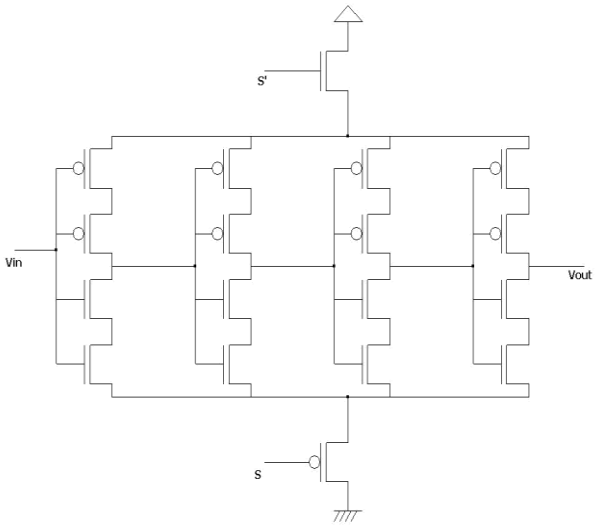

Figure 5.1.1: Forced sleep method using a chain of 4 inverters 23

4.1.2 Stacked sleep approach using a chain of 4 inverters

In this stacked sleep approach we size the transistors of the inverter to have equal rise and fall times in each state. Figure 5.1.2 depicts a chain of four inverters using stacked sleep approach. This method uses aspect ratio W/L = 3 for all nmos transistors and W/L = 6 for all pmos transistors in the main inverter circuit. For the sleep transistors and extra transistors it uses aspect ratio W/L = 1.

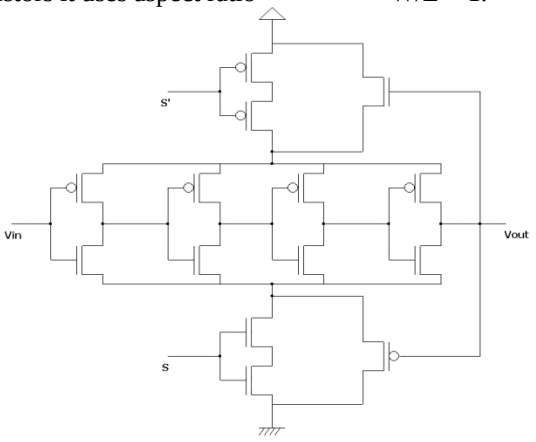

Figure 5.1.2: Stacked sleep approach using a chain of 4 inverters

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4.1.3 Variable body biasing technique using a chain of 4 inverters

In variable body biasing technique we size the transistors of the inverter to have equal rise and fall times in each state. Figure 5.1.3 depicts a chain of four inverters using variable body biasing technique. This method uses aspect ratio W/L = 3 for all nmos transistors and W/L = 6 for all pmos transistors in the main inverter circuit. For the sleep transistors and extra transistors it uses aspect ratio W/L = 1.

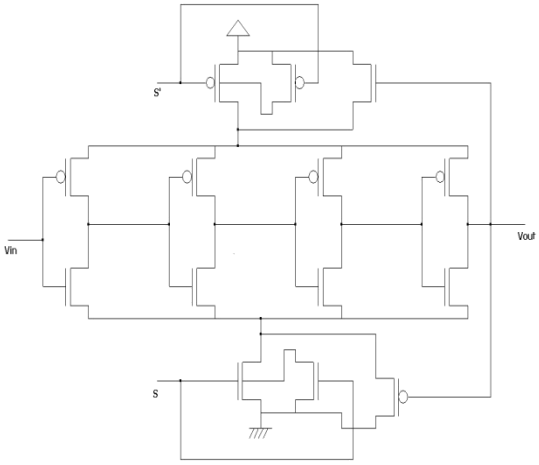

Figure 5.1.3 Variable body biasing technique using a chain of 4 inverters

4.2 Application in SRAM cell

We implement the techniques in SRAM cell.

4.2.1 Forced sleep application in SRAM cell

Figure 5.2.1 depicts the forced sleep application in SRAM cell.

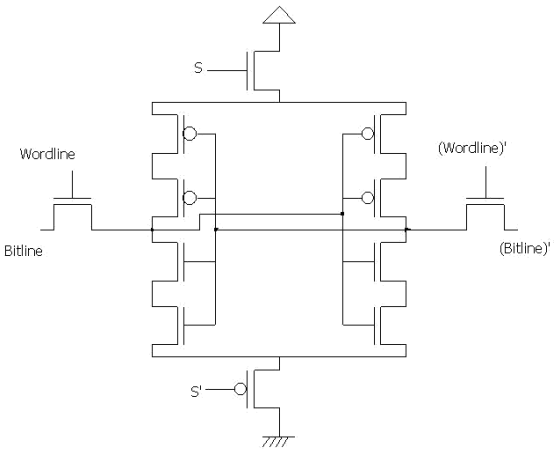

Figure 5.2.1: SRAM cell using forced sleep method

4.2.2 Stacked sleep application in SRAM cell

Figure 5.2.2 shows the stacked sleep application in SRAM cell.

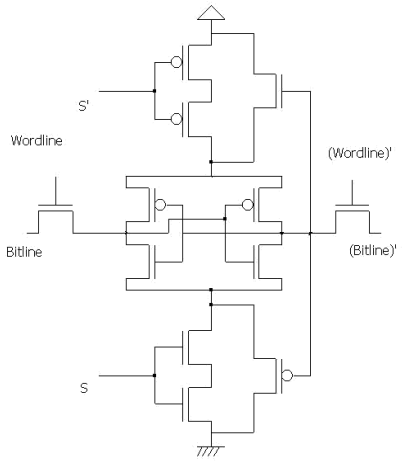

Figure 5.2.2: SRAM cell using stacked sleep approach

4.2.3 Variable body biasing application in SRAM cell

Figure 5.2.3 shows the application of variable body biasing technique in SRAM cell.

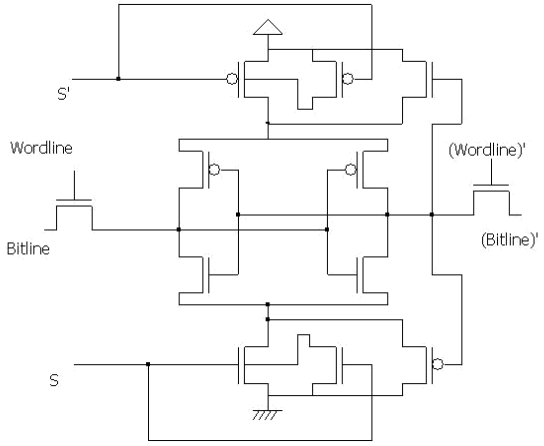

Figure 5.2.3: SRAM cell using variable body biasing technique

V. RESULTS

We compare the stacked sleep approach, variable body biasing technique and forced sleep technique to a base case (Figure 3.1) and five other previous approaches, namely sleep transistor, forced stack, sleepy stack, sleepy keeper and dual sleep. Thus, we compare nine design approaches in terms of power consumption (dynamic and static), delay and area. To show that the approaches are applicable to general logic design, we choose a chain of four inverters.

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We use Synopsis HSPICE [18] for simulation purpose to estimate delay and power consumption. Area is calculated with the help of MICROWIND. All considered approaches are evaluated for performance by using a single, low-Vth for all transistors.

The inverter chain uses three inverters each with W/L=6 for PMOS and W/L=3 for NMOS for the base case. For example, sleep transistors (Figure 3.2) used in the pull-up and pull-down networks of the base case inverter chain have W/L=6 and W/L=3, respectively. Transistors in the forced stack approach (Figure 3.3) are sized to half of the size of the base case transistors, e.g., transistors used in pull-up and pull-down of the base case inverter chain have W/L=3 and W/L=1.5, respectively. Similarly, transistors, including sleep transistors, in the sleepy stack approach are sized to half of the size of the base case transistors.

Variable body biasing technique (Figure 4.3) uses aspect ratio W/L=3 for NMOS transistor and W/L=6 for PMOS transistor in the main inverter portion. For the sleep transistors this technique uses aspect ratio W/L=1 for both the NMOS and PMOS transistors. The extra two transistors of the design for maintaining the logic state during sleep mode also use aspect ratio W/L=1. Stacked sleep approach also uses the same aspect ratio that is used in variable body biasing technique. In the forced sleep approach aspect ratio W/L=1.5 for NMOS and W/L=3 for PMOS is used.

For layout purpose we have used DSCH software where we have got a verilog while designing the circuit. Then after the compilation of the verilog file in MICROWIND software we got the accurate layout of the design. In this way we got the layout of each method. We have used BSIM4 PTM [19] technologies and adopted 130nm, 90nm, 45nm, 32nm and 22nm processes. The chosen technologies and their supply voltages are given in Table 1.

Table 1:
Power supply voltage for different technologies

180n	130n	90n	65n	45n	32n	22n
1.8V	1.3V	1.2V	1.1V	1.0V	0.9V	0.8V

5.1 Simulation results for logic circuits

The simulation results are given in tabulated and figure form below:

5.1.1 Simulation results for a chain of four inverters

Table 2 shows the result of different methods using 32 nm technologies.

Table 2:
Data for 32 nm technology:

Method	Prop. Delay (s)	Static power (w)	Dynamic power (w)	Area (μm^2)
Base case	2.4484E-11	8.7649E-08	3.6138E-06	1.20
Sleep	3.6201E-11	1.6272E-09	2.7774E-06	2.45
Forced stack	1.3511E-10	3.9920E-10	8.0436E-07	1.38
Sleepy stack	5.8477E-11	7.0533E-10	1.4503E-06	2.07
Sleepy keeper	4.0711E-11	1.4976E-09	2.8465E-06	1.83
Dual sleep	3.8831E-11	1.1840E-09	2.0870E-06	1.28
Stacked sleep	1.3128E-10	1.9640E-10	7.2014E-07	1.54
Variable body biasing	7.8629E-11	3.6360E-10	1.0344E-06	1.54
Forced sleep	3.3781E-09	5.9908E-12	1.3517E-07	1.78

REFERENCES

[1] International Technology Roadmap for Semiconductors by Semiconductor Industry Association, 2002. [Online] Available http://public.itrs.net

[2] J. Park, "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005. [Online].

[3] [3] Linda E. M. Brackenbury, "Design of VLSI Systems- A Practical Introduction",

[4] Department of Computer Science, Manchester University.

[5] KIM, C. and ROY, K., "Dynamic Vt SRAM: a Leakage Tolerant Cache Memory for Low Voltage Microprocessors," Proceedings of the International Symposium on Low Power Electronics and Design, pp. 251–254, August 2002.

[6] KIM, N., AUSTIN, T., BAAUW, D., MUDGE, T., FLAUTNER, K., HU, J., IRWIN, M., KANDEMIR, M., and NARAYANAN, V., "Leakage Current: Moore's Law Meets Static Power," IEEE Computer, vol. 36, pp. 68–75, December 2003.

[7] S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.

[8] NARENDRA, S., S. BORKAR, V. D., ANTONIADIS, D., and CHANDRAKASAN, A., "Scaling of Stack Effect and its Application for Leakage Reduction," Proceedings of 148 the International Symposium on Low Power Electronics and Design, pp. 195–200, August 2001.

[9] J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 148-158, September 2004.

[10] J. Kao and A. Chandrakasan, "MTCMOS sequential circuits, Proceedings of European Solid-Stat Circuits Conference, pp 332-335, September 2001.

[11] Se Hun Kim, V.J. Mooney, "Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design" Proceeding of the 2006 IFIP International Conference on Very Large Scale Integration, pp367-372, Oct. 2006.

[12] Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design Vincent J. Mooney III, School of Electrical and Computer Engineering, Georgia Institute of Technology , Atlanta, GA USA(mooney@ece.gatech.edu)

[13] Nittaranjan Karmakar, Mehdi Z. Sadi, Md. Khorshed Alam and M. S. Islam1, "A Novel Dual Sleep Approach to Low Leakage and Area Efficient VLSI Design" IEEE-RSM Proc. 2009, Kota Bahru, Malaysia

[14] NOSE, K. and SAKURAI, T., "Analysis and Future Trend of Short-Circuit Power," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 19, no. 9, pp. 1023–1030, September 2000.

[15] CHANDRAKASAN, A. P., SHENG, S., and BRODERSEN, R. W., "Low- Power CMOS Digital Design," IEEE Journal of Solid-State Circuits, vol. 27, no.4, pp. 473–484, April 1992.

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