Abstract
A non-contact method for parallel testing of System-in-Package (SiP) assemblies is presented. This technology allows for JTAG testing of partially or fully populated SiPs in wafer form, in advance of final packaging. The technology utilizes non-contact GHz short-range, near field communications to transfer bi-directional data to SiP substrates; creating a Wireless Test Access Port or WTAP. The system is integrated with a standard probe card to deliver power and wireless signals. The wireless probes convert high frequency RF (GHz) transceiver signals to standard tester ATE logic levels and allow the use of standard probers and JTAG testers. In addition, all transceivers (DUT and probe) use antenna structures and electronics that are fully CMOS compliant. Enhancing the economics of SiP manufacture by enabling parallel non-contact testing of SiPs before packaging is a key benefit of this technology.

1. Introduction
The Semiconductor Industry Association defines a SiP as any combination of semiconductors, passives, and interconnects integrated into a single package [1]. The testing of such heterogeneous SiP modules is a significant and growing problem in the electronics manufacturing industry, where current test technology only allows testing after complete assembly and packaging of the SiP.

SiPs are analogous to PCBs in the sense that multiple chips and passives are combined into one substrate. SiPs use passive substrates and various technologies, (Si, SiGe, .13um, .25um, digital, analogue, RF, bare die, flip chip ICs etc.) combined together in a miniature package.

Unlike PCBs the miniature size of SiPs precludes normal testing as the signal connections and the IC pads themselves are miniature and inaccessible, or occupied.

Like ICs before them, the cost of testing a SiP is likely growing more quickly than its manufacturing cost as SiPs evolve into more complex designs. A SiP has the functional complexity of a populated PCB combined with the inability to provide access or test points for internal signals.

Rapid growth in the highly cost conscious consumer and communications (primarily cellular phone) applications, as shown in Figure 1, has magnified this problem.

Classical PCB testing has evolved to improve test time and coverage with the concept of a Test Access Port (TAP), which gives access to signals on the PCB. JTAG is the usual name used for the IEEE 1149.1 [2] standard for Standard TAP and Boundary-Scan (BS) Architecture for test access ports used for testing printed circuit boards using BS. The TAP Fig. 2 is used to assist in fault location and thus enable PCB repair and retest in an efficient manner.
Repair and retest of SiPs is not viable given their assembly and construction methods. Never the less, testing of SiPs in this manner would be useful if it could be carried out in a fast, flexible, and nondestructive way. SiPs are seen as an economic way to reduce the time-to-market by the use of small specific function ICs on miniature substrates rather than the time, cost and effort to build completely integrated ICs known as System-on-Chip (SoC). Rather than the vastly more expensive complete circuit integration of SoC solutions, SiP technology enables the best-of-class, best-cost, or best-mixed technologies in separate ICs to be assembled on one SiP substrate.

Unfortunately, testing a SiP is not the same as testing an IC. SiP testing has the challenges similar to system or PCB level testing combined with the technical challenges of chip testing. An example of the latter is the fine placement of test probes required for SiP testing. The inherent flexibility of SiP level integration means that specific ICs included on a SiP are changeable with a smaller non-recurring engineering (NRE) investment than that of a monolithic solution. This means that SiP testing methods must be flexible as well. The design-for-test of single monolithic ICs is not available in SiPs as SiPs typically don’t use fully custom ICs.

Like PCB testing IC testing has evolved to include boundary scan testing which is included on many chips and built to the JTAG standard for testing IEEE 1149.1. JTAG TAP techniques allow for the testing of ICs on PCBs without the need to individually probe IC pins.

Fig. 3 shows a wireless JTAG Test Access Port (WTAP) that can be used to enable parallel (multi-DUT) non-contact SiP testing. This technique overcomes two major economic and technical challenges of SiP manufacturing that is, testing coverage and throughput. This method is also economic in that it uses standard automatic test equipment (ATE) infrastructure and techniques.

![Figure 3](image)

**Figure 3** Non-contact Probe Card Test for SiPs

2. System-in-Package Testing

The earlier mentioned PCB and IC test issues continue for SiP packaging where a set of VLSI ICs, and discretes are placed on to substrates to create a compact system. SiP assembly includes bare die and flip chip techniques to provide very high levels of system integration in a physically small but low cost package. Additionally, passives can be included as separate parts or even integrated in the SiP substrate. The substrates used in SiPs are evolving along the same path as that of ICs with finer features and greater complexity. Fig. 4 shows two SiP areas, which are a portion of a wafer scale method of producing SiP substrates. The ability to produce large numbers of SiPs simultaneously on a single wafer produces a bottleneck as SiP testing is currently done serially.

The addition of each IC to a SiP substrate has a negative impact on yield. Typically the final packaging is done without the ability to test devices as they are added to the SiP substrate. Even if there is the ability to test devices as they are added to SiPs, it is currently not done because of yield loss due to multiple test probe touchdowns, and the need for multiple probe card designs for each manufacturing step or individual SiP design. One issue shared between SiPs and ICs is that probe testing requires touchdown and scrubbing of IC pads. Scrubbing creates some damage on pads, which affects their ability to be wirebonded to the SiP. Another reason pre-package testing is limited in SiPs is that the number of signals/pads is large if they are individually tested. If IC pads on SiPs were accessible for massively parallel contact probe testing there would be significant yield loss in subsequent wirebonding-manufacturing steps.

![Figure 4](image)

**Figure 4** Wafer Scale SiP substrates, courtesy NXP.

Even without these issues, it is difficult to conceive of how intermediate tests can be done because of the 3D nature and mixed technologies (flip chip, wire bond, surface mount, discrete etc.) used in SiPs. This could technically be done, however it requires a major investment in multiple multi-level custom probe cards, test stations, and test time; all of which would be detrimental to SiP economics.

The growth in SiP design wins is driven by cost and the ability to produce miniature yet advanced products. Using Known Good Dies (KGD) is a way to increase yield in products, however in SiPs it is not always possible or feasible for cost and test time reasons. Thus for economic reasons, SiPs often use untested, partially or only wafer tested dies. This means that there is a guaranteed fall out and a resultant waste built into the SiP manufacturing process as it is currently done.
Because SiPs are normally tested only after packaging, a test coverage gap is created between the starting dies and the final packaged SiP. This gap or test blindness zone can cause problems especially on large volume products, which is the main target of SiP technology.

As a result of this coverage gap, yield improvement is very difficult and the invested assembly and packaging cost is applied to all units even nonfunctional ones, whose condition is only visible at the end of the packaging process. Without partial-assembly-testing there is no opportunity to cull defective devices early in the manufacturing value chain. Yield loss when mounting dies or passives remains invisible without the ability to do test during production. With half of all packaged systems being SiPs, and SiPs only being tested after assembly, there is likely billions of dollars being wasted because of test blindness.

A standard method for testing ICs is defined in the IEEE 1149.1 JTAG standard [2]. This standard defines a Test Access Port (TAP) for creating boundary scan tests on individual ICs or devices under test (DUTs). Many modern chips of various complexities are built with a JTAG interface.

Wireless, non-contact testing [3] can potentially alleviate many of the above SiP testing constraints, allowing for significant improvements in both the economics of SiP manufacturing, and the ability to integrate more test functions with less I/O.

Important feedback during the production process [4,5] can be gained in addition to the basic earlier tests. This feedback relays information regarding any global or local physical faults, and even circuit-level faults, providing the process engineer the ability to respond earlier, leading to improved yield and thus an improvement in the economics of SiP manufacturing. With partial-assembly-testing dies, substrates, passives, and VLSI parts can be tested as they are assembled.

This paper reports the results of a non-contact Probe and corresponding DUT, which integrate active CMOS circuitry and multiple miniature antenna structures to provide wireless JTAG access for the testing of SiPs. The method of non-contact testing and WTAP presented here combines the benefits of non-contact probing with access into otherwise hidden test points in SiPs, and allows testing during SiP assembly. Being fast and low-impact, WTAP SiP testing allows for increased test coverage on a larger population of devices, while maintaining manufacturing throughput. The technology can be used in a massively parallel manner with multiple transceiver probe sets communicating with multiple SiP DUTs using the non-contact method.

3. System Design

The design of the wireless JTAG antenna structures, transceiver circuits, and probe design requires optimizing the trade-offs among several parameters and design criteria.

In this design, several considerations need to be addressed:
- On-chip real estate requirements for antennae and transceiver circuits.
- Sufficient RF coupling range to allow for probe, DUT, or SiP misalignment and prober over-travel.
- Sufficient intelligence in DUT transceiver to allow the testing of bare SiPs (bare except for WTAP).
- Compatibility with standard JTAG test equipment.
- Utilizing a base-line CMOS (not specialized RF) process for cost and multi-source purposes.
- Ensuring that test component (WTAP) has minimal impact on normal SiP device operation or manufacturing yield.

Fig. 3 shows the basic arrangement for a non-contact RF probe in the middle of a traditional probe card. The probe card provides power and I/O access between ATE equipment and the non-contact probe. The probe card also provides contact (probe) power to the SiP or, alternatively, to the DUT/WTAP.

The probe consists of a CMOS device with micro antennas and transceiver circuits. The DUT is also a CMOS IC with micro antennas. The DUT extends the (JTAG) boundary scan and test signals to other chips on the SiP substrate. The antennae and transceiver circuits are incorporated into the DUT with a goal of minimal impact on SiP performance and use minimal real estate. The main advantages of non-contact wafer probing are earlier test and higher reliability, less contact (therefore reduced pad scrub marks), and the ability to add components to the SiP and at the same time allow retest (with scan chain expansion) as components are added. This is achieved with a standard cantilever probe card, with an added support and wireless transceiver IC placed into the probe card center opening.

Each antenna and transceiver circuit is capable of probing one input/output (I/O) site on the DUT. Multiple DUTs are assembled on to the SiP wafer and each DUT (SiP area) contains multiple parallel RF channels emulating the JTAG test signals, Fig. 5.

The DUT transceiver (SiP) circuits are powered from a separate power probe(s), which contacts the DUT or SiP substrate using the hybrid, probe card. Hybrid probe card in this instance refers to a design in which digital data is exchanged thanks to non-contact RF transceivers, and power is provided through standard probe needles from the same probe card assembly.

On the same card, the non-contact WTAP probe is powered from the usual ATE-accessible probe card pins. After test, the DUT transceiver circuits are put into a low power standby mode and do not affect normal SiP
operation. I/O connections to the transceivers are buffered both on the DUT and probe ICs.

Part of the system design effort is to integrate the transceiver circuits and antenna structures into the design flow of the silicon IC.

3.1 Digital design

The JTAG organization has defined a standard (IEEE 1149.1) - giving the test architecture and a set of instructions for testing ICs and enabling boundary scan tests.

The architecture is made of the following elements:
- A set of 4 dedicated test pins: TDI, TDO, TMS, and TCK. These pins are collectively referred to as the TAP (Test Access Port).
- A boundary-scan cell on each device with primary input or output.
- A finite-state machine TAP controller.
- An Instruction Register (IR), holding the current instruction.
- A 32-bit identification register.

The standard JTAG terminals are:
- Test Data In (TDI): serial test data in,
- Test Data Out (TDO): serial test data out,
- Test Mode Select (TMS): input control signal,
- Test Clock (TCK): dedicated test clock, and
- Test Reset (*TRST): optional reset signal.

Our JTAG design includes a separate wireless *TRST signal which is an asynchronous reset to the DUT JTAG interface. This signal is also brought out via bond pads to the SiP substrate for use by other chips.

Extensions to the basic JTAG standard are needed for multi DUT testing. References [6-9] give details on implementations for extending JTAG TAPs for SiPs, PCBs, systems, and remote systems respectively. In this work, augmentations to JTAG are included to enable flexibility and extensibility for SiP applications similar to the above references.

Extensions to the JTAG method with additional serial communications signals for use in multi DUT and control situations have been proposed by others [6,7]. Additional functionality for similar purposes is implemented in this design. An additional transmit (probe to DUT) signal DIRIN is used to provide a direct data path for additional testing. Two receive channels are included: TDO, which is corresponds to the standard JTAG data out and DIROUT, which is used as an extra output channel available on the SiP. The DIROUT channel is also connected to an internal DUT clock (ring oscillator), which is used for parametric testing. The JTAG control registers are used to enable or disable the functions of DIROUT and DIRIN. The DUT includes a JTAG ID code as well as a TAP interface and multiplex logic to enable or disable 8 extra I/O test pins on the DUT. These I/O pins are programmable under JTAG control and can be used to extend scan chains or enable logic for incrementally added SiP components. In summary a total of 15 signals are brought to the SiP by the wireless TAP.

3.2 RF design

Many microfabricated antenna designs have been, and continue to be, researched for various applications such as clocking [10] and data transfer [11]. These designs are generally intended for non-test applications and do not meet the cost, performance and data integrity requirements for applications such as SiP testing. The designs presented here create RF transceivers meeting the cost and performance goals of SiP applications. Specialized RF CMOS technologies and other technologies like SiGe are not used for the stated economic reasons.

Although many designs may be used for transmitting and receiving data wirelessly, many are not suitable in wafer testing applications since they require a large power budget, or utilize large amounts of silicon real estate on the DUT or probe. Additionally, the bit error rate for testing purposes must be extremely low. The non-contact probe card technology presented uses surface antenna structures (Fig. 6) and CMOS transceiver circuits on the probe and DUT.
3.3 Silicon Chip Antennas

As a starting point, an antenna structure was chosen with the following attributes:

- Transceiver (DUT/probe) antenna 120 μm square - comparable to bond pad sizes yet sufficiently large to allow for reasonable probe-to-DUT misalignment.
- Probe-to-DUT distance of 30 μm distance was chosen to allow for probe over-travel and still provide guard banding.
- RF Carrier Frequency 0.5 - 3 GHz. A high enough frequency to allow miniature antennas to be used and coupled and yet a low enough frequency to be built in base-line logic CMOS. 1.5 GHz was chosen as a reasonable target.

A major issue in designing RF circuits and antennas in base-line CMOS is that there exist various “design rules” or design practices, which complicate or perhaps negate RF, design goals. Chemical Mechanical Polishing (CMP) metal is used in VLSI manufacturing is one such practice. Fig. 6 shows an example of the CMP fill metal, “design rule” used in modern VLSI designs. This metal is included in the IC fabrication process to allow each layer to be planarized before the next layer of metal or insulation is added. In fact - CMP is one of the key breakthroughs, which has enabled VLSI to go beyond the previous limit of 3 or so metal layers to 8 or more [12]. The CMP fill metal has an impact on high-speed signals on the IC itself and in particular high-speed RF signals off-chip, for example signals generated or received by the spiral antenna.

The wireless transceiver electronics required on the DUT can have a negative impact on chip real estate if not carefully designed. Matching antenna structures and transceiver circuitry on the probe card enable bi-directional communication with the DUT. When the WTAP DUT is in normal operating mode (non test mode), the transceiver circuits are disconnected from the application circuits and thus have no impact on performance.

Referring again to the hybrid wafer probe system shown in Fig. 3 during testing, the DUT is brought into close proximity (less than 100 μm) with the matching antenna array on a non-contact probe card. ATE is connected to a conventional wafer probe test system. Data signals (I/O) and power from the tester are transferred through the probe card to the DUT via wireless data signals and wired (contact probe) power contacts. The data signals modulate/demodulate a high frequency carrier (1.5 GHz) generated by transceiver circuits, providing a wireless bi-directional data link between the probe and the DUT.

The prober PCB supplies power to the non-contact probe in the standard way through the ATE probe card interface. Power to the DUT is supplied through a minimal number of probe needles from the probe card. SiP power is supplied from the DUT or alternatively directly from probe needles from the probe card. The reverse is also possible; that is DUT power from SiP substrate. In either case, the idea is to minimize the number of actual probe needle locations. Note that in this arrangement none of the SiP ICs require probe needle contact.

A critical task of this work is the design and performance of the microfabricated antennae and transceiver circuits used in the system with a standard prober and applied to testing SiPs and SiP wafers. These transceiver components (DUT and probe) are designed on companion but separate CMOS chips using 0.13-μm technologies. One chip is designed to be the probe while the other acts as the DUT. Optimized antenna design and very low transmission power levels help minimize signal cross talk and IC area.

4. Experimental Results

4.1 RF Simulations

The performance of the antenna structures and transceiver circuits is critical to the operation of the WTAP; and, they have been extensively modeled and simulated. For the antennae, the simulations were performed using a combination of four different simulation software 3D packages. The first two packages, Totem (developed in an academic environment) and AxFDTD use the Finite Difference Time Domain (FDTD) method. The third and fourth packages were Advanced Design System (ADS) and Sonnet, which use Method-of-Moments (MoM) analysis. Simulations on each of the different packages determined the optimum antenna geometry, antenna pitch, antenna size, matching circuits, and antenna termination from a theoretical point of view. The different tools were used to extract and verify (as nearly as possible) different details of the antennas including extracting equivalent lumped elements and coupling coefficients. A discussion of basic antenna design modeling for wireless chip to chip communications can be found in several references [5,10].

4.2 Design of Experiment (DoE): Scaled antennas

While the computer models for the antennas are helpful, they are necessarily incomplete because of the micro environmental details within the ICs. For example, CMP metal is used on sub-micron VLSI chips to allow manufacturability and yield with multi-layer metal chips. It is a key enabler of the production of chips, [12] but creates a major impact in the electromagnetic microenvironment especially when attempting to have wireless communications off-chip. Because fabrication and experimentation of antennas directly in VLSI is expensive and time consuming, a design-of-experiments model of the antenna environment on-chip was
conceived to answer unknowns with respect to antenna microenvironments. Several scaled antenna environments were produced at a size of 200 times the equivalent linear chip scale. These were fabricated using standard electronics materials. These results allowed a quick test of the microenvironment issues for the eventual silicon design.

Theoretically, antennas scale over all sizes and wavelengths. That is, size is directly proportional to wavelength, therefore antenna length, inductance and capacitance scale directly with linear size.

The various antenna environments are listed as follows:
- GP = Ground Plane under antenna
- CMP = CMP metal fill pattern around & under antenna
- RING = Metal guard ring around antenna
- PARA = Parasitic antenna under the top antenna.
- 2x = Double layer (stacked) windings on antenna
- 1x = Single layer windings on antenna
- 8um = minimal gap antenna coupling

4.3 Scaled antenna experimental test results
The scaled antenna test was setup as follows:

A Signal generator (HP 8702B) was wired to an RF Coupler (Mini Circuits ZEDC-10-2B) and connected to provide constant transmit power; the forward path of the coupler was connected to the ‘transmit’ antenna of the scaled test pair; and, at the ‘receive’ antenna, an oscilloscope was used to measure the coupling of the antenna pairs.

Fig. 7 shows a representative set of experimental results (coupling voltage versus frequency) with various scaled antenna environments. In Fig. 7, one can see that the CMP appears to have improved coupling over that of a bare antenna (1X), while a ground plane (GP) has a definite negative impact. The design challenge is to pick an antenna structure that can give high coupling and wide bandwidth and yet not be too high in operating frequency, which is limited in CMOS.

Our conclusion from the DoE was that the design frequency of 1.5 GHz could be obtained with consideration of the microenvironment. CMP does not seem to have a major impact however. Conducting structures should not be placed (if possible) directly within the antenna area.

4.4 Transceiver Design
Earlier simulations included AM, FM and direct digital modulation techniques [5]. Because the modest system requirements for this implementation of JTAG (10 M-baud throughput), Amplitude Modulation (AM) was chosen for its low design risk and simplicity of implementation. The transceiver circuits used for data transfer were designed and simulated with standard commercial VLSI Computer Aided Design (CAD) tools.

For simplicity the receive chain utilized a low noise amplifier (LNA) without frequency tuning. This gives a low power and chip real estate budget, and at the same time avoids the need for tuned elements, which would have deleterious frequency dependences when coupled to different antennas.

Since the transmission range is small, but constrained by the use of a relatively low frequency CMOS technology, careful designs of the transmitter and receiver are required. An envelope detector was used for demodulation. This circuit was designed with a minimal number of components to save area.

One area of particular attention is the susceptibility to noise in a test environment. The high carrier frequency versus the relatively modest data rate goes a long way to mitigating against noise. A guard ring placed away from the antenna was included, and careful consideration of CMP design rules (metal fill) and an N-well barrier was placed around the transceiver in the physical layout. This was done to reduce the susceptibility to interference caused by noise and to reduce coupling to the rest of the circuit. The area occupied by the transceivers using the AM technique is on the order of the antennas themselves.

The transceivers were designed with a base-line 0.13 um CMOS process of a major semiconductor foundry and industry standard CMOS CAD simulation tools as follows:
- Number of metal layers: 8 available, 8 used
An IC was fabricated and is shown in Fig. 8. This figure shows both the DUT (Left) and the probe (Right) as well as antennas (TOP). Here the probe IC is wire bonded (lower right) to a ceramic board, which is part of the non-contact probe shown at the center of the probe card in Fig. 10.

![Figure 8](image)

**Figure 8** Non-contact DUT (l), probe (r), antennae (t) in 130 nm technology mounted on ceramic probe interface board.

### 4.5 Transceiver Transmitter Results

After fabrication, the DUT/probe ICs were tested for functioning RF transmit signals on a standard probe station. A custom RF (non-contact) probe was designed and placed proximally central to the DUT/probe antennas to show operation of 5 independent transmit path signals, TDI, TCK, TMS, DIRIN, *TRST. An RF spectrum analyzer was used with the custom probe to observe the independent RF carriers.

Fig. 9 shows the results of one such test and demonstrates the independent (parallel) nature of the transmitting signals. The testing showed 100% yield of the devices tested (14), indicating that the fabrication of the basic RF transmit carrier was successful. Each RF signal is controlled by its own Voltage Controlled Oscillator (VCO) and further by its own data path. The carrier frequency measured was 1.48 GHz with a spread of less than 100 MHz. This is completely adequate with respect to narrow frequency required by the tuning effect of coupling antennas mentioned earlier. These parallel RF signals between the probe and DUT (SiP) become virtual wires for the JTAG signals, thus providing a wireless TAP. These 5 "transmit" signals are used for the JTAG probe signals and on the DUT there are 5 corresponding receivers.

![Figure 9](image)

**Figure 9** Five independent transceiver transmitter (channels), Measurements.

### 4.6 Probe physical design

Fig. 10 shows the final hybrid non-contact probe card. The non-contact probe is placed in the center opening of a standard probe card. Standard probe needles, seen on the periphery of the non-contact probe card, provide power to the SiP non-contact DUT.

The non-contact probe shown in the center of Fig. 10 consists of 5 elements:

1) Probe transceiver IC.
2) Ceramic transition hybrid.
3) PCB with ribbon connector to probe PCB
4) Back mounting post.
5) Non-contact probe mount (fits within topside probe card PCB ring).

![Figure 10](image)

**Figure 10** Probe card showing cantilever power probes (outer) and non-contact transceiver probe (center).

All of these must fit into the throat of the opening of an unmodified probe card. Bench testing was carried out on a standard prober. Face to face error rate testing was carried out on a custom xyz probe holder. SiP production testing was carried out on an Electroglass 4090u prober with an Agilent 93k tester on the production floor of NXP’s production facility in Caen, France.

Electrical parametric tests can detect defects other than functional faults. For example, Iddq tests can detect some resistive faults that are not severe enough to cause
a logical fault in digital circuits. Some tests can be used to detect elevated quiescent current above normal [13-15]. A standard element in testing is a ring oscillator, which can be used to find basic gate delays as well as yield issues. A long chain ring oscillator was included in the WTAP DUT to allow process parameters to be observed both by the wireless interface (ring oscillator frequency) as well as ATE (Iddq) connected to the prober.

With the hybrid design, the DUT can be placed in various modes and the SiP can be tested for Iddq as it is assembled. Any out-of-spec part can then be noted for rejection, or a manufacturing step can be flagged for repair and thus avoid additional investment in component placement or final packaging.

5 Error Rate Testing

Error rate tests were performed to test the integrity of the system. These tests evaluate the raw error rate under ideal and non-ideal DUT probe placement conditions and evaluate the range of mechanical offsets possible.

On the transmit (digital input) probe side, a test pattern was generated with a Tektronix CSA 907T test set. The DUT ‘receive’ signal (digital output), was connected to a companion Tektronix CSA907R receiver. The clock rate was set to 20 MHz on the test units to match the design goal of 10 Mbaud data rate. The pseudorandom bit pattern was selected on the transmitter, and the receive test set was set to observe the same pattern. The receiver level settled on 0.4 volts. This low voltage is due to 50-ohm termination of the test set loading the CMOS DUT output. The low power CMOS logic output of the DUT normally would not see 50 ohms and thus loaded the output to a lower voltage level.

Figure 11 is a side view of the probe over a DUT mounted on a SiP substrate. In this view there is a 30um gap between DUT and non-contact probe.

Figure 11 Non-contact probe and WTAP/DUT on SiP substrate.

Fig. 12 shows error rate versus vertical and lateral probe to DUT alignment offsets. The figure shows a set of error rate (<10⁻⁹) contours. Within the contour, the error rate is essentially zero and outside, the error rate rapidly increases to 100%.

The +z direction is that of greater separation (height) between probe and DUT. The other directions x and y are horizontal offsets between the DUT and probe antennae. Zero on the x or y axis is where DUT and probe antennas are aligned. The +x (zx) contour is an increase (more silicon overlap) between the DUT and probe ICs, see Fig. 11. The –x (zx) contour shows a decrease (less silicon overlap) between the DUT and probe ICs. The +/-y (zy) contour is a lateral shifting of the antennas (constant silicon overlap). In Fig. 12 shows that for good data integrity the required probe location is approximately +/-50um in the x or y direction, and 0 to 45um in the z direction.

These distances are well within the tolerances of modern prober equipment. To mount the floating probe, a miniature XYZ translation stage was designed to facilitate testing and provide the independence between probe needle location and floating probe. In production, the xyz offsets are fixed in a test station and not modified. The offsets are set to bring the floating probe within the zone of high data integrity, and at the same time allow for prober over-travel (overdrive) to occur without touchdown damaging the floating probe head.

When using contact probe cards, if one data pin does not contact properly, the probe card must be lifted off and another touchdown attempted. When using a hybrid probe card, the inherent redundancy of the power and ground pins means that if one pin does not make proper contact, there is less need to lift off and touch down again. Since the data path is completely wireless data integrity does not depend on touchdown success. Power-only contact is relatively easily done with SiP designs, as the periphery of a SiP is much longer than that of an IC providing multiple power contact possibilities.
6.  Discussion of results
In this wireless design a total of 15 test signals (5 JTAG, 2 Communications, and 8 I/O) were added to the SiP without requiring a single (data) contact probe needle. This means that scrub damage to pads (and debris) is reduced by a large measure and at the same time multiple partial-assembly-test(s) are enabled.

The data integrity results meet expectations as the error rate is shown to be very low <10^{-10}. The data rate of 10 Mbits/second was achieved by the transceiver design meeting the design specification. The goal of a 30um standoff distance (~1 mil) was exceeded by the system, allowing an even wider acceptable variation in DUT, probe, or SiP locations. The wide mechanical tolerances shown by the transceivers enable implementation of a multi-DUT probe card which confirms the high throughput potential of this system. One can envision a massively parallel multi-DUT system for simultaneous wafer level SiP testing.

The choice of standard CMOS as technology platform has not been a limiting factor in the communications and thus can enable low cost use.

Given the large standoff distance it is likely that much higher data rates are possible using a modified transceiver design. The current IC used rate-limited I/O cells in the CMOS design and therefore testing above 20 MHz was not attempted.

7.  Future Work
This work shows that non-contact SiP testing is practical and addresses key test cost bottlenecks in SiP manufacturing. This technique can be used at multiple points along the assembly of SiP devices. This technique could find applications in many fields including SiP assembly test, and could even be included in SoC designs to provide non-contact testing capability. Because of the non-contact and compact nature of this approach, massively parallel wafer scale testing is made practical.

A generic non-contact interface for SiP testing of various designs could be implemented using the technique shown here. Such a design could be implemented as a standard IC, which would be added to all SiP designs to provide a consistent test access portal. A potential universal and standardized non-contact Test Access Port could be envisioned for SiP, SoC, PCB, and even packaged devices.

7.1 Scaling of Designs
The transceiver sizes presented are quite small and could be placed under pads for a more compact design. However, the design soon becomes I/O pad limited and there is little reason for further logic optimization. As the circuits are migrated to smaller process nodes (0.13, 0.9 and 0.065 um) [16], the transceiver and antenna sizes will continue to shrink, pitches will decrease, and operating frequencies will increase, as shown in Table 1. Parallel data paths are enabled by smaller sizes leading to higher speed testing. One limit is the basic cutoff frequency (fT) of the chosen technology. For the current design, a conservative fT of digital CMOS was assumed. At the present time, it is not clear what limits or advantages VLSI scaling will bring to the RF aspect of this technique.

<table>
<thead>
<tr>
<th>Process (nm)</th>
<th>Pitch (um)</th>
<th>fT (GHz)</th>
<th>Area Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>90</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>130</td>
<td>65</td>
<td>60</td>
<td>0.5</td>
</tr>
<tr>
<td>90</td>
<td>45</td>
<td>100</td>
<td>0.25</td>
</tr>
<tr>
<td>65</td>
<td>35</td>
<td>150</td>
<td>0.13</td>
</tr>
</tbody>
</table>

Transceivers will have an even smaller real estate cost on scaled ICs. It is possible to envision that wireless test circuits be included in ICs designed for SiPs as an IP block. The transceivers could then be connected to external antennas designed on the SiP substrate. This would enable cost reduction and add flexibility by decoupling the transceivers and the antenna locations on the SiP.

7.2 Other future work
Because of the reduced pin count enabled by the WTAP (zero data probe pins used), and the small footprint of both the test head and the DUT, a logical next step is to design multi-headed SiP WTAP test cards. This can bring large economies to test by allowing massively parallel SiP testing and is easily implemented given the wide 3D location tolerance shown in this work.

We will continue to develop more efficient transceivers by optimizing CMOS designs. Various modulation techniques or data compression can be used to save RF and DC power on both DUT and probe. Although restricted by CMOS process design rules, antennae of differing designs can be envisioned.

Previous work shows that a completely non-contact technique [5] is feasible for modest power budgets. The design of SiP coupled wireless power generation will be investigated

An obvious enhancement would be a die shrink by overloading communications (modulation), or digital techniques (data compression) into smaller real estate. I/O speed enhancement by compression or more sophisticated forms of Boundary Scan or digitally combining JTAG signals into serial RF streams (BIST) appears feasible. Reduced Pin count JTAG [17] is a distinct possibility both on the RF and the DUT side.
It is worthwhile to investigate techniques for isolating transceivers from on-chip application circuits to decrease impact of substrate noise and allow even greater standoff distance between DUT and probe. This may enable wireless packaged IC testing or packaged SiP testing using the same wireless techniques.

Ref. [6] describes an approach expanding on the 1149.1 standard to create a multi-DUT TAPs for SiP architectures (SiP-TAP). This work extends the concept of TAP into a wireless TAP, WTAP and can be used to extend SiP TAP to multi-DUT SiP WTAP implementations.

8. Conclusions

We have shown a non-contact technique that can be used to replace classical contact probing to enable JTAG testing of SiP substrates and devices.

The relaxed alignment requirements for this technique enable massively parallel testing of wafer-scale SiP devices and thus remove a key economic barrier to SiP manufacturing.

As evident from the test results, the signals can be sent between DUT and probe with a high level of reliability for JTAG functions. The results prove the feasibility of a very low cost (fully CMOS) design.

A novel and effective approach to SiP module or SiP wafer-level testing of integrated circuits is presented. This technology uses standard ATE, JTAG, and probing equipment. It can be used to allow selected testing during assembly of simple or complex SiP systems. Also demonstrated is that the floating-head RF transceiver placement location with respect to the SiP DUT is within that of standard prober/probe tolerances making this technology practical from a production point of view.

With utilization of this technology the 3D nature of SiP systems does not become a limiting factor, as it is when using other testing methods. The RF transceiver technology is shown to be robust and can be used and extended with not only JTAG extensions but also BIST on SiP devices as well. Antennae and transceiver circuits are designed to address practical VLSI design and production issues and permit non-contact testing of ICs on SiP wafers using hybrid non-contact probes.

This work shows that a standard wireless interface can be achieved for SiPs, as well as potential applications in SoC or even packaged devices.

High throughput massively parallel testing with good test coverage on SiPs is enabled by this approach.

9. References