Burst Mode Data Recovery Circuit

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ABSTRACT
Burst mode is a data transmission mode in which data is sent faster than normal transmission modes. In this project, a burst mode data recovery circuit is designed which utilizes a phase locked loop and delay locked loop. The phase locked loop provides clock signals with four different phases. The delay locked loop provides the recovered data using the 4x oversampling technique. The 4x oversampling technique samples the input data into four samples with respect to the four clock signals. The sampler and synchronizer circuit is designed using single edge triggered flip-flop, conventional double edge triggered flip-flop and transmission gate based double edge triggered flip-flop. They are compared for power consumption. The sampler and synchronizer circuit using transmission gate double edge triggered flip-flop reduces the power consumption of data recovery circuit. The burst mode data recovery circuit is implemented in 180nm technology using Cadence Virtuoso Software.

Keywords *– Burst Mode, Data Recovery Circuits, Delay Locked Loop, Flip-flops, Oversampling Technique*

I. INTRODUCTION

Burst mode is a high speed data transmission mode used to facilitate sequential data transfer at maximum throughout. Burst mode data recovery circuit can be designed using phase locked loop and delay locked loop. An oversampling technique is incorporated with the delay locked loop to recover the data signal. Therefore the data recovery circuit can recover the data in a short acquisition time and can enhance jitter tolerance. The Fig.1 shows the basic block diagram for the burst mode data recovery circuit. The quadrature voltage controlled oscillator of the phase locked loop provide clock signals with four different phases such as 0^0, 90^0, 180^0 and 270^0 according to the reference frequency. The 4x over sampler uses these four clock signals to sample the data signal which is delayed by the delay locked loop. The decision circuit chooses the recovered data from the samples provided by the sampler and synchronizer.

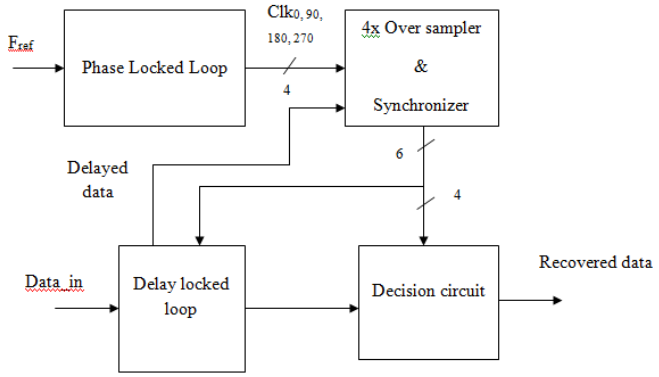

Fig.1 Basic block diagram of burst mode data recovery circuit

Nowadays, low power consumption is of major concern in designing the circuits. The sampler circuit is a D flip-flop array. The oversampling circuit is realized for various flip-flops such as single edge triggered flip-flop, conventional double edge triggered flip-flop and transmission gate based double edge triggered flip-flop and are compared for their power consumption. Since transmission gate double edge triggered flip-flop has lower power consumption, it is used for designing the sampler and synchronizer circuit. The transmission gate based flip-flop has less area consumption compared to the other two since the transistor count is low. The data recovery circuit is designed using this low power sampler and synchronizer circuit; hence it further reduces the power consumption of the whole circuit.

II. BLOCK DIAGRAM

Based on the concept of multiple sampling phases to oversample each data bit, we adopt the 4× oversampling data recovery architecture using a DLL for phase tracking. To decrease system complexity and design bottleneck of VCDL, combining the 4× oversampling technique with DLL not only can recovery in rapid time but also decrease the tuning range of VCDL. The Fig.2[1] shows the block diagram of proposed burst mode data recovery circuit. The PLL provides the multiphase sampling clocks, and the DLL in the oversampling CDR circuit tracks input signals for phase

aligning. There are two modes for data recovery: 1) the phase-picking mode and 2) the phase-aligning mode. When the data recovery circuit receives a burst-mode data stream, the burst mode data recovery circuit operates in the phase-picking mode at first. Employing the VCDL as a post amplifier, the input data stream is sampled as four results by the 4x oversampling circuit. Following the oversampling circuit, a synchronizer is composed by a D flip-flop (DFF) array to generate and synchronize the sampling patterns. By detecting these synchronized sampling results with phase detectors (PDs), one of lead or lag signals can be determined as the data transition detection. In summary, four detected sets are generated. In this period, the phase-picking controller (PPC) determines the phase detection results through a voting regime. The voting operation requires only four to seven clock cycles before the burst mode data recovery circuit enters into the phase-aligning mode. In phase-picking mode, the charge pump (CP) input LEAD_CP and LAG_CP are disabled to keep the control voltage generated by the loop filter at the same level. Therefore, the feedback loop would not operate in this mode.

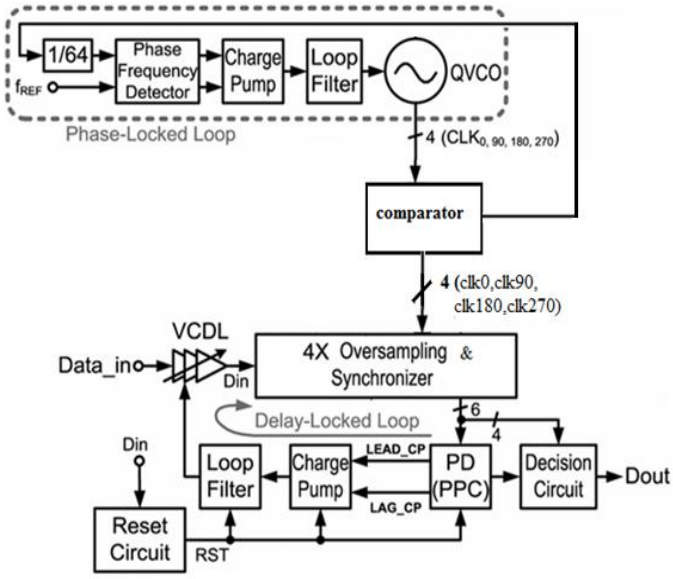

Fig.2 Block diagram of proposed burst mode data recovery circuit

After the phase-picking mode has decided the selected clock for aligning and retiming, the data recovery circuit enters into the phase-aligning mode. The DLL is composed of a VCDL, a 4x sampler, a synchronizer, a CP, a loop filter, and a PD. In the phase-aligning mode, the VCDL not only provides the voltage gain to amplify input signal but also controls the delay time of input data for aligning. The delayed data are sampled and synchronized by a 4x sampler circuit and a synchronizer.

The PD outputs the phase comparison with the CP for controlling the control voltage generated by the loop filter. The control voltage adjusts the phase of input data through the VCDL, and the retimed phase of delayed data can be aligned to the selected clock to achieve the biggest retimed margin. Finally, the decision circuit selects one of the synchronized sampling patterns sampled by the retiming clock as the Dout. For circuit measurement, the reset circuit is composed to detect the data status and enables the CDR regime through the reset signal (RST).When the data stream enters, the reset circuit is triggered by the input positive transition and generates the signal RST to enable the data recovery operation. In the beginning, the periodical preamble signal is detected with the sampling clocks and processed with the synchronizer to synchronously output six sampled data in parallel with four *T*CLK.

A. Sampler and Synchronizer and Decision Circuit

In Fig.3 [1], the sampler is composed by a DFF array with four-phase sampling, and the synchronizer uses 10 DFFs to parallelize the six sampled outputs. The longest signal path is four DFFs in serial. Since the retimed data synchronizing to the clocks are generated by the PLL, the outputs of synchronizer are independent of input data jitter.

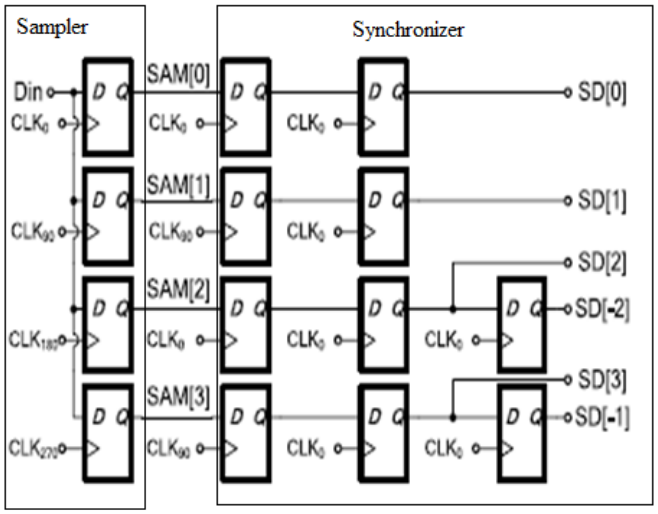

Fig.3 Sampler and synchronizer.

The outputs of synchronizer, SD[0]-SD[3], also be the input of the decision circuit, and one of these pattern is selected as the recovery data. The transmission gate based DFFs are used for realizing the circuit. Although the oscillator's output is stabilized, it is not enough to sample demodulated bit stream accurately due to its frequency error and synchronization problem. To remedy these problems, an oversampling synchronizer is utilized.

B. PHASE DETECTOR

The Fig.4[1] shows the PD scheme with the PPC to generate lead and lag signals for DLL. Following sampler and synchronizer, the sampled data are grouped into four patterns for phase determination.

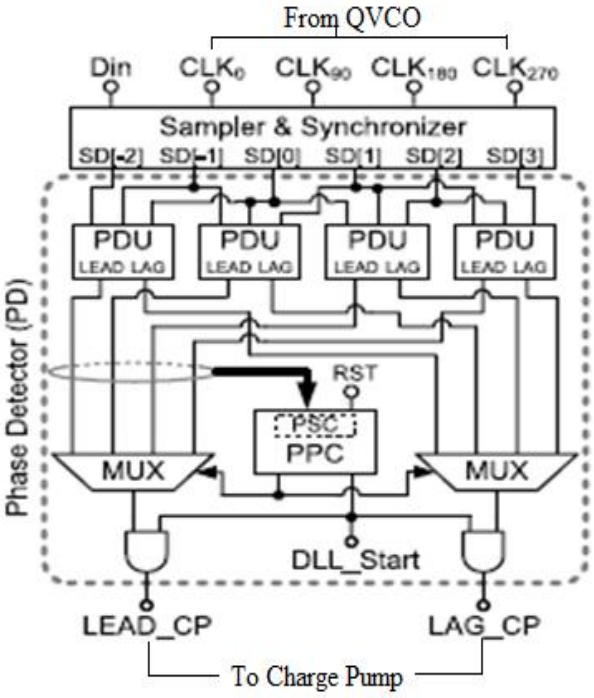

Fig.4 Phase detection scheme for phase picking

We use four phase determination units (PDUs) to determine the transition of Din. Using three data samples, SD[n-2], SD[n-1] and SD[n], through three consecutive clock edges, the PDU can determine whether a data transition is present and whether the clock leads or lags the data. For the absence of data transitions, all three samples are equal and no action is taken. The phase picking controller(PPC) can detect the transition location immediately using four PDU lead signals, LEADs.

III. RESULTS AND COMPARISON

The circuits are designed in 180nm technology. The schematics of the circuits were drawn in cadence virtuoso software and also simulated. The data recovery circuit provides the recovered data as the output. The phase locked loop produces the clock signals with four different phases and is given to the sampler and synchronizer circuit to produces the samples with respect to these clock signals.

The Fig.5 shows the simulation result of the clock and data recovery circuit with sampler and synchronizer designed using transmission gate based double edge triggered flip-flop. Here the input signal starts with a high to low transition. The reset signal turns low at the first positive edge of the data signal. The delayed data signal is obtained according to the control signal Vc obtained from the loop filter. The sampler and synchronizer samples the data signal with respect to the clock signals provided from the phase locked loop. The phase detector provides the lead and lag signals. Out of the four samples the decision circuit provides the correct data output.

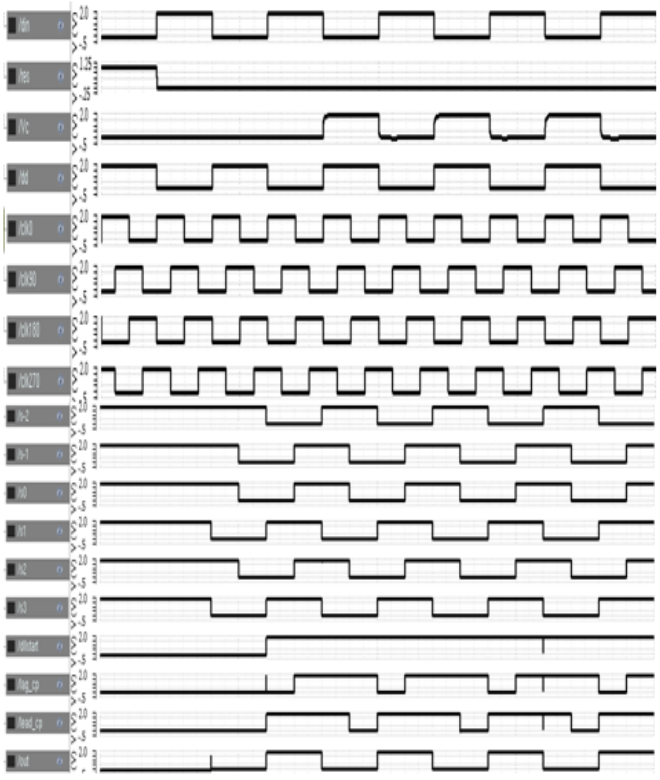

Fig.5 Output of data recovery circuit

The power consumption of the data recovery circuit is measured with sampler and synchronizer designed using single edge, double edge and transmission gate based flip-flop.

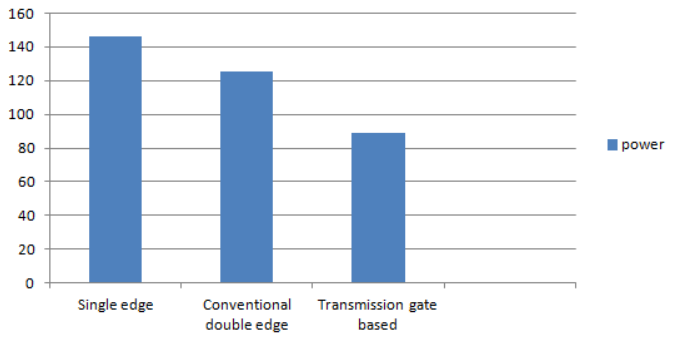

Fig.6 Power comparison (mw) of data recovery circuit

The Fig.6 shows the power comparison of data recovery circuit. From the chart it is very clear that the data recovery circuit with transmission gate based sampler and synchronizer has lower consumption compared to conventional double edge and single edge triggered flip-flop

IV. CONCLUSION

The burst mode data recovery circuit which utilizes a 4x oversampling technique is designed. The phase locked loop provides the clock signals for sampling the data signals. The delay locked loop along with the oversampling technique recovers the data signal. The sampler and synchronizer was designed using three different flip-flops such as single edge triggered, conventional double edge triggered and transmission gate based double edge triggered flip-flops and their power consumption is compared. Out of these, sampler and synchronizer designed using transmission gate based flip-flop has lower power consumption and area. Therefore the sampler and synchronizer in the proposed recovery circuit have low power consumption. Hence the power consumption of the recovery circuit also reduces. The circuit is implemented in CMOS 180nm technology. The burst mode data recovery circuit can be used in passive optical networks for upstream data transmission. In the future scope, the oversampling range of the sampler can be increased so as to obtain more samples of the data signal which can reduce the noise signal. More efficient flip-flops can be used to further reduce the power and area consumption.

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