

# What's the Matter with Kansas Lava?

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- Test circuit behavior.
- Generate documentation.
- Sanity check code generation.

```
data Seq a = Seq (Stream a) AST
```

Do the two embeddings do the same thing?

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prop_HAComm x y = (halfAdder x y) == (halfAdder y x)
  where types = (x :: Comb Bool, y :: Comb Bool)
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- No observable intermediate values.
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```
instance Eq a => Eq (Comb a) where
  (Comb x _) == (Comb y _) = lhs == rhs
  where lhs = (unX x :: Maybe a)
        rhs = (unX y :: Maybe a)
```

```
instance Eq a => Eq (Seq a) where
  (Seq x _) == (Seq y _) = error "undefined"
```

# Observing Intermediate Values

```
fullAdder a b cin = (sum,cout)
  where (s1,c1) = halfAdder a a
        (sum,c2) = halfAdder cin s1
        cout = xor2 c1 c2
```

# Observing Intermediate Values

```
fullAdder a b cin = ((sum,cout),debug)
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- This changes the circuit interface, requiring all users of the `fullAdder` to change how they call it.
- It's also incredibly time consuming and error-prone.

```
class Probe a where  
  probe :: String -> a -> a
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```
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  where (s1,c1) = (probe "ha1" halfAdder) a a  
        (sum,c2) = halfAdder cin s1  
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```

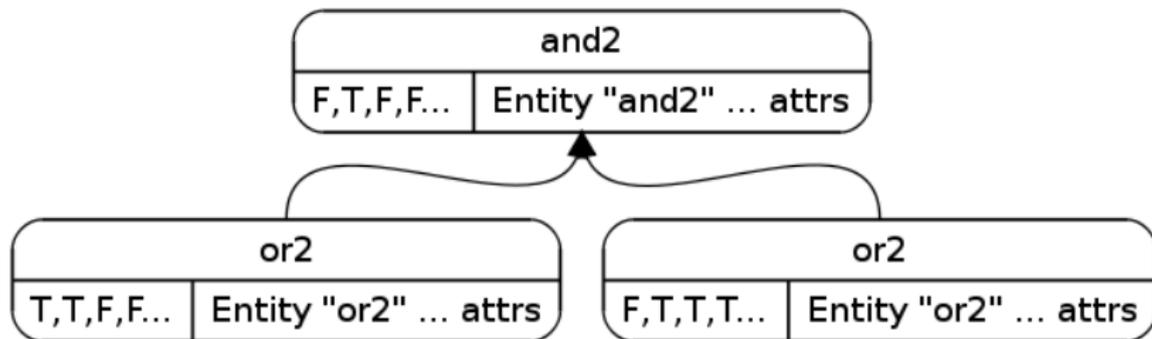
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```

```
> test $ fullAdder false true false  
ha1_0: "F" :~ "F" :~ "F" :~ "F" :~ ...  
ha1_1: "F" :~ "F" :~ "F" :~ "F" :~ ...  
ha1_2: "(F,F)" :~ "(F,F)" :~ "(F,F)" :~ "(F,F)" :~...
```

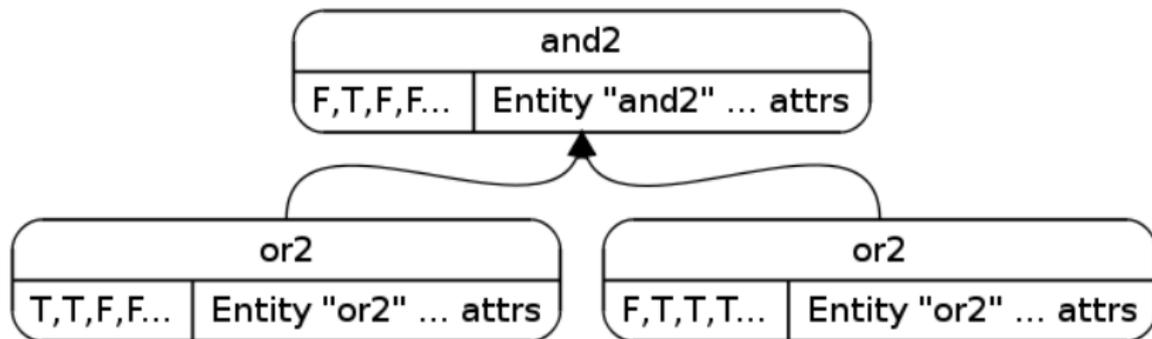
# Probe Implementation

```
and2 :: (Signal sig) => sig Bool -> sig Bool -> sig Bool
and2 = liftSig2 (\ (Comb a ae) (Comb b be) ->
                 Comb (a && b)
                 (Entity "and2" [ae,be]))
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and2 = liftSig2 (\ (Comb a ae) (Comb b be) ->
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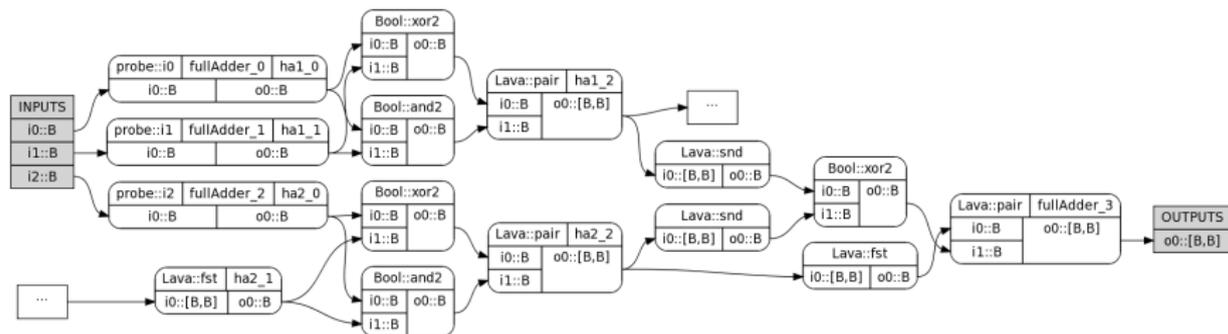
# Putting Probes to Work

```
fullAdder a b cin = (sum,cout)
  where (s1,c1) = (probe "ha1" halfAdder) a b
        (sum,c2) = halfAdder cin s1
        cout = xor2 c1 c2
```

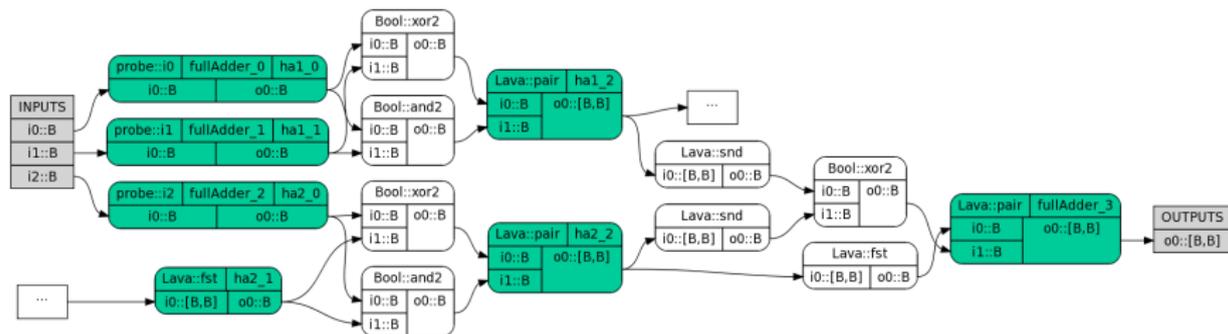


```
halfAdder :: Seq Bool → Seq Bool → (Seq Bool, Seq Bool)
```

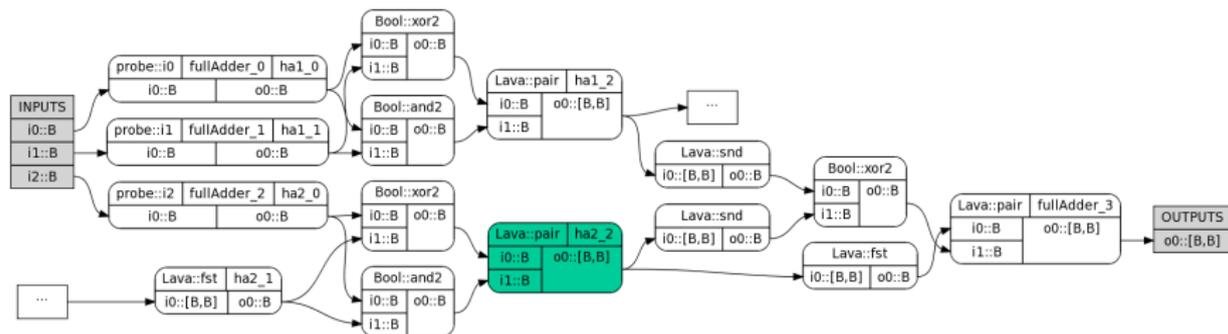
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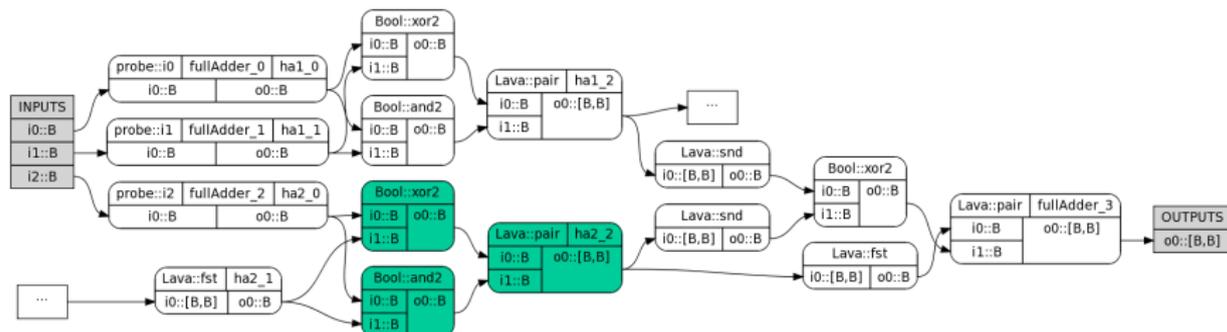


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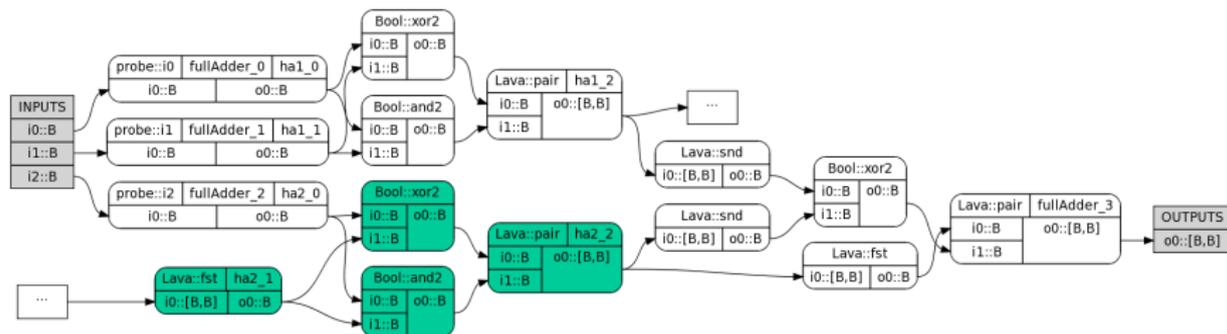




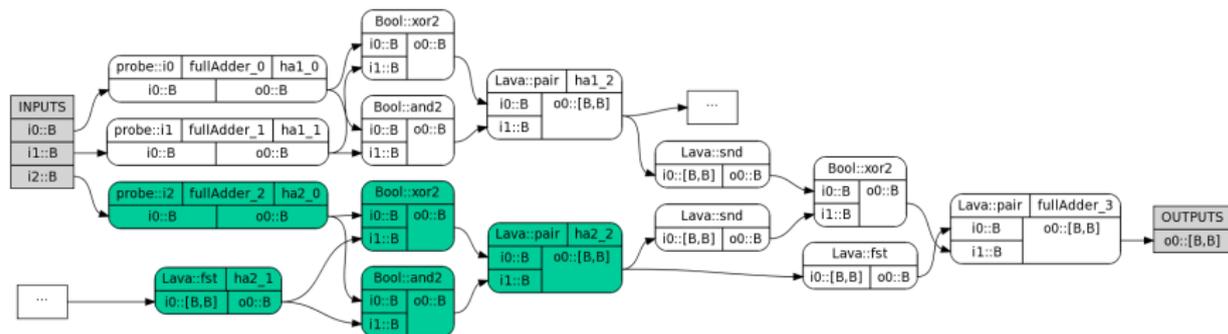
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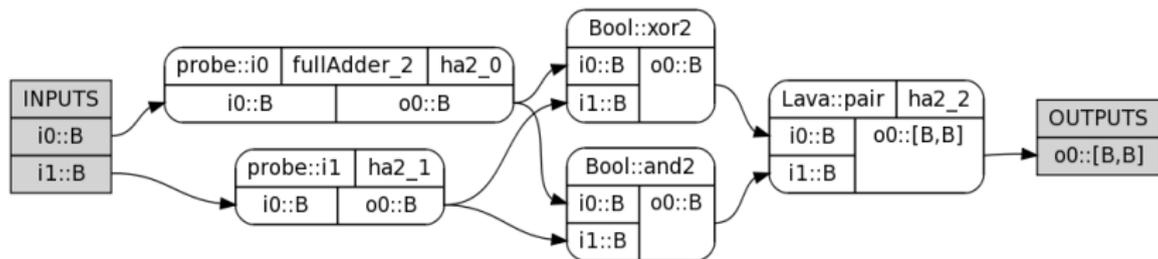
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Using the probe data and the extracted subcircuit, we can generate a testbench in VHDL and run it with modelsim:

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```
ha2.shallow
```

```
0000  
1110  
0101  
0000  
1001  
0101  
0101  
...
```

# Testbench

Using the probe data and the extracted subcircuit, we can generate a testbench in VHDL and run it with modelsim:

## ha2.shallow

```
0000
1110
0101
0000
1001
0101
0101
...
```

## ha2.info

```
(0) F/0 -> F/0 -> (F,F)/00
(1) T/1 -> T/1 -> (F,T)/10
(2) F/0 -> T/1 -> (T,F)/01
(3) F/0 -> F/0 -> (F,F)/00
(4) T/1 -> F/0 -> (T,F)/01
(5) F/0 -> T/1 -> (T,F)/01
(6) F/0 -> T/1 -> (T,F)/01
...
```



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- Kansas Lava allows the importation of existing VHDL blocks. We could use this system in reverse to check the shallow embedding.
- A semi-automated algorithmic debugger.
- Testing optimizations.
- A dataflow visualizer.

# Questions?