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High-Speed VCSEL-Based Transceiver for 200 GbE Short-Reach Intra-Datacenter Optical Interconnects

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Abstract: The soaring demand for higher speeds in datacenters to address the relentless growth of the global IP traffic places optical interconnects in the spotlight. In this manuscript, we present a high-speed optical transceiver for intra-datacenter connectivity. The transceiver is based on single-mode, single-polarization high-speed vertical-cavity surface-emitting lasers (VCSELs), a VCSEL driver chip, and a linear receiver. Following a step-by-step approach, we present the architectures, assembly processes, and experimental results from the different modules. More specifically, we demonstrate (1) a data transmission experiment at 80 Gb/s using PAM-4 (four-level Pulse Amplitude Modulation) modulation for a reach of up to 500 m by employing a single-mode VCSEL module, and (2) a full-link experiment proving up to 64 Gb/s per lane capacity using PAM-4 signaling of the VCSEL-based optical transceiver test vehicles in back-to-back configuration and up to 56 Gb/s for 500 m and 2 km transmission distances. The acquired experimental results verify the suitability of the optical transceiver for intra-datacenter interconnects' applications.

Keywords: short-reach optical interconnects; intra-datacenter connectivity; VCSEL-based transmitter; VCSEL; linear receiver; high-speed optical transceiver; 200 GbE applications

1. Introduction

Rapidly expanding new technologies, video services, artificial intelligence [1], and cloud applications have caused a relentless growth in IP traffic. Predictions indicate that by the end of 2021, the annual global datacenter IP traffic will exceed 20.5 ZB, a threefold increase from 2016 [2]. Moreover, the nature of these applications and the intrinsic characteristics of networks mean that an enormous proportion of this traffic stays within the datacenter, accounting for 71.5% of the total. In such a challenging landscape, operators struggle to keep pace with the increasing demand for speed, cost, and energy efficiency [3,4].

Optical interconnects are in the spotlight as an enabling technology that will accommodate the leap forward to the next decade. While shipments of 100 GbE devices are growing exponentially and will continue to proliferate until 2023 [5,6], replacing the respective 40 GbE in datacenters, the next upgrade step is nearby [7]. For this reason, different techniques (space division multiplexing,

polarization multiplexing, advanced modulation formats) and technologies (modulator-based transmitters, vertical-cavity surface-emitting laser (VCSEL)-based transmitters) are used to meet these requirements for intra-datacenter connectivity. Augmenting the number of parallel optical lanes offers a straightforward path towards scaling the link capacity but lacks in power efficiency and footprint [8]. Polarization multiplexing as a means of generating four-level signals in the optical domain was shown to achieve a 28 Gb/s transmission rate [9]. A four-channel compact and a low power transmitter module were reported in [10] to exhibit a limited bitrate of 25 Gb/s per lane. An eight-channel hybrid transmitter based on InP lasers, SiP modulators, and parallel single-mode fibers was shown in [11] to reach 56 Gb/s per lane. In [12], the hybrid integration of electronics and SiP integrated circuits resulted in the realization of a 56 Gb/s transceiver for a transmission distance of up to 2.2 km. Scaling the bitrate of each optical lane has also been demonstrated using discrete multitone formatting and complex digital signal processing [13].

Especially in the field of short-reach optical interconnects, vertical-cavity surface-emitting lasers (VCSELs) over multimode fiber (MMF) links are a dominant technology in the market since they have several beneficial characteristics, namely, low manufacturing and packaging costs, small footprint, low power consumption, high reliability, and high bandwidth density [14,15]. Several attempts have been made to use VCSEL-based transmitters that operate at 850 nm in combination with MMF to achieve bitrates of up to 60 Gb/s [16–22]. High-speed transmitters of up to 71 Gb/s were demonstrated but with a small bit-rate-distance product [23,24]. Single-mode VCSELs reduce the effect of modal and chromatic dispersion in the link and, as a result, extend the reach capability of the transmitter. Besides, datacenter operators have already started to replace multimode fibers with single-mode fibers in their datacenter environments, shifting from parallel optics to WDM (Wavelength-Division Multiplexing) solutions. The driving force for this trend is the continuous requirement to upgrade the type of installed multimode fibers to support higher bandwidth and longer reach as the datacenter grows in both size and traffic. Facebook is a prominent example that has come up with using low-cost single-mode fibers for short distances in the datacenter environment, a trend supported by other hyper-scale datacenter operators like Microsoft and Amazon [25]. Data rates of 30 Gb/s at 1270 nm and 40 Gb/s at 1525 nm were reported to obviate the need for equalization [26,27]. Using the transmitter- and receiver-side equalization, a 56 Gb/s C-band VCSEL was showcased to have the ability to transmit only NRZ (Non-Return-to-Zero) signals [28]. A 56 Gb/s driver-integrated circuit for VCSEL transmitters with on-chip equalization functionalities was reported in [29]. Although the device exploited more advanced modulation formats and thus augmented the overall capacity, it does not constitute a complete transceiver solution.

In this paper, we present a high-speed VCSEL-based optical transceiver tailored for intra-datacenter connectivity. We describe the architectures and assembly processes of all the modules that comprise the optical transceiver, namely (1) high-speed single-mode VCSELs, (2) the high-speed VCSEL driver, and (3) the linear receiver. Moreover, we provide the experimental results from (1) a high-speed single-mode VCSEL able to transmit data at 80 Gb/s for up to 500 m of a standard single-mode fiber (SSFM) and (2) a high-speed optical transceiver with a 64 Gb/s per lane capacity suitable for high-speed intra-datacenter interconnects. Materials, methods, and processes used for the development of the structures along with the respective experimental setups are described in Section 2. In Section 3, we present the experimental results that were acquired and in Section 4, we summarize the key points of the manuscript.

2. Materials and Methods

2.1. Materials and Architecture of the Devices

The following subsections describe the structure of the devices (the high-speed VCSEL, transmitter, the VCSEL driver, and the linear receiver) and the fabrication processes that were used.

2.1.1. High-Speed Single-Mode VCSELs' Structure and Fabrication Process

The single-polarization, single-mode VCSELs described in this manuscript operate at the 1.5 μm wavelength window [9,30]. The structures were based on a double-mesa short-cavity design with a length threefold the laser's emission wavelength, permitting the minimization of the photon lifetime. To reduce parasitic limitations, the double-mesa VCSEL module was fully encapsulated in benzocyclobutene (BCB). A highly strained active region embedded between an n-doped InP layer and a highly doped AlInAs cladding (Figure 1a) enhanced the intrinsic dynamic performance of the structure. The optical gain was provided by six AlGaInAs quantum wells with a 5.0 nm thickness, grown with a 1.7% compressive strain. The dielectric distributed Bragg reflectors (DBRs) at the top (outcoupling) and the bottom (hybrid) of the design had reflectivity percentages of 99.3% and 99.9% respectively. A circular p^+-AlGaInAs/n^+-GaInAs buried tunnel junction (BTJ) with a diameter of $d_{btj} = 5$ μm confined the current within the structure. A p^+n junction with a reversed bias expanded over the bottom mesa diameter d_{bm} to achieve current blocking outside the aforementioned area, whereas the BTJ was overgrown by an n-type doped indium phosphide layer to counterpart the length of the cavity. The capacitance of the structure C_{bm} was proportional to $(d^2_{bm} - d^2_{btj})$ and was associated with the depleted region due to the steep change in the concentration of the reverse-biased junction impurities. The double-mesa architecture proposed in this manuscript allowed the construction of 16 μm bottom mesas, which limited the capacitance of the VCSEL and enhanced its overall response.
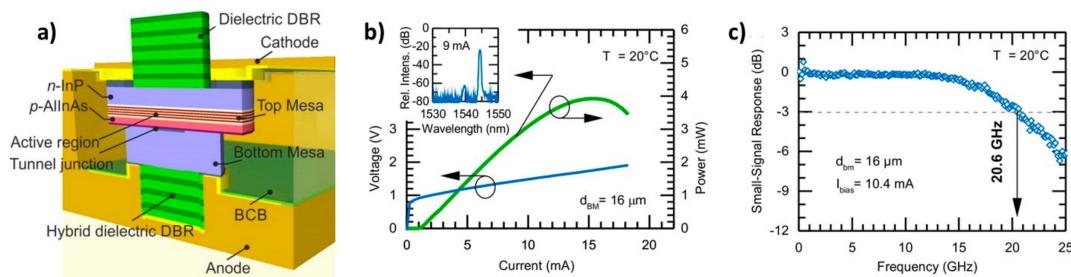

Figure 1. (**a**) The structure of a double-mesa vertical-cavity surface-emitting laser (VCSEL), (**b**) room-temperature LIV (Light-Current-Voltage) characteristics and optical spectrum (inset), (**c**) s21 graph of a 16 μm double-mesa VCSEL.

Figure 1b shows the power, current, and voltage characteristics of the double-mesa VCSEL; the inset shows its optical spectrum at 9 mA. At standard temperature conditions, the lasing threshold was achieved at around 1.0 mA whilst the peak output power was met at approximately 4 mW. To measure the small-signal modulation response of the VCSEL (Figure 1c), an HP 8519C network analyzer was used. The maximum modulation bandwidth was achieved at 10.4 mA and measured to be 20.6 GHz.

2.1.2. VCSEL-Driver Architecture and Transmitter Assembly

The single-channel block diagram of the PAM-4 VCSEL driver is shown Figure 2.a and is thoroughly described in [31]. It comprised a four-tap symbol-spaced feed-forward equalizer (FFE) and a selective falling-edge pre-emphasis (SFEP). The equalizer's taps were independently controlled, which allowed the driver to be optimally configured according to the specific transmission scenario, whereas the SFEP module was used to reduce the effect of pulse width distortion on the generated PAM-4 signal. The VCSEL driver chip was fabricated in 130 nm SiGe BiCMOS technology and exhibited a footprint of 1×2.8 mm. The transmitter board comprised a two-channel VCSEL driver and a respective array of single-mode VCSELs described in Section 2.1.1. Initially, the development of a four-channel VCSEL driver was targeted but the mismatch between the channel width of the VCSEL driver (>1 mm due to the on-chip PAM-4 generation and equalization) and the cathode pitch of the VCSELs (350 μm) prohibited such a design. The limitation in the channel pitch of the VCSEL driver mainly derived from the bond pad spacing of its data inputs (MSB (most significant Bit) and LSB (least

significant Bit)). The assembly rested on a PCB (Printed Circuit Board), designed to simultaneously drive two VCSEL driver chips. To reduce the parasitic inductance between the VCSEL and the driver, the VCSEL anode voltage was supplied by the driver chip. A second technique used to reduce the parasitic inductance was to place the decoupling capacitors directly underneath the VCSELs, omitting additional bond wires, while using the thickness of the capacitors to put the VCSEL and driver surface at the same height.
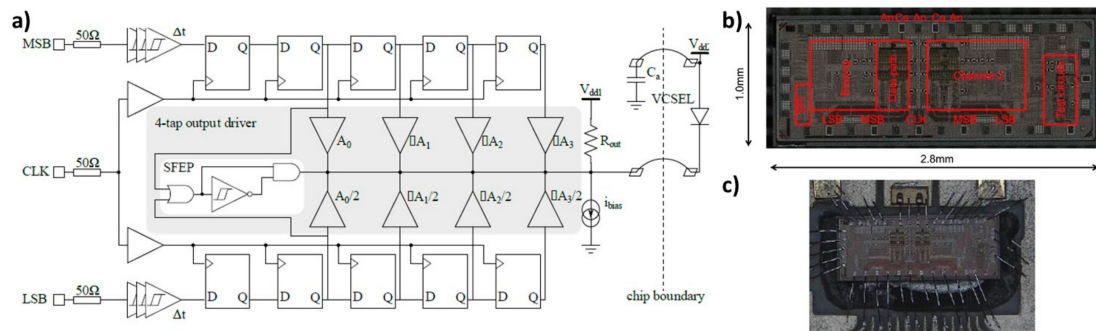
Figure 2. (**a**) Single-channel block diagram of a PAM-4 VCSEL driver, (**b**) annotated die photo of the VCSEL driver, (**c**) VCSEL driver board closeup.

2.1.3. Linear Receiver Architecture and Assembly

The linear receiver board was based on previously reported designs [31–33], which comprised a two-channel linear TIA (Transimpedance Amplifier) array (Figure 3a) that operates in tandem with a surface-illuminated photodiode array. Commercial 25 Gb/s photodiodes were used for the assembly. The TIA exploited a multi-stage low-noise linear data path architecture that converted the photocurrent to the respective voltage value, amplified it, and fed it to a 50 Ω output buffer. The saturation between the different amplifier stages was obviated by using an event-driven gain–bandwidth control loop that provided the necessary linearity and bandwidth for PAM-4 detection. The fabrication of the TIA chip was based on 130 nm SiGe BiCMOS technology and had a footprint of 1×3.7 mm. The assembly rested on a PCB that featured a cavity to align the top of the TIA with the top of the PCB to minimize the bond wire length.
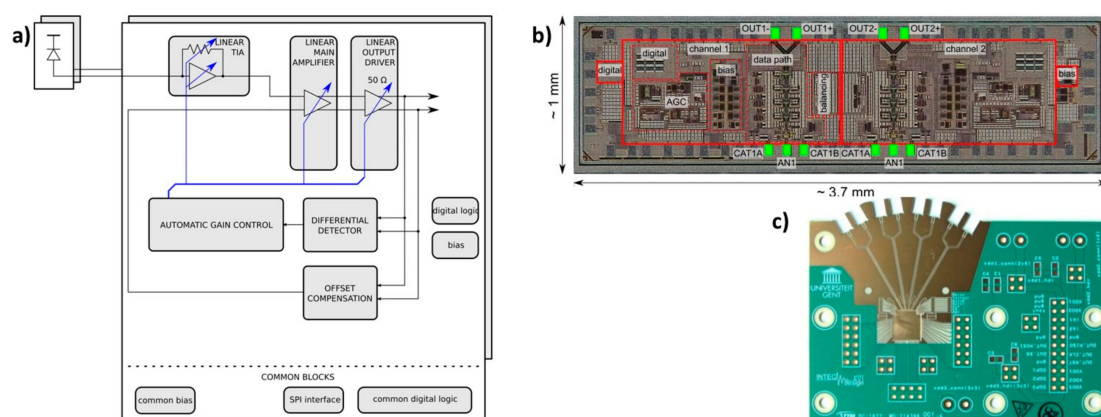

Figure 3. (**a**) Block diagram of a 2×1 TIA array, (**b**) micrograph of the TIA array die, (**c**) dual-channel receiver board.

2.2. *Experimental Setups*

The experimental setups used to test the proposed modules are described in the following subsections.

2.2.1. Experimental Setup Used for the Single-Mode High-Speed VCSEL Experiment

The experimental setup used for the high-speed single-mode VCSEL experiment is shown in Figure 4.
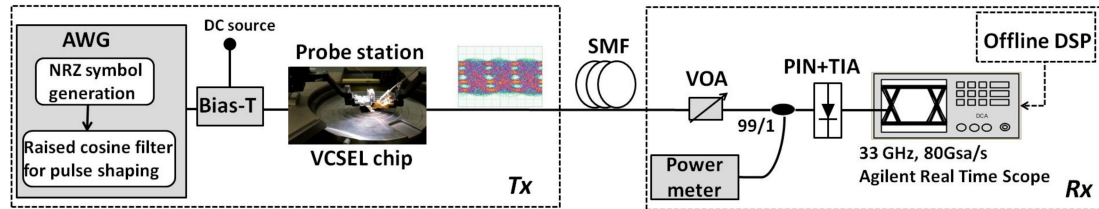

Figure 4. The experimental setup used for the high-speed single-mode VCSEL experiment.

The single-ended output of an 8 bit, 65 GSa/s keysight arbitrary waveform generator (AWG) was used to generate the respective PAM-4 electrical test signals with a repeating pattern length of 210 symbols. Digital pulse shaping was implemented by exploiting a raised cosine (RC) filter with a roll-off factor of a = 1 to restrict the bandwidth of the transmitted signal to the main lobe. A high-precision voltage source was used to drive the VCSEL above its lasing threshold. The generated electrical PAM-4 signal, with a voltage swing of 550 mV$_{P-P}$, was superimposed on the DC signal by means of a Bias-T and modulated the VCSEL directly, which resulted in a generated optical PAM-4 signal that exhibited 1.5 dBm output optical power. The light from the VCSEL was coupled to a cleaved standard single-mode fiber (SSMF) using a vertical-probing arrangement and was fed to an off-the-shelf, limiting 40 Gb/s photoreceiver, with a 35 GHz 3-dB bandwidth, a 0.6 A/W responsivity, and a 500 V/W conversion gain. A variable optical attenuator (VOA) was used to adjust the launched optical power in the receiver for bit error rate (BER) measurements. Alternatively, a spool of 500 m of the standard single-mode fiber (SMF) was utilized to evaluate the received optical signals in a transmission scenario.

The received signal was digitized by a 33 GHz, 80 GSa/s Agilent Infinium DSO-X 93304 real-time oscilloscope for BER assessment. Offline processing was applied to the digitized signal and more specifically to resampling, symbol timing recovery, and static equalization, to compensate for the bandwidth limitations of the channel. To enable symbol detection, automatic thresholding was used and subsequently the received PAM-4 signals were evaluated in terms of BER for back-to-back configuration after transmission over a 500 m spool of SSMF. Comparison between the received sampled signal and the original bit sequence was made to count the actual erroneous bits and perform the BER measurements.

2.2.2. Experimental Setup for the Transceiver Link Experiment

The experimental setup used for evaluating the performance of the full link is shown in Figure 5.
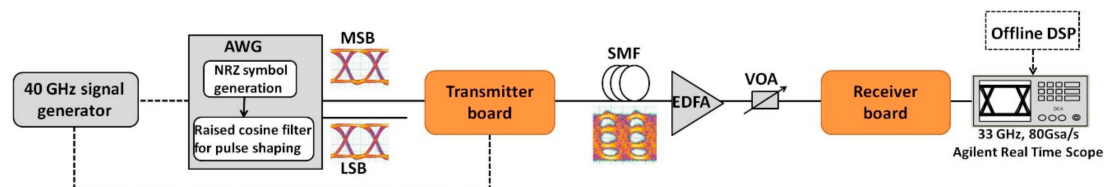
Figure 5. The setup that was used for the full-link experiment.

Two single-ended outputs of an 8 bit, 65 GSa/s keysight AWG with a repeating pattern length of $2^9 - 1$ symbols generated two identical NRZ electrical signals of 500 mV peak-to-peak to feed the respective MSB and LSB AC-coupled inputs of the VCSEL board. To decorrelate the NRZ tributaries used for generating PAM-4, a delay difference of 10 bits was introduced between the two AWG outputs. The baud rate was varied to investigate the link's performance under different data transmission scenarios. Pulse shaping to restrict the bandwidth of the baseband signal was performed

by implementing a raised cosine electrical filter with a roll-off factor of a = 1. A 40 GHz Anritsu signal generator phase locked to the AWG provided the full-rate clock reference for the transmitter board. The generated PAM-4 optical signal was transmitted through a 500 m and 2 km link of SSMF to the linear receiver board. To investigate the dependence of the BER to the incident optical power in the linear receiver, an erbium-doped fiber amplifier (EDFA) with a 28 dB gain, a 13 dBm saturated output power, and a noise figure of approximately 3.8 dB was employed along with a variable optical attenuator (VOA). The BER assessment was performed by exploiting the equipment Infiniium DSO-X 93304 real-time oscilloscope (Keysight Technologies, Santa Rosa, CA, USA) and the offline processing is described in Section 2.2.1.

3. Experimental Results and Discussion

Results from the two different experimental processes are discussed thoroughly in the following subsections. Moreover, overshoots can be observed in the case of 40 Gbaud, which derived from the VCSEL's bandwidth limitations.

3.1. Transmission of 80 Gb/s up to 500 m Exploiting the High-Speed Single-Mode VCSEL Module

Figure 6 shows the indicative optical eye diagrams at 32 and 40 Gbaud in the back-to-back configuration that were acquired with a 70 GHz equivalent time oscilloscope. As expected, the increase at the symbol rate of the signal leads to the closure of the eye pattern since the effect of intersymbol interference (ISI) is more decisive.
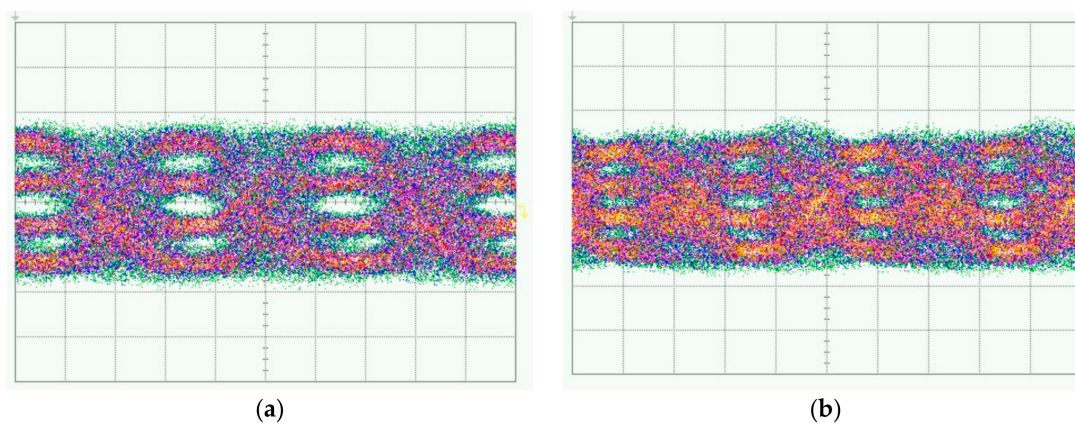

| (**a**) | (**b**) |

Figure 6. PAM-4 optical eye diagrams at (**a**) 32 and (**b**) 40 Gbaud in back-to-back configuration.

Figure 7 presents the measured bathtub curves for the cases of 32 and 40 Gbaud input signals for both transmission scenarios, which were plotted against the average received optical power in the receiver. The green and red solid lines correspond to the obtained optical signal at 32 Gbaud in back-to-back configuration and after propagation over 500 m of SSMF, respectively. Following the same rationale, the dotted black and blue lines refer to the received optical signal at 40 Gbaud for the two different transmission scenarios. As observed, for the case of 32 Gbaud and within a power range of 10 dBm (between −10 dBm and 0 dBm), the acquired BER values lie well below the hard FEC (Forward Error Correction) limit for both transmission configurations. At 40 Gbaud, despite the reasonable degradation that is observed and is mainly caused by the 3 dB bandwidth of the VCSEL, the measured BER values lie below the hard FEC limit even after propagation over 500 m of SSMF. It should also be noted that the limiting operation of the commercial receiver used in the experimental setup imposed an additional penalty to the received signal. Especially for power values higher than 0 dBm, the BER values deteriorate since the device loses its linear response. The VCSEL's excellent performance makes it an ideal module for implementation in high-speed short-reach optical interconnects.
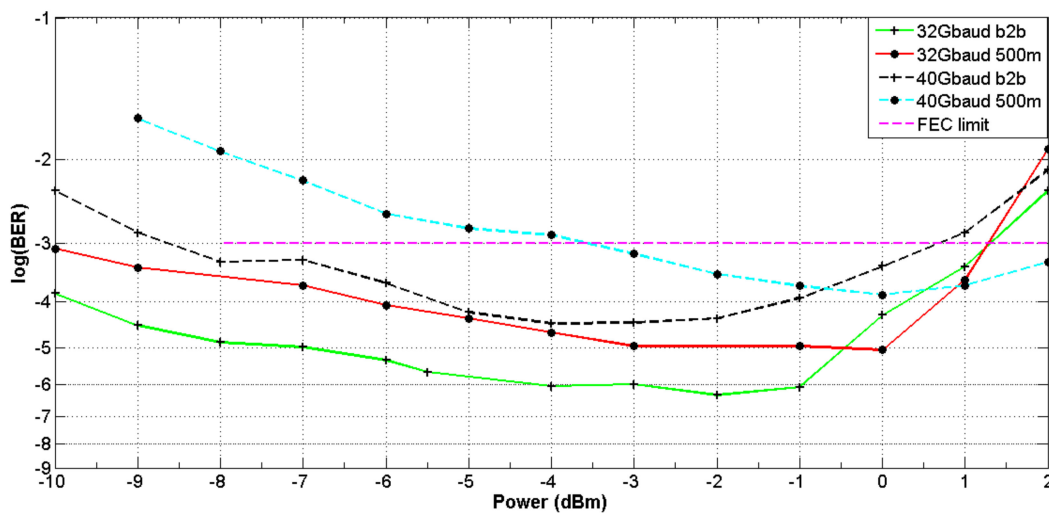
Figure 7. Bit error rate (BER) curves at 32 and 40 Gbaud in back-to-back configuration and after propagation over 500 m.

### 3.2. Up to 64 Gb/s Experiment Employing a VCSEL-Based Transceiver

The acquired PAM-4 optical eye diagrams for different transmission speeds and distances are shown Figure 8. The diagrams were captured by a 70 GHz equivalent time oscilloscope. As expected, the eye diagrams exhibit better eye opening for lower baud rates. Moreover, propagation through the SSMF, especially in the case of a reach of 2 km, introduces degradation to the eye diagram of the multi-level signal as a result of fiber dispersion at 1550 nm.
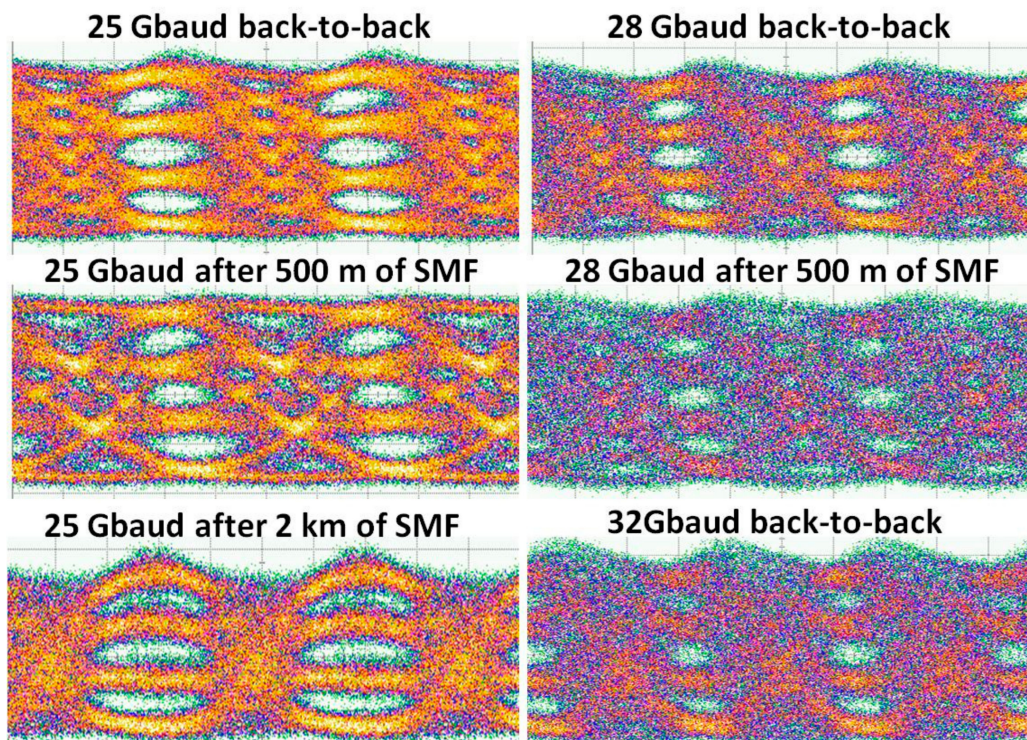
Figure 8. PAM-4 optical eye diagrams at the output of the linear receiver at 25, 28, and 32 Gbaud for back-to-back configuration and propagation in 500 m and 2 km of SSMF.

The acquired BER values at 25, 28, and 32 Gbaud for the aforementioned transmission distances were plotted against the average received optical power that was calculated from the measured

photocurrent (Figure 9). The BER curves depicted by the crosses correspond to the obtained 25 Gbaud signal in back-to-back configuration and after propagation over 500 m and 2 km. Following the same rationale, the black circles and the x-marks refer to the received signals at 28 and 32 Gbaud, respectively, according to the aforementioned transmission conditions (back-to-back configuration and after transmission over 500 m). It is evident that for lower baud rates, the received PAM-4 optical signal exhibits better performance in terms of BER. It is also clear that an extension in the transmission distance leads to the degradation of the obtained BER curves. As observed for cases of 25 Gbaud and 28 Gbaud, the achieved BER values lie well below the FEC limit for all the transmission scenarios. Moreover, the respective power penalties for transmission over 500 m and 2 km SSMF at 25 Gbaud were 0.2 dB and 0.6 dB for a BER equal to 6×10^{-4}. Similarly, the received 28 Gbaud signal exhibited a power penalty of 1.8 dB for a BER in the order of 5×10^{-4}. Finally, in the case of 32 Gbaud, only the back-to-back configuration achieved acceptable BER values, whereas propagation through 500 m of SSMF was severely affected by the effect of chromatic dispersion and, as a result, the signal failed to reach the FEC limit.
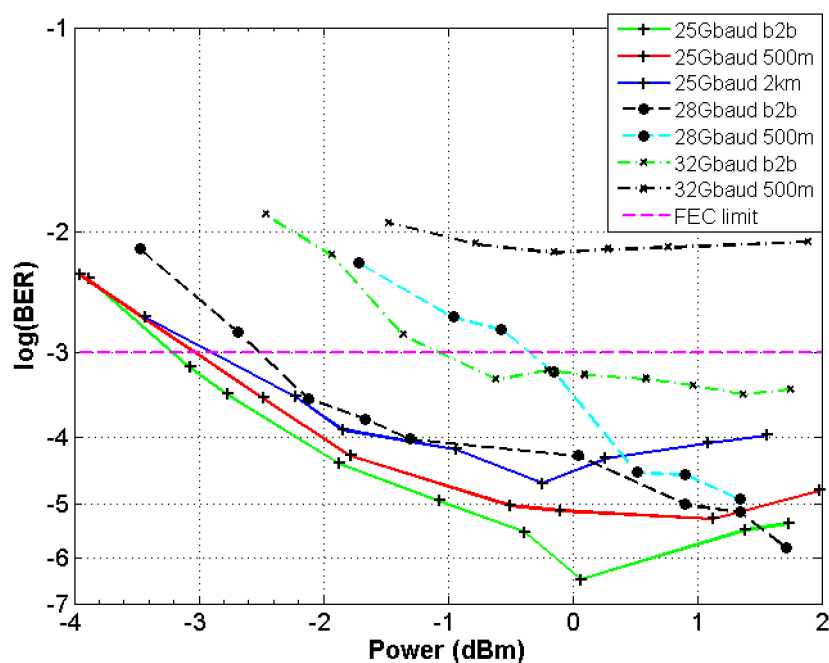
Figure 9. BER curves at 25, 28, and 32 Gbaud for back-to-back configuration and propagation in 500 m and 2 km of a standard single-mode fiber.

4. Conclusions

We have presented a high-speed VCSEL-based optical transceiver tailored for intra-datacenter connectivity. Architectures, assemblies, and experimental results from different modules that comprise the transceiver were demonstrated. The single-mode VCSEL was evaluated and exhibited a high-speed functionality of up to 80 Gb/s based on PAM-4 signaling over a 500 m link, whereas the optical transceiver demonstrated up to 64 Gb/s per lane capacity in a back-to-back configuration and 56 Gb/s per lane capacity in a full-link data transmission experiment over a 2 km link. The results prove that the device is suitable for 200 GbE intra-datacenter applications.

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