A NEW CARRIER RECOVERY METHOD FOR A SIX-PORT MILLIMETER WAVE RECEIVER

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Abstract --- A new direct conversion wide band (23 GHz – 31 GHz) six-port millimetre wave receiver for QPSK communications suitable for integrated circuit fabrication is proposed, to satisfy mass-market wireless communications. The receiver contains one multi-chip module consisting of a wide-band six-port junction, four RF detectors (diodes), video amplifiers and I&Q decoder. The prototype circuits are fabricated in hybrid integrated circuits and the receiver topology is suitable for fabrication in microwave monolithic integrated circuits (MMICs). A new method of carrier recovery using six-port output voltages is proposed. A control signal for VCO is generated and simulation results are presented.

1 INTRODUCTION

It is widely recognized that direct conversion receivers offer unique advantages in wireless communications by reducing circuit complexity and allowing a higher level of circuit integration than traditional heterodyne receivers [1]. Six-port direct conversion receivers have been proposed [2,3,4,5] as multi-mode or software receivers operated with DSPs programmed for a number of modulation schemes. This paper presents recent results obtained on a new uni-mode six-port based hardware type receiver designed with application specific circuits (ASC) for QPSK communications. The proposed millimeter wave ASC approach is useful to design other uni-mode receivers at lower or higher operating frequencies (microwaves and sub-millimeter waves) using either discrete [3,5] or distributed parameter [2,4] six-ports. The channel bandwidth is solely limited by speed of video and decoder circuits such that data rates are limited mainly by video-amplifier bandwidth (e.g. 25 MHz).

A new carrier recovery method is presented in this paper in which voltage control signal to VCO is generated using the output signals of the six-port.

2 RECEIVER ARCHITECTURE AND OPERATING PRINCIPLE

Fig.1 shows hardware six-port receiver architecture with a number of circuit functions to provide I&Q data and a control voltage signal from received QPSK signals.

The equations for signals Q and I (where v_1, v_2, v_3, v_4 are voltages at the four inputs of Q&I decoder) are:

$$\begin{cases} Q=\text{if } [v_3>v_2] \text{ then } (1) \text{ else } (-1) \\ I=\text{if } [v_2>v_1] \text{ then } (1) \text{ else } (-1) \end{cases} \quad \textbf{(1)}$$

Comparators, logical circuits and a frequency/voltage converter are used to obtain a signal for the carrier recovery circuit. The carrier recovery circuit contains four LPF with cut-off frequency of 10 KHz, a “sense of rotation “ circuit (1) and a frequency/voltage converter (2) that are shown in Fig.1. If VCO frequency is different from carrier RF frequency a rotating I&Q constellation appears. At each rotation a clock signal C is generated as shown in Fig 3. When the clock signal C falls from 1 to -1 the memory keep the sign S and the sense of constellation rotation is determined. The frequency of rotation is converted into a voltage to control VCO**.** The equations for control signals C and S used in the sign generation (where the v_1, v_2, v_3, v_4 are the voltages at the inputs of Q&I decoder) are:

$$\begin{cases} C=\text{if }[0.05*v_2>v_1]\text{and}[0.6*v_3>v_2]\text{then}(1)\text{else}(-1) \\ S=\text{if }[0.5*v_3>v_2]\text{ then }(1)\text{ else }(-1) \end{cases} \qquad \textbf{(2)}$$

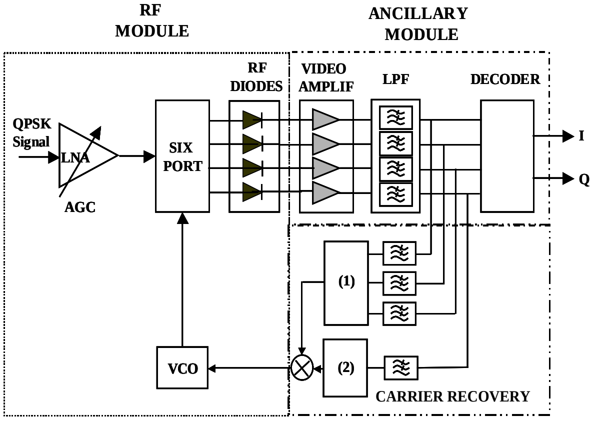

Fig.1. Receiver architecture

If VCO frequency is different from carrier RF frequency, the four output DC voltage levels change in time (Fig. 5). Therefore the outputs Q and I change as shown in Fig.6 and Fig.7. A graphical representation in I/Q plane is given in Fig.2. The hatched circle marks the I/Q capture zone. When the I/Q point crosses to the exterior of the marked circle, the memory circuit of Fig.3 retains the sign (the sense of rotation). The frequency difference between RF and VCO signals is converted into a DC voltage magnitude using a frequency/voltage converter (Fig.4).

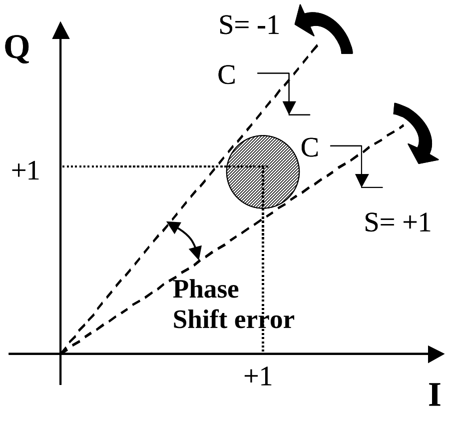

Fig.2 Determination of the sense of rotation

To this DC voltage is added the sign given by the "sense of rotation" circuit of Fig.3 and resulting control voltage signal is applied to VCO as shown in Fig.1. After capture the I/Q point remains fixed in the marked circle. The diameter of this circle is a function of the coefficients used in equation (2). The synchronization is obtained with a briefly interruption of QPSK modulation (I=1 and Q=1).

It is to be noted that the power levels at the inputs of the six-port should be equal: in practice an AGC circuit is necessary to equalize power levels within 3 dB. Comparators and logical circuits are used in the "sense of rotation" circuit as shown in Fig.3. Three TL3016 comparators are used in addition with a "logic-and " circuit and a memory circuit.

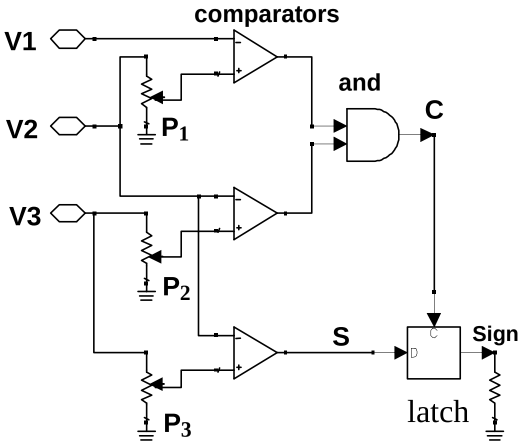

Fig.3. The "sense of rotation " circuit

An electrical implementation of the frequency/voltage converter is presented in Fig.4, using ST-TSH321 operational amplifier.

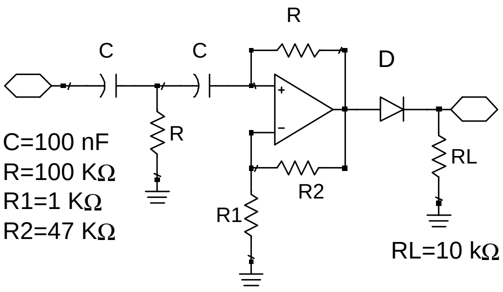

Fig 4.The frequency/voltage converter circuit

The magnitude of DC output voltage is a linear function of the input frequency. The constant of conversion [V/Hz] given in Fig.8 is a function of R1 and R2, and the frequency range and linearity of conversion is a function of R and C.

3 SIMULATION RESULTS

For two equal power signals at the input of six-port (for this case the power levels are – 20 dBm) the DC voltages at the outputs of RF module (v_1, v_2, v_3, v_4), in function of phase shift between the two signals, are given in Fig 5.

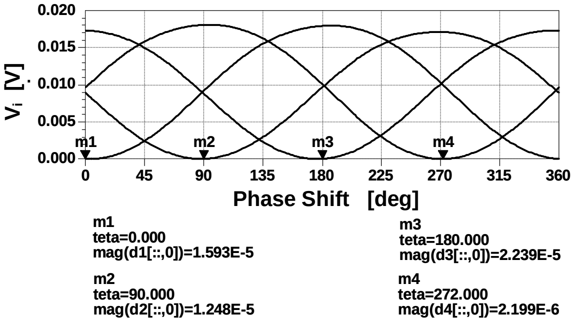

Fig 5. The DC outputs voltages to phase shift

Each DC voltage value has a minimum level during a 360° phase shift between RF and VCO signals. If a frequency (phase) difference exists, the v_i voltage values change in time and the C and S signals are used for sign generation in the "sense of rotation " circuit.

When a frequency difference between RF and VCO signals exists, the I, Q, C and S signals are given in Fig 6. for a positive difference (in this case, the frequency difference value is equal to +1 KHz).

The I, Q, C and S signals are given in Fig.7 for a negative difference between RF and VCO frequencies (in this case, the frequency difference value is equal to -1 KHz). At each clock signal C, a value for S is obtained. If the frequency difference value is positive the sign is positive**.** If the frequency difference value is negative, the sign is negative.

The frequency of each v_i signal is the difference between RF and VCO frequencies. One of this DC output voltages (in this case v_4) and a frequency/voltage converter could be used to obtain the magnitude of the control voltage for VCO as shown in Fig.4. Simulation results are presented in Fig. 8.

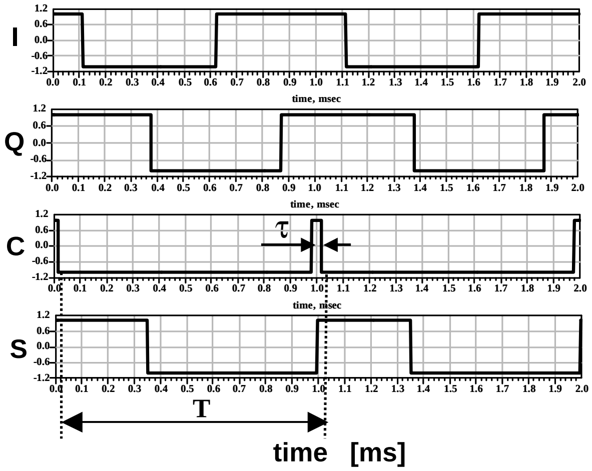

Fig 6. The simulated output signals for +1 kHz frequency difference

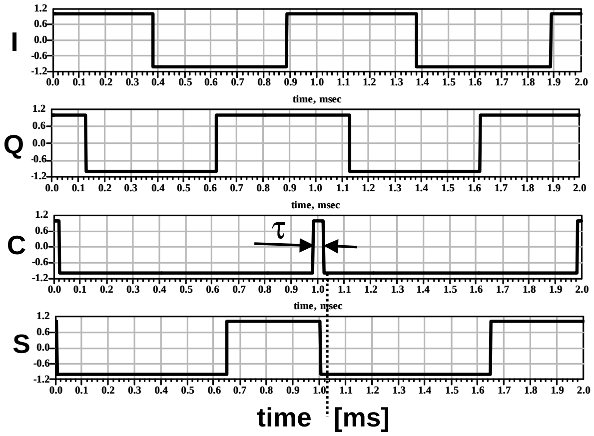

Fig 7. The simulated output signals for -1 kHz frequency difference

The simulated result of BER versus Eb/No is shown in Fig.9. Data rate for the QPSK signal is 40 Mbps and the phase shift error of VCO from synchronism is: a) max ± 20°, b) ± 35° and c) ± 40°.

The phase shift error of VCO (related to the diameter of hatched circle in Fig.2) is determined by the coefficients of equations (2). Those were chosen for a maximum phase shift of ± 20° were the simulated BER curve is identical with the theoretical one (curve "a" in Fig.9).

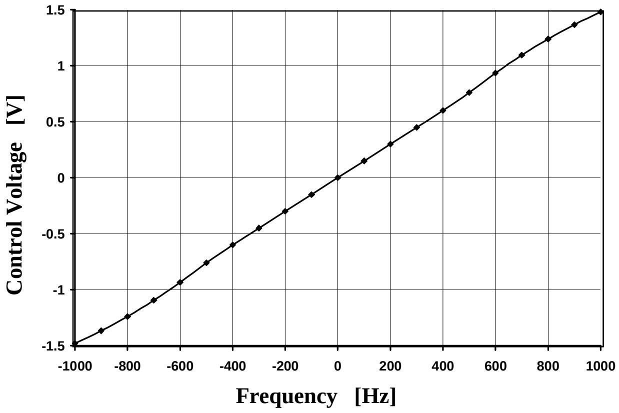

Fig.8. Simulated results of control voltage response in opened control loop to positive and negative frequency differences between carrier and voltage control oscillator frequencies

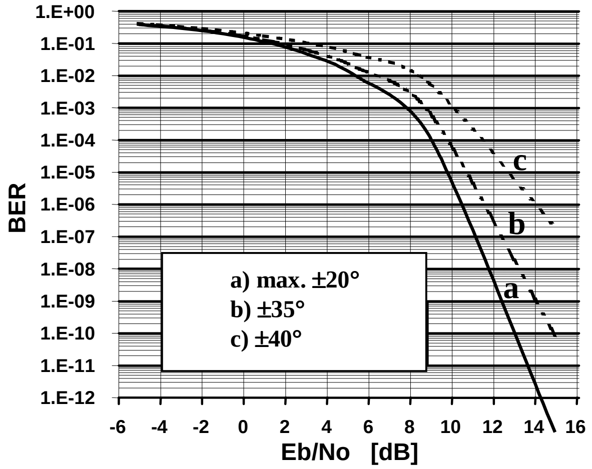

Fig.9. Simulated results of BER vs. Eb/No for different VCO phase shift errors from synchronism

The phase shift error is equal to **±(τ/T)*180°** (the simulation results of Fig. 6 for C control signal).
This control signal is obtained during the synchronization time (a QPSK signal of I=1 and Q=1 is transmitted).

CONCLUSIONS

A new carrier recovery method for a direct conversion hardware receiver based on six-port technology suitable for mass-market wide band millimeter wave applications was presented in this paper. The proposed concept of six-port receiver was verified by measurements and simulations made on hybrid integrated circuit prototype having an operating band of 8 GHz (23 GHz – 31 GHz).
BER results on operating dynamic range, signal to noise ratio, signal interference and LO phase noise measurements encourage fabrication of MMIC integrated front-ends of this receiver [6]

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