Intrinsic Evolvable Hardware Used for Fault Tolerance Systems

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ABSTRACT

The main target of this chapter is to present the intrinsic evolvable hardware structures: concept, design and applications. The intrinsic evolvable hardware structures concept join more research areas like: bio-inspired searching methods (evolutionary algorithms), optimization of algorithms by parallel processing and reconfigurable circuits. First, a general overview about intrinsic evolvable hardware structure is presented. The intrinsic evolvable hardware structure consists in two main modules: hardware genetic algorithm and dynamic reconfigurable circuit. In a particular application, the hardware genetic algorithm searches the configuration that makes the reconfigurable circuit to correctly respond to application requirements. In a background section are presented the genetic algorithm concept as a bio-inspired search solution, the hardware reconfiguration concept with sub areas classifications and the research directions in the evolvable hardware structures areas with application examples. In the first part of the main section are presented the design solutions for hardware implementation of genetic algorithm. Then the solutions are presented for the reconfigurable circuit design and interconnection between reconfigurable circuit and hardware genetic algorithm. Finally, are presented several applications that illustrate the usefulness of the intrinsic evolvable hardware structure. Intrinsic evolvable hardware can be used as a method of resolving faults occurring in some parts of the digital circuit.

Keywords: Artificial Intelligence, Dynamic/Static Reconfiguration, Evolutionary Design, Evolvable Hardware, Fault Tolerance Systems, Field Programmable Gates Array

1. INTRODUCTION

Currently, there is often the requirement of building autonomous systems. Exploring space and others inaccessible areas using autonomous mobile electronic platforms, requires careful increasingly higher feasibility of systems and their fault tolerance. FPGA (Field Programmable Gates Array) digital systems may be subject to slight error types (soft errors) which appear only in a single clock cycle execution or large errors (hard errors) which are perma-

DOI: 10.4018/joci.2012040102
nently. There are several solutions to solve “on the place” these errors, which are a feature of autonomous systems, from static approximations of deterministic solutions to heuristics methods including intrinsic evolvable hardware (Rashad, 2012).

Intrinsic evolvable hardware is a strategy to redesign the circuit “on the place”, without others external systems – human operators or computers. Intrinsic evolvable hardware involves running an evolutionary algorithm - for example a genetic algorithm, fully integrated on chip, usually used to find solutions to design digital circuits (finding configurations of connections between layers of gates, multiplexers, etc. from areas) starting from different functional requirements (Xuesong, 2011) and requirements related to the nature of hardware resources which can be used (some types of circuits or certain configurations), energy consumption, allocation of on-chip components to size - to optimize the silicone area occupied (Walker, 2011), configuration matrices silicon layers assigned to programmable analog and digital arrays (PAnDA) (WalkerII, 2011) and others. In this case we speak of a basic feature of evolutionary algorithms (hardware implemented or not) that is multi-objective designing (Liang, 2012).

Functional requirements are present in the first configuration of the circuit - the evolutionary synthesis of logic circuits, and the reconfiguration of the circuit after it has suffered some damage during operation or it would restore some routes that are too busy signals and generate cohesion etc. (Vernekar, 2010).

The starting point for this chapter is the intrinsic evolvable hardware structure (configurable through its own resources) illustrated in Figure 1.

It is composed of several modules, each allocate the sections in this chapter. A reconfigurable circuit is a circuit which can change their behavior according to a map of configurations that is generated.

The process of generating the map of connections, from a structural or functional description of the new behavior is called logic synthesis of the circuit. There are several methods for synthesis of logic circuits, but in principle the synthesis is a laborious process, requiring a high volume of operations (performed with the DeMorgan rules, minimization).

The evolutionary algorithms are search algorithms in an expanded space of multiple objective solutions. They are used in several areas in which other search methods are not effective. The use of evolutionary algorithms to solve multi objecti ve problem of has be moti vated mainly because of population of solution-based nature of its which allow generation of several optimal set in a single run (Coello, 2002). In evolvable hardware structures, they are used to found a map of configurations in

Figure 1. Intrinsic evolvable hardware structure
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