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A generally applicable calibration algorithm for digitally reconfigurable self-healing RFICs

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Abstract: The design of radio frequency integrated circuits (RFICs) presents many challenges. To meet design performance goals, designers are often forced to choose between over designing the critical RF analog blocks or increasing the complexity of the analog calibration control circuitry in order to obtain calibration responses which can be solved using convex optimization algorithms. This common approach to RFIC design can lead to both longer design times and circuit design solutions which are not generally applicable for multiple performance-critical blocks in an integrated chip system. To overcome the increased design burden for high-performance RF blocks, global optimizers, such as genetic algorithms, can be used to calibrate out performance degradations at runtime, but require the fine-tuning of many algorithm-specific parameters, thus making them difficult to use and implement in an embedded calibration application. The self-healing calibration approach advocated in this work exploits the observation that RF blocks equipped with suitable sensors and digitally reconfigurable actuators often have locally optimal solutions in the calibration response space which sufficiently meet the performance objective. More specifically, in this work the feasibility of applying direct search local optimization algorithms to the digitally reconfigurable self-healing RFIC calibration problem is investigated. Implementation details for a hybrid direct search calibration algorithm which is relatively straightforward to use and implement are given, performance results using an eight-dimensional digitally reconfigurable self-healing RFIC test case are presented to show the efficacy of the proposed calibration strategy, and implementation overhead estimates are given to aid the RFIC designer in incorporating the developed direct search calibration strategy into their embedded calibration framework.

Speaker: Eric J. Wyers received the B.S. degree with High Honors from the University of Illinois at Urbana-Champaign, IL USA, in 1996, the M.S. degree from Oregon State University, Corvallis, OR, USA, in 2003, and the Ph.D. degree from North Carolina State University (NCSU), Raleigh, NC, USA, in 2013, all in electrical engineering. He has held various industry positions as an analog integrated circuit designer and is the co-author of two U.S. patents. He is currently a Postdoctoral Research Scholar at North Carolina State University, Raleigh, NC, USA. His current research interests include highly efficient calibration techniques for sensor/actuator-based integrated RF systems, the application of iterative optimization algorithms to integrated circuit design problems, CMOS and III-V device stress characterization and modeling for 3D heterogeneous integration applications, “beyond CMOS” applications, low-power design techniques for high-speed communication circuits, and emerging topics in analog, RF, and mixed-signal circuit design, reliability, and yield. Dr. Wyers is a member of the Institute of Electrical and Electronics Engineers (IEEE), Eta Kappa Nu, Tau Beta Pi, and the Society for Industrial and Applied Mathematics (SIAM).