Optimization and implementation of a multi-level buck converter for standard CMOS on-chip integration

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Outline

- Introduction and motivation
- Series-connected multiphase multilevel buck converter
  - Ideal topology. Amplifier and regulator operation
  - Self-driven low-floating-capacitor PFM-operated 3-level converter
- Design-space optimization
- Mixed-signal implementation in 0.25µm TSMC CMOS
  - Air-core bondingwire-based inductor, tapered buffer and transistor design
  - Inductor current zero-crossing detection circuit
- Conclusions
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3-Level (2-cell) Buck Converter

- 3-level (2-cell) converter has been proposed for high voltage inverters [Meynard et al., 1992]
- “g1-g2” & “g3-g4” are complementary switches
- g1 and g3 have the same duty cycle
- VC = ½ Vin

**Objective:**
Investigate potential for lower ripple/ higher efficiency / lower reactive component size / higher bandwidth realization of DC-DC converter
Switching Ripple in the 3-Level Buck Converter

Ripple comparison of 3-level and buck converter with same $f_s$, $L$, $C$

- 4 times smaller peak inductor current ripple
  \[ \Delta i_{\text{max}_n} = \frac{1}{(n-1)^2} \Delta i_{\text{max}_2} \]

- 8 times smaller peak capacitor voltage ripple
  \[ \Delta v_{\text{max}_n} = \frac{1}{(n-1)^3} \Delta v_{\text{max}_2} \]

Ripple results similar to two-phase converter, but with a single, smaller inductor.
3-Level (2-cell) Buck Converter

Comparison of 3-level and buck converter

- For $\Delta v_{max} = 12 \text{ mV}$, $f_s_3 = 200 \text{ kHz}$, $f_s_2 = 560 \text{ kHz}$ $\Rightarrow \eta_2 = 0.83$ and $\eta_3 = 0.92$

$\Rightarrow$ improved efficiency

- Same $f_s$, $\Delta v_o$, $\Delta i_L \Rightarrow L_3 = 0.25L_2$, $C_3 = 0.5C_2 \Rightarrow$ reduced area

Example application to switching power amplifier
Two-Tone Signal Generation Using a 3-Level and a Buck Converter

A two-tone signal generated with a three-level and a buck converter.

Switching frequency, $f_s = 1$MHz, $f_{\text{sig}} = 100$kHz, $f_o = 550$kHz, $Q = 1$
Experimental Envelope Tracking Waveforms

Standard buck converter

- Standard buck and 3-level buck compared for the same open-loop bandwidth and the same switching frequency
- Modulation: rectified sine-wave at $f_m = 20$ kHz
- 30dB lower switching-frequency harmonic in the 3-level converter

3-level buck converter
Flying capacitor voltage control

- Digital (verilog) controller implementation using FPGA

- \( x \) and \( y \) are sampled at
  - \( V_{sw} = V_C \) or
  - \( V_{sw} = V_{in} - V_C \)
Experimental waveforms for flying capacitor voltage control

Uncontrolled capacitor $C_x$ voltage

Controlled capacitor $C_x$ voltage

$V_{sw}$

$g_1$

$g_3$

$D > 0.5$

$D < 0.5$

$V_{in} - V_c$

$V_c$

$V_{in} - V_c$

$V_c$

$V_{in} - V_c$

$V_c$

$V_{in} - V_c$

$V_c$
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3-level self-driving PFM low-Cx buck converter

Low-C_x resonant 3-level buck converter in DCM. Self-driving transistor-level topology

Self-driving scheme to interconnect power transistors and drivers, which reduces the voltage across the power MOSFETs gate dielectric.
3-level self-driving PFM low-Cx buck converter

- Use of core transistors to implement the power MOSFETs
- Use of core transistors to implement power drivers of $P_2$ & $N_2$
- Reduces the power consumption of the power drivers

Driver supply voltage and $vgs$ for all power MOSFETs, Cadence transistor-level simulations.

37 MHz switching frequency
26 nH inductance
3-level self-driving PFM low-Cx buck converter

Output voltage ripple as a function of $V_o$, for the 3-level ($C_x$ sweep) and the classical (dotted line) Buck converters.

Control signal-to-output voltage transfer function comparison between the 3-level ($C_x$ sweep) and the classical (dotted line) Buck converters.

Representative waveforms corresponding to a DCM operated 3-level Buck converter, duty cycle below 50%.

$L=35\,nH$  \hspace{1cm}  $V_{bat}=3.6\,V$

$C_o=30\,nF$  \hspace{1cm}  $V_o=1\,V$

$f_s=25\,MHz$  \hspace{1cm}  $I_o=100\,mA$
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Circuit topology considerations

Optimized design space exploration (II)

1) Model each performance index (ripple, efficiency and area) as a function of design parameters: inductor, capacitor and switching frequency

* A priori parameters and assumptions are application-oriented: topology, $V_{in}$, $V_{out}$, and the target IC technology parameters.

**Output voltage ripple**

$$\Delta V_o = \frac{V_o D T_s}{RC} = \frac{V_o D}{RC f_s} = f_{\Delta V_o}(L, C, f_s)$$

**Efficiency**

$$\eta = \frac{V_{in} I_L - P_{L-DC} - P_{L-core} - P_{Q-all}}{V_{in} I_L} = f_\eta(L, C, f_s)$$

**Occupied area**

$$Area = A_C + A_L + 2A_Q = f_{\text{area}}(L, C, f_s)$$
Circuit topology considerations

Optimized design space exploration (III)

2) Define a merit figure encompassing the performance indexes to be maximized or minimized

*generic merit figure*

\[
\Gamma(x_1,\ldots,x_n) = \frac{\prod_{i} \beta_i f_i^{\gamma_i}(x_1,\ldots,x_n)}{\prod_{j} \beta_j f_j^{\gamma_j}(x_1,\ldots,x_n)}
\]

*Boost converter case example merit figure*

\[
\Gamma(L,C,f_s) = \frac{f_\eta(L,C,f_s)}{f_A^2(L,C,f_s) \cdot f_{\Delta v_o}(L,C,f_s)}
\]

Note that the area dependence is square-weighted so as to solve the ill-conditioned solution of \(\Delta v_o \to \infty\) when \(A \to 0\).

\(f_s = \{1\text{MHz,100MHz}\},\ L = \{10\text{nH,1uH}\},\ C = \{10pF,10nF\}\)
Optimized design space exploration (IV)
Design example for a standard 0.35 μm CMOS technology

3) Obtain optimum point within design space \((L, C, f_s)\) as regards efficiency, occupied area, functionality

Specs: \(\Delta v_o = 0.1\ V\ \ i_{out} = 0.4\ A\)
Optimization result: \(L = 30\ nH, C = , f_s = 50\ MHz\)
Optimized design space exploration

3-level converter design example for a standard 0.25 µm CMOS technology

Table 6.3. 3-level converter selected design main characteristics, referred to $I_o = 100mA$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor (L)</td>
<td>26.75 mH</td>
</tr>
<tr>
<td>Output capacitor (C_o)</td>
<td>28.5 mF</td>
</tr>
<tr>
<td>$C_e$ capacitor ($C_{fe}$)</td>
<td>5.07 mF</td>
</tr>
<tr>
<td>Switching frequency ($f_s$)</td>
<td>37.28 MHz</td>
</tr>
<tr>
<td>$T_1$ and $T_3$ duration</td>
<td>6.35 ms</td>
</tr>
<tr>
<td>$T_2$ duration</td>
<td>5.05 ms</td>
</tr>
<tr>
<td>$T_1$ and $T_3$ inactivity states duration</td>
<td>917 ps</td>
</tr>
<tr>
<td>Operating mode</td>
<td>DCM</td>
</tr>
<tr>
<td>Inductor current at the end of $T_1$ ($I_{L1}$)</td>
<td>211.2 mA</td>
</tr>
<tr>
<td>Total power losses ($P_{total}$)</td>
<td>45.5 mW</td>
</tr>
<tr>
<td>Power efficiency ($\eta$)</td>
<td>96.68%</td>
</tr>
<tr>
<td>Total occupied area ($A_{total}$)</td>
<td>5.08 mm$^2$</td>
</tr>
<tr>
<td>Output voltage ripple — $I_o = 100 mA$ ($\Delta V_o$)</td>
<td>44.6 mV</td>
</tr>
<tr>
<td>Output voltage ripple — $I_o = 5 mA$ ($\Delta V_o$)</td>
<td>49.4 mV</td>
</tr>
</tbody>
</table>

Design space exploration of a CMOS-compatible 3-level converter: 70% efficiency, 5mm$^2$ silicon and $f_s=37$ MHz
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Bondwire triangular spiral inductors in standard CMOS

- Area underneath inductor is usable for capacitors and power MOSFETs

<table>
<thead>
<tr>
<th>Technical parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired inductance</td>
<td>50 nH</td>
</tr>
<tr>
<td>Tolerance on desired value</td>
<td>3 %</td>
</tr>
<tr>
<td>Bonding pad resistance</td>
<td>13 mΩ</td>
</tr>
<tr>
<td>Bonding wire resistivity</td>
<td>49.69 Ω/m</td>
</tr>
<tr>
<td>Bonding wire radius</td>
<td>12.5 μm</td>
</tr>
<tr>
<td>Distance between bonding wires</td>
<td>50 μm</td>
</tr>
<tr>
<td>Area coefficient γ_L,A</td>
<td>1</td>
</tr>
<tr>
<td>Resistance coefficient γ_L,R</td>
<td>10</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final inductance L</td>
<td>48.95 nH</td>
</tr>
<tr>
<td>Outer side length s_cat</td>
<td>2.6 mm</td>
</tr>
<tr>
<td>Number of turns n_L</td>
<td>4</td>
</tr>
<tr>
<td>Occupied area A_L</td>
<td>3.02 mm²</td>
</tr>
<tr>
<td>ESR R_L</td>
<td>1.503 Ω</td>
</tr>
</tbody>
</table>
Power MOSFETs

Complete loss optimization of on-chip CMOS synchronous rectifier

- $W_P = 3092\mu m$
- $W_N = 2913\mu m$
- Power drivers with 7.59 and 7.48 tapering factors
- Overall losses 37.1mW

Breakdown of loss distribution, corresponding the optimized design of power MOSFETs and their associated drivers.
Power MOSFET gate drive design

Additional degree of freedom: impact of $W_p$ upon efficiency and delay

$Q_i$ and $Q_{e1}$ variation as a function of the PMOS channel width of the minimum inverter ($W_n = 0.3\mu m$)

$t_{fr1}$ and $t_{fre1}$ parameter variation

Total energy losses as a function of the number of inverters $n$ and the minimum inverter PMOS channel width $W_p$. The area includes all the designs constrained to a propagation delay lower than 1.15 ns.
The body diode of the NMOS power switch turns-on as a consequence of a premature cut-off of the power transistor.

1. The NMOS is switch-off before $i_L=0$
2. The parasitic body-diode is turned-on

Inductor current charges the x-node parasitic capacitor and a positive voltage pulse appears in $V_x$ voltage, due to late cut-off of the power transistor.

1. The NMOS is switch-off after $i_L=0$
2. A positive voltage pulse appears in $V_x$
$i_L = 0$ detection circuit. Circuit for time adjustment. Inductor current observer.
$i_L = 0$ detection circuit Mixed-signal implementation in 0.25µm CMOS
Time-domain performance of $i_L=0$ detection circuit

Before adjustment

After $i_L=0$ adjustment
Complete integrated 3-level CMOS switching power converter
Full-transistor-level circuit results (I)
Full-transistor-level circuit results (II)
Full-transistor-level circuit results (III)
Experimental results
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- Three-level converter results in favorable trade-offs in terms of decreasing the switching ripples, decreasing the switching frequency, reducing the size of the filter elements, increasing the converter open-loop bandwidth, or increasing the converter efficiency.

- The 3-level converter with low-Cx, self-biased drivers and operating in DCM/PFM has been presented as a candidate for DC-DC converter integration.

- The use of the self-driving scheme to supply the drivers allows the use of thin-oxide transistors which increases the performance of the switches.

- Design optimization results in the 3-level converter outperforming the Buck converter.

Future research lines

- Linear-assisted scheme for multilevel converters
- Explore extending the approach to more intermediate levels
- Use different modulations (e.g. asynchronous sigma delta)
- Applying time optimal control