

Thermal Behavior Investigation of Cascode GaN HEMTs

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Abstract

This paper presents the evaluation of heat generation behavior and related thermal measurement analysis of packaged high-power AlGaIn/GaN high electron mobility transistors (HEMTs) cascaded with low-voltage MOSFET and SiC SBD. Since thermal management is extremely important for high power packaging, a hybrid integration of the GaN HEMTs onto a DBC substrate and metal case is proposed. We investigate the temperature performance of cascode GaN HEMTs by thermal simulations in comparison to the experimental results by using infrared thermography. For a power dissipation under 11.8 W, the peak temperature of the GaN HEMTs is 118.7 °C.

1. Introduction

AlGaIn/GaN High Electron Mobility Transistors (HEMTs) have the advantages of wide bandgap, high breakdown voltage, and high electron mobility. Unlike conventional field-effect transistors (FETs) which are added impurities to produce n-type and p-type material, the conducting channel of HEMT is generated by the piezoelectric polarization caused by its heterojunction structure. Due to the dislocation between AlGaIn and GaN layers, there would be piezoelectric polarization at the interface. When voltage inputs to gate, the electron concentration at heterojunction would change and form two-dimensional electron gas (2DEG), which plays the role of conducting channel. ⁽¹⁾ The GaN HEMTs fabricated on large diameter Si substrates have emerged as promising candidates for high-voltage power management applications. However, device performance degradation is still an unsolved issue with present-day GaN technology. ^(2, 3) With high power application of GaN HEMTs, the heat accumulation in the device became the main effect of the reliability. Therefore, a great concern with the devices is the thermal management. In this work, we simulated the thermal distribution of cascode GaN FET and illustrated the related measurement.

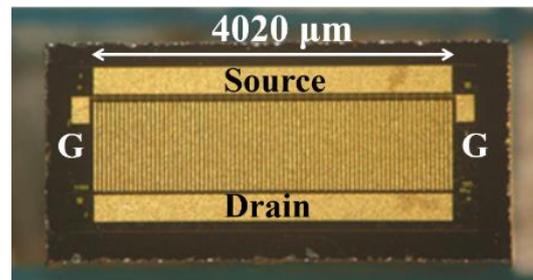
2. GaN HEMT Structure

The AlGaIn/GaN HEMTs used in this research were made by Compound Semiconductor Device Lab., National Chiao Tung University. The geometry is shown in Fig. 1. First, 3.9-μm-thick GaN/AlGaIn buffer layers were grown

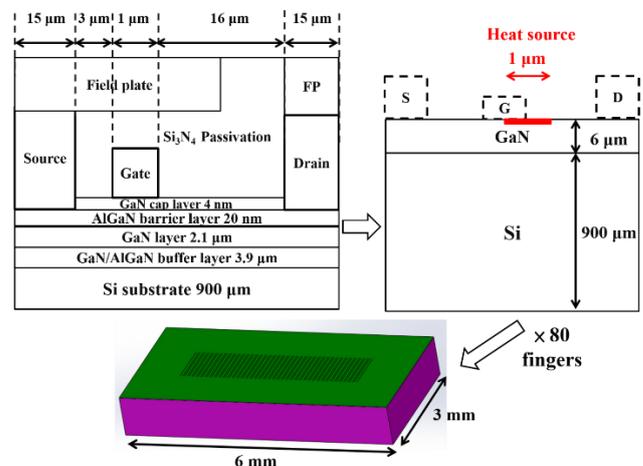
on 900-μm-thick substrate. Next, a 2.1-μm-thick GaN layer, a 20-nm-thick AlGaIn barrier layer and a 4-nm-thick GaN cap layer are grown in order. Then, the drain and source on the transistors were made of Ti/Al/Ni/Au (20 nm /120 nm /25 nm /100 nm) multi-layers as well as Ni/Au (50 nm /450 nm) for gate. After that, the chip was passivated by a Si₃N₄ layer as passivation (Fig.1 (b)), which can protect the transistors from oxidation and corrosion. Finally, the gold field plates were plated on source and drain. All fingers are connected by air bridges (Fig. 1(a)) and link to the pads separately.

3. Cascode GaN FET Packaging

The AlGaIn/GaN HEMTs are working in depletion mode; therefore, the application is limited. Normally-off operation characteristic is required in industrial power drive



(a) The top view of AlGaIn/GaN HEMTs.



(b) The cross-section of a single finger and simplified structure for simulation.

Fig. 1. Structure of AlGaIn/GaN HEMTs in this paper.

circuits to satisfy fail-safe criteria and simple gate drive configuration. A popular solution proposed to address the normally-off requirement is a cascode configuration consisting of a high-voltage, normally-on GaN HEMTs device and a low-voltage silicon MOSFET as shown in Fig.2. The gate of the HEMT connects to the source of the MOSFET to form the source of the cascode GaN FET. From equation (1), if the gate-to-source voltage V_{GS} is smaller than the threshold voltage V_{TH} , the operation is in cutoff region, which indicates that the cascode GaN FETs is turn-on when V_{GS} is larger than V_{TH} . In addition, the low-voltage MOSFET is a normally-off device, so the cascode GaN FET is normally-off. Combining the advantage of high switching frequency of GaN HEMT and the characteristic of normally-off MOSFET, the cascode GaN FET can be used for more applications.

$$I_D = \begin{cases} 0, & \text{for } V_{GS} \leq V_{TH} & - \text{cutoff} \\ K((V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2), & \text{for } V_{DS} \leq V_{DSAT} & - \text{linear} \\ 0.5K(V_{GS} - V_{TH})^2, & \text{for } V_{DS} \geq V_{DSAT} & - \text{saturation} \end{cases} \quad (1)$$

Due to the requirements of the electrical performance experiments, we referred a metal TO-257 packaging to design a four-pin lead frame. First, GaN HEMTs and low-voltage MOSFET were attached to the AlN DBC substrate. Next, these parts were attached to the four-pin lead frame. Colloidal silver was used as the attachment. Then, wire-bonding connects drain, gate, and source to the four pins separately as shown in Fig.3. There were two pins that connect to source and one of them acts as a Kelvin source. This connection reduced the parasitic inductance of GaN HEMT and make the measurement of electrical performance more accurately.⁽⁴⁾

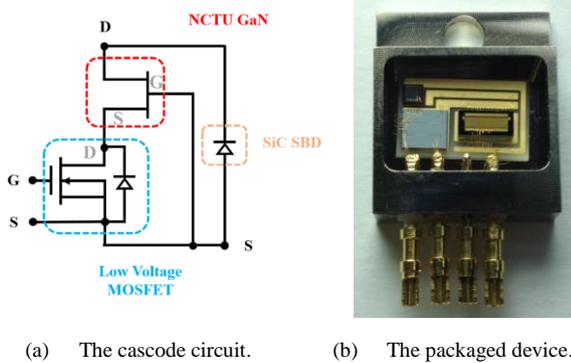


Fig. 2. The NCTU GaN HEMT is cascaded with a low-voltage MOSFET.

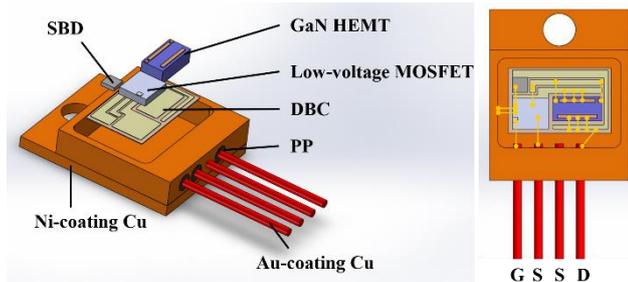


Fig. 3. Cascode GaN FET packaging.

4. Thermal Behavior Investigation

This packaging provides three ways to spread heat that is generated by the working device. First, most heat spreads directly to the bottom of the device. The DBC substrate and the lead frame forms the main access that spreads heat. Second, heat also dissipates from bonding wires. However, due to the small cross-section area of the wires, the amount of heat dissipation in this way is so small that can be ignored in simulation. Last, some heat spreads to the ambience from the device surface. Since there were three ways to dissipate heat, it seemed that the heat can be efficiently eliminated from device. In order to realize and improve thermal problem, we simulated the packaged devices to predict the thermal distribution and operated related experiments. The process and results are displayed as follow.

4.1 Simulation Approach

SolidWorks was used to build the model and Ansys Icepak supported simulating thermal distribution of the packaged cascode GaN FET. The heat is generated at the area that under drain-side gates.⁽⁵⁾ Therefore, we set the areas as heat sources, as shown in Fig.1(b). In addition, the scale discrepancy between thin films is large. Therefore, in the simulation, we simplified the device structure and the heat sources as shown in Fig.1(b). As it had been mentioned, the bonding wires were ignored in simulation because of the small amount of heat dissipation from this way. Due to the measurement requirement, the packaged GaN FET was put on a 50 °C board. The thermal conductivities of some used materials vary from temperature, so we refer to (6) to set the values displayed in Table 1. After setting the materials and meshing the model, the thermal distribution from Ansys Icepak simulation is shown in Fig.4.

Table 1 Thermal Conductivity of GaN, AlN, and Silicon

Temperature (K)	Thermal conductivity k (W/mK)		
	GaN	AlN	Si
300	210	285	148
400	145	195	98.9
500	110	150	76.2
600	90	115	61.9

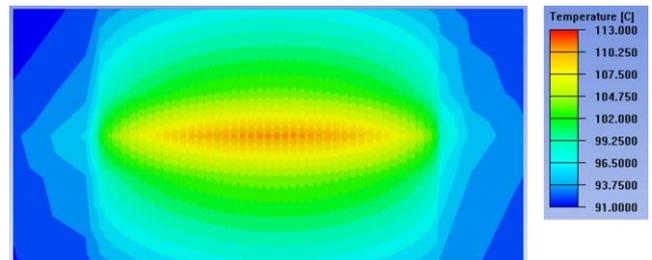


Fig. 4. Temperature distribution of GaN HEMT by simulation.

4.2 Measurement

To inspect the real thermal condition, the infrared (IR) thermal camera has been used to obtain the temperature distribution of the packaged device under different working conditions^(7, 8). Fig. 5 illustrates the GaN HEMT temperature distribution under DC current. The dotted-line rectangular is GaN HEMT. The peak temperature locates in the center as expected due to Joule heating. From the figure, we could also see that the temperature of connecting points between bonding wires and the chip is high as well, which indicated that bonding wires are not good at conducting heat. It verifies that ignoring bonding wires in simulation is reasonable. The peak value of the measurement will be discussed with the simulation results below.

4.3 Results

Figure 6 shows the simulation result of device surface temperature. It can be observed that the heat accumulated at the middle area of the device surface caused the peak temperature. When the power loss of GaN FET is 12 W, the device temperature would reach about 120 °C. There are 80 local maximum points which stand for 80 heat sources. The result of the measurement by using infrared thermography is shown in Fig.7. Due to the limit of resolution, we use the trend line to compare the results between simulation and measurement.⁽⁹⁾ From Fig.7, when the power loss of GaN FET is 12 W, the device temperature would reach about 118.7 °C. As the heat source locates near the middle point, its temperature is higher than the close one. This appearance indicates that it is more difficult for those heat sources to conduct heat to outside. As a result, the packaging material plays an important role in thermal management.

Figure 8 shows the peak value of device surface temperature by measurement and simulation. For power dissipation under 12 W, the peak temperature versus power dissipation curve is almost linear. As the power dissipation increases, the peak temperature gets higher. The results of experiments are in accordance with that of simulation which verify that the simulation is valid and can be used to predict the thermal distribution for higher operation power. However, devices has the limit of endurable heat, which means the power dissipation cannot be unlimited high. Therefore, to make the operation power much more higher, it is necessary to improve the packaging in the future.

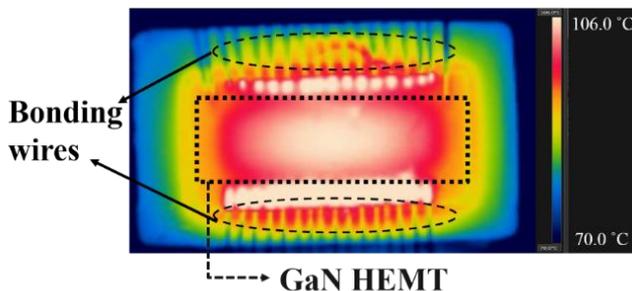


Fig. 5. The profile of GaN HEMT under infrared (IR) thermography microscope.

5. Conclusions

In order to use the high power device in a various application, we cascade the GaN HEMTs and low-voltage MOSFET. However, the thermal management is an extremely critical issue. Therefore, in this paper, thermal distribution was investigated by simulation approach and infrared thermography experiment. We showed the construction of the GaN HEMTs and the cascode way of GaN HEMT and the low-voltage MOSFET is displayed as

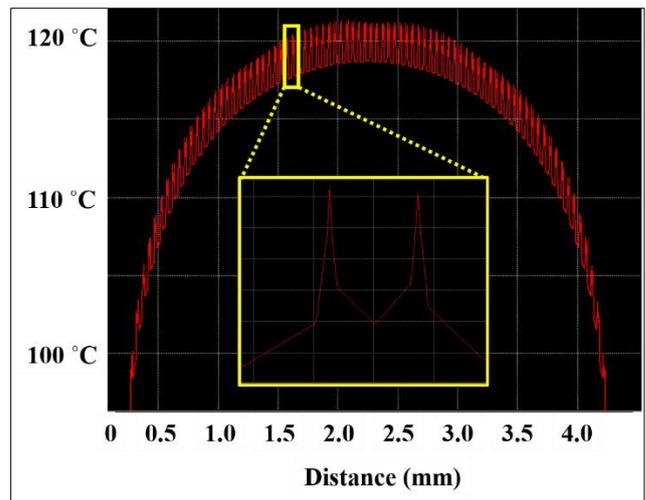


Fig. 6. Temperature curve of GaN HEMTs surface from simulation.

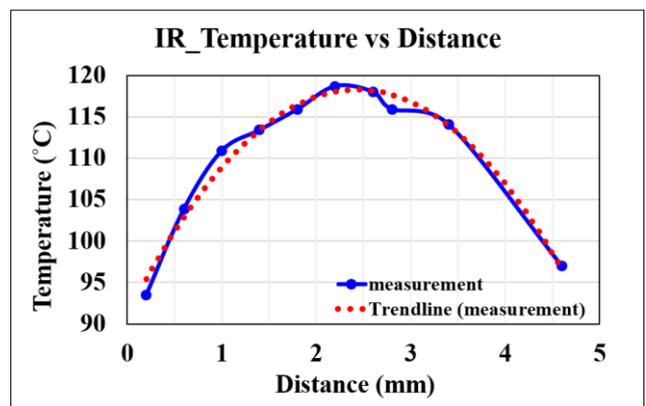


Fig. 7. Temperature curve of GaN HEMTs surface from infrared thermography.

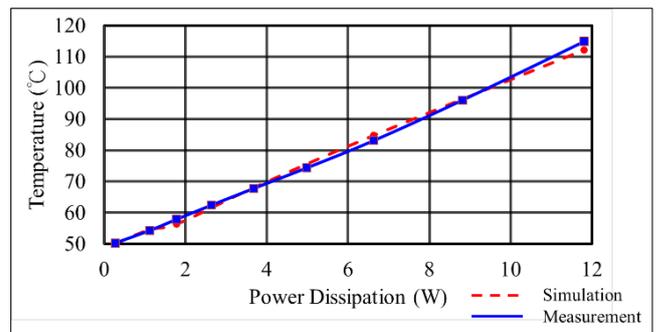


Fig. 8. Peak surface temperature of GaN HEMT by experiment and Ansys Icepak simulation.

well. Then, the Finite Element Method simulations and thermal measurement by using IR thermography microscope of thermal distribution of cascode GaN power devices were presented. The experimental results revealed that when the power loss of GaN FET is 12 W, the peak temperature is 118.7 °C. In the reasonable range, the peak temperature of device surface is linear to the power dissipation. Comparing the outcome, the measurement result is almost in accordance with that of simulation. Based on this simulation result, we can predict the sequence of peak temperature of operation cascode GaN FET and moreover, to see if the package can efficiently dissipate the heat.

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