A Free but Efficient Class AB Two-Stage Operational Amplifier

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Abstract — A low voltage two stage operational amplifier with class AB output stage is presented, featuring simplicity and efficiency. It has a large effective output current boosting factor (~50) and close to a factor 2 bandwidth enhancement. This is achieved at the expense of minimum additional circuitry with no extra static power dissipation. Experimental verification of the characteristics of the proposed circuit is provided.

I. INTRODUCTION

Two stage or Miller op-amps (Fig. 1a) are the natural choice for low-voltage applications with resistive loads that require rail-to-rail output swing. For high slew rate requirements a class AB output stage is commonly used in order to maintain low static power dissipation and with capability to generate output currents that are essentially larger than the output stage quiescent current $I_{Qout}^0$ [1]-[6]. Most class AB output stages can be considered implementations of the basic scheme shown in Fig. 1b where a floating battery with value $V_{bat}$ is connected between the gate terminals of the output transistors. This causes output voltage variations at node X to be transferred to node Y and leads to class AB operation. A very important practical aspect is the incorporation of a circuit to control $I_{Qout}^0$. This circuit is used to adapt the value of $V_{bat}$ so that the output current has the desired nominal value $I_{Qout}^0 = I_{DSQ} = I_{D} = I_{b}$ that remains independent of supply voltage variations and technology parameters. Another important aspect in modern CMOS technology is the low supply requirements for the class AB output stage and for the $I_{Qout}^0$ control circuitry. This is due to the fact that, in order to prevent gate oxide breakdown, supply voltages in modern deep sub-micrometer CMOS technology have essentially reduced values (~1.5V) while transistor threshold voltages have remained relatively large (~0.4V). This has led to decreased headroom for $V_{GS}$ variations and for the number of transistors that can be stacked between the supply rails. The difference between $V_{DD}$ and the minimum supply requirements of the output stage $V_{DDmin}$ usually determines the maximum drain-source voltage of the output transistors $V_{DSmax}$ and with this the maximum output current and slew rate enhancement factor $I_{Qout}^0 / I_{b} = (V_{DSmax}^0 / V_{DSQ})^2$ (where $V_{DSQ}$ is the quiescent drain-source voltage of $M_{6,7}$) and slew rate enhancement. Some common class AB schemes require a value $V_{DDmin}$ greater than two gate-source voltages (for example see [1]) and leave very small $V_{DD}$ headroom for output current enhancement in modern CMOS technology. Another important aspect for class AB circuits is that the additional current $I_{control}$ required by the quiescent current control circuitry adds to the static current consumption of the op-amp. This reduces the effective output current enhancement factor defined here by $EOCEF = I_{Qout}^0 / (2I_{b} + I_{control})$. This factor has a value $EOCEF=0.5$ for a class A op-amp with $I_{Qout}^0 = I_{b}$. Assume for example a circuit in a low voltage environment with $V_{DSmax} = 3V_{DSQ}$ so that $I_{Qout}^0 = 9I_{b}$ and a circuit (like that of [1]) with $I_{control} = 4I_{b}$. In this case $EOCEF=1.5$. In spite of the fact that the maximum output current is relatively large this corresponds to a modest $EOCEF$ value due to the additional current required by the quiescent current control circuitry. In this paper we report a two stage op-amp with a very compact implementation of a Class AB output stage. The proposed circuit has essentially the same static current requirements as the class A op-amp of Fig. 1a and the output stage has also the same minimum

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supply requirements: $V_{DD\min}=V_{GS6}+V_{SD2\text{sat}}+V_{SD5\text{sat}}$. This value is close to a transistor's threshold voltage. The here proposed op-amp shows enhanced phase margin and higher unity gain frequency than the conventional class A op-amp. For this reason we denote this circuit “Free class AB op-amp”. Experimental results of a fabricated test chip in 0.5μm CMOS technology are shown that verify the characteristics of the proposed structure.

II. PROPOSED CIRCUIT

Fig. 1c shows the proposed class AB op-amp. The only difference with respect to the conventional class A op-amp is that the output stage includes a large resistive element implemented using a minimum size diode connected PMOS transistor $M_{R\text{large}}$ and a small valued capacitor $C_{bat}$. Under quiescent conditions and since no DC current flows through $M_{R\text{large}}$, the voltage at the gate of M7 is the same as at the gate of M5 so that the quiescent current in M5 and M7 has the same value $I_b$. Transistor M6 is (as usual) sized with W/L dimensions twice as large as those of M3, M4 so that the quiescent current in M6 has also a value $I_b$. During dynamic operation, when the output of the op-amp is slewing, the voltage at node X is subject to a large change. Given that capacitor $C_{bat}$ can not discharge/charge rapidly through $M_{R\text{large}}$, it acts as a floating battery and transfers the voltage variations at node X to node Y. This provides class AB operation to the output stage.

A. Remarks

a) The value of $C_{bat}$ can be small. Its minimum value is determined by the parasitic capacitance $C_y$ at node Y (mainly the gate-source capacitance of M7) which forms a voltage divider with $C_{bat}$. This divider leads to attenuated voltage variations at node Y according to $V_y=V_xC_{bat}/(C_{bat}+C_y)$. A value of $C_{bat}>2C_y$ allows to transfer voltage variations from node X to node Y with relatively small attenuation. $C_{bat}$ can be implemented using the gate–source capacitance of an MOS transistor operating in triode mode.

b) Transistor $M_{R\text{large}}$ is intended to operate as a very large resistive element ($R_{large}$). It is implemented by using a minimum size diode connected PMOS transistor with source and substrate terminal interconnected. It can also be implemented using a transistor biased in subthreshold according to the biasing techniques described in [7]-[9]. It
operates in cutoff so that its ON resistance is extremely high and corresponds to the leakage resistance of the Nwell-source PN junction (this assuming Nwell technology).

c) Straightforward small-signal analysis of the circuit of Fig. 1c (with the capacitor $C_{bat}$ replaced by a short circuit and $M_{Rlarge}$ by an open circuit) shows that both the proposed class AB op-amp and the conventional class A op-amp have the same gain-bandwidth product $GB=g_{m1,2}/C_c$ while the high frequency output pole shifts from a value $\omega_{p2}=g_{m6}/C_L$ for the conventional op-amp to a value $\omega'_{p2}=(g_{m6}+g_{m7})/C_L$ for the proposed op-amp. This is approximately a factor 2 larger: $f'_{p2} \approx 2f_{p2}$. Since by maximizing $GB$ then $f_{p2}$ determines the unity gain frequency, the op-amp of Fig. 1c has higher unity gain frequency and improved phase margin than that of Fig. 1a. This is verified in the section on experimental results.

d) The output stage can operate with a minimum supply voltage close to a transistor’s threshold voltage: $V_{DDmin}=V_{GSS}+V_{SDSsat}+V_{SDSsat}$.

e) Due to class AB operation the proposed op-amp has approximately symmetrical slew rate. This as opposed to the conventional class-A op-amp that has nonsymmetrical slew rate: a large negative slew rate and a positive slew rate with value $SR=I_b/(C_c+C_L)$.

f) In some cases the op-amp slew rate might be limited by the internal node $X$ and by the maximum current that the first stage can deliver to $C_c$. In this case a low voltage class AB differential input stage as that reported in [10]-[11] can be used in order to achieve high slew rate at both the internal node and the output node of the op-amp.

g) The circuit shown in Fig. 1d is a fully differential version of the circuit of Fig. 1b. It features similar characteristics as the single ended version but, as it is expected from a fully differential circuit, it has higher power supply and common mode rejection ratios than the single ended version.

III. Experimental Results

A test chip prototype including the circuits of Fig. 1a and of Fig. 1c was fabricated in 0.5μm CMOS (AMI-MOSIS) technology with NMOS and PMOS threshold voltages of about 0.67V and −0.96V, respectively. Following transistor sizes (in μm) were used: M1,M2: 30/1, MB,M3,M6: 60/1, M4,M5: 10/1, M7: 20/1, M_{Rlarge}: 2/1, $C_{bat}$=3pF, $C_c$=1pF, $R_c$=10kΩ. Fig. 2 shows the microphotograph of the fabricated chip. The area of the class AB op-amp is 195x63 μm². The circuits were tested with a single supply $V_{DD}=2V$ a bias current $I_b=10μA$ and $C_L=25pF$. Fig. 3a and 3b shows the experimental input and output waveforms of the op-amps of Fig. 1a and 1c respectively for a 250kHz 1Vpp input square waveform. The corresponding measured slew rates were 0.410V/μs and 20V/μs. This corresponds to an effective slew rate enhancement factor of 50. The large overshoot in the response of the class A op-amp is an

Figure 2. Microphotograph of fabricated chip

Figure 3. Experimental pulse response input and output waveforms (a) Conventional class A op-amp (b) Free class AB op-amp
indication of its reduced phase margin with respect to the class AB op-amp.

Figure 4 shows the measured ac open loop response of the circuits of Figs. 1a and 1c. The measured unity gain frequencies are 6MHz and 11MHz respectively. The lower unity gain frequency for the class A op-amp is due the lower value of its output pole $f_{p2}$. Both op-amps can be seen to have the same $GB=11$MHz. The measured open loop DC gain was 45 dB in both cases. Measured values were in excellent agreement with simulations.

IV. CONCLUSIONS

A very simple implementation of a class AB two stage op-amp was introduced. It has essentially the same static power dissipation and circuit complexity as the conventional class A op-amp. As opposed to most previously reported class AB two stage op-amps the proposed circuit is characterized by a large effective output current enhancement factor. It also features enhanced bandwidth and phase margin and low supply requirements. The characteristics of the circuit have been experimentally verified.

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REFERENCES


