Decananometer Surrounding Gate Transistor (SGT) Scalability by Using an Intrinsically-Doped Body and Gate Work Function Engineering

Yasue YAMAMOTO†, Takeshi HIDAKA†††, Hiroki NAKAMURA††, Hiroshi SAKURABA††, and Fujio MASUOKA††, Members

SUMMARY This paper shows that the Surrounding Gate Transistor (SGT) can be scaled down to decananometer gate lengths by using an intrinsically-doped body and gate work function engineering. Strong gate controllability is an essential characteristic of the SGT. However, by using an intrinsically-doped body, the SGT can realize a higher carrier mobility and stronger gate controllability of the silicon body. Then, in order to adjust the threshold voltage, it is necessary to adopt gate work function engineering in which a metal or metal silicide gate is used. Using a three-dimensional (3D) device simulator, we analyze the short-channel effects and current characteristics of the SGT. We compare the device characteristics of the SGT to those of the Tri-gate transistor and Double-Gate (DG) MOSFET. When the silicon pillar diameter (or silicon body thickness) is 10 nm, the gate length is 20 nm, and the oxide thickness is 1 nm, the SGT shows a subthreshold swing of 63 mV/dec and a DIBL of -17 mV, whereas the Tri-gate transistor and the DG MOSFET show a subthreshold swing of 71 mV/dec and 77 mV/dec, respectively, and a DIBL of -47 mV and -75 mV, respectively. By adjusting the value of the gate work function, we define the off current at $V_G = 0$ V and $V_D = 1$ V. When the off current is set at 1 pA/µm, the SGT can realize a high on current of 1020 µA/µm at $V_G = 1$ V and $V_D = 1$ V. Moreover, the on current of the SGT is 21% larger than that of the Tri-gate transistor and 52% larger than that of the DG MOSFET. Therefore, the SGT can be scaled reliably toward the decananometer gate length for high-speed and low-power ULSI.

key words: Surrounding Gate Transistor (SGT), scaling, intrinsic channel, gate work function engineering

1. Introduction

Due to the growing demand for high-performance and low-power ULSI, MOS transistors with sub-20 nm gate lengths are required [1]. As a result, as we continue to scale down CMOS devices, new compact three-dimensionally structured MOS transistors with an excellent tolerance to short-channel effects are needed.

A promising candidate is the Surrounding Gate Transistor (SGT) [2]. The SGT, whose source, gate, and drain are arranged vertically with respect to the silicon substrate, uses the sidewalls of the silicon pillar as the channel region. The pillar sidewalls are also surrounded by an oxide layer and the gate electrode. The SGT has excellent features such as steep cut-off characteristics, small substrate bias effects, and excellent channel reliability, which is a direct result of the full depletion of the transistor body caused by the strong controllability of the surrounding gate structure. Many other non-classical multi-gate transistors have also been proposed as the potential candidates, such as GAA [3], [4], TRI [5], FinFET [6], VRG [7], Tri-gate [8], and Pi-gate device/structure [9], [10].

The SGT has received much attention for future use in DRAM, Flash EEPROM, and conventional CMOS applications [2], [11], [12]. However, by applying conventional CMOS scaling methods to the nanometer-scale SGT, a higher body impurity concentration would be necessary, which would then increase the threshold voltage. This unfortunately leads to the following additional problems: obtaining the fully-depleted condition becomes more difficult, the carrier mobility is decreased, and finally, threshold voltage fluctuations due to statistical fluctuation of dopant atoms within the channel would become more pronounced [13].

However, when an intrinsically-doped channel is used, the SGT can suppress the threshold voltage fluctuations and the decrease in the carrier mobility. Moreover, the intrinsically-doped SGT will have higher gate controllability of the silicon body. Then, in order to define the threshold voltage, the gate work function will need to be modified by using metal or metal silicide gate. In this paper, we analyze the scalability of the SGT defined by using an intrinsically-doped silicon pillar and gate work function engineering. We compare the device characteristics of the SGT to those of the Tri-gate transistor and DG MOSFET [14]. In Sect. 2, we clarify the operation mechanism of the ideal fully-depleted SGT using an intrinsic silicon pillar. In Sect. 3, the device characteristics of the SGT are compared with those of the Tri-gate transistor and DG MOSFET. The three-dimensional (3D) device simulation conditions used to investigate the device characteristics are explained. In addition, the short-channel characteristics, optimized gate work function and the $I_{on}$-$I_{off}$ characteristics are shown for each device. In Sect. 4, we present our conclusions.

2. Operation Mechanism

First, the details of the SGT structure are described. Fig-
Figure 1(a) shows a schematic view of the SGT where $R$ is the silicon pillar radius, $L$ is the gate length, and $W_{SGT}$ is the gate width. The source, gate, and drain of the SGT are vertically arranged with respect to the silicon substrate. The gate electrode completely surrounds the silicon pillar, forming a channel region along the pillar sidewalls. Since the pillar is cylindrical, the entire channel has a uniform curvature and no “corner effects” occur within the structure. Therefore, in the SGT, we need not consider the effect of the corner. The body region in the silicon pillar is intrinsically-doped because the addition of dopants would lead to unacceptable statistical fluctuations of the threshold voltage and increased surface scattering along the Si-$\text{SiO}_2$ interface which reduces the carrier mobility. The gate material is metal or metal silicide which has a proper work function to suppress the off current and to adjust the threshold voltage.

Figure 1 shows the two other non-classical MOS transistor structures that will be compared to the SGT. Figure 1(b) shows a schematic view of the Tri-gate transistor where $t_{Si}$ is the silicon body thickness, $W_{Si}$ is the silicon body width, and $W_{Tri-gate}$ is the gate width. Figure 1(c) shows a schematic view of the DG MOSFET where $W_{DG}$ is the gate width.

Second, the operation mechanism of the intrinsically-doped SGT is explained. Figure 2 shows the energy band diagrams of the intrinsically-doped SGT where $E_{FM}$ is the Fermi level of the gate, $E_c$ is the conduction band energy in the body region, $E_i$ is the intrinsic Fermi level in the body region, and $E_v$ is the valence band energy in the body region. In this figure the gate work function is at midgap. At zero gate voltage, the intrinsic channel and hence the bands remain flat throughout the silicon pillar as shown by the dotted lines in Fig. 2(a). When a positive gate voltage is applied, the potential in the body decreases, and the potential barrier between the body and the source becomes smaller, causing carriers to be injected from the source. However, the carrier density is too small to create an electric field in the gate oxide. Therefore, the entire potential in the body region is decreased by an amount equal to that of the applied gate voltage, keeping flat band as shown by the solid lines in Fig. 2(a). As the applied voltage is further increased, the injected carrier density becomes large enough to create an electric field in the gate oxide along the direction of accelerating negative charge toward the metal electrode indicating that the potential distribution in the body is determined by the amount of carriers injected from the source. Therefore, the potential in the body region bends downward near the surface as shown in Fig. 2(b). The curved shape
of the potential in the gate oxide is due to an electric field concentration effect attributed to the cylindrical structure. The range of gate voltage corresponding to Fig. 2(a) will be called Region I and the range of gate voltages corresponding to Fig. 2(b) will be called Region II. In Region I, the SGT has higher gate controllability of the silicon body.

The above formation mechanism of band diagrams will be explained in more detail. Figure 3 shows the 3D simulation [15] results of the intrinsically-doped SGT with $2R = 10$ nm, $L = 200$ nm, and $t_{ox} = 1$ nm where $t_{ox}$ is the gate oxide thickness. Poisson’s equation and the drift-diffusion transport equation were solved with the drain voltage ($V_D$) equal to 0.05 V, the source voltage ($V_S$) equal to 0 V, and the gate voltage ($V_G$) variable.

Figure 3(a) shows the dependence of $\psi_{\text{surface}} - V_G$ and $\psi_{\text{center}} - V_G$ on $V_G$ for the intrinsically-doped SGT with a midgap gate work function where $\psi_{\text{surface}}$ is the potential at the surface and $\psi_{\text{center}}$ is the potential at the body center. The device can be analyzed by looking at two specific regions of operation. Region I is defined as the range of the gate voltage region when $\psi_{\text{surface}} - V_G = \psi_{\text{center}} - V_G = 0$. In this region, as $V_G$ increases, $\psi_{\text{surface}}$ and $\psi_{\text{center}}$ follow $V_G$ and hence $\psi_{\text{surface}} = \psi_{\text{center}} = V_G$. Region II is defined as the range of the gate voltage region when $\psi_{\text{center}} - V_G > \psi_{\text{surface}} - V_G > 0$. In this region, as $V_G$ increases, $\psi_{\text{surface}}$ and $\psi_{\text{center}}$ do not follow $V_G$ because $\psi_{\text{center}}$ increases at a smaller rate than $\psi_{\text{surface}}$ and hence $V_G > \psi_{\text{surface}} > \psi_{\text{center}}$.

Figure 3(b) shows the potential distribution ($\psi - V_G$) along the direction of the Source-Drain (point A to B) and MOS (point B to C) within the body region at $V_G = 0$ V, 0.4 V, 0.6 V, and 0.7 V. At $V_G = 0$ V, 0.4 V (Region I), in the region proceeding within 10 nm from point A, due to the diffusion potential, $\psi$ is larger than $V_G$. From this region to point C, $\psi$ is equal to $V_G$. At $V_G = 0.6$ V, 0.7 V (Region II), in the region proceeding within 10 nm from the point A, due to the diffusion potential, $\psi - V_G$ is larger than that of the other positions. From this region to point B, $\psi - V_G$ is the essentially the same value. From point B to point C, $\psi - V_G$ is smaller when closer to the surface.

Figure 3(c) shows constant potential contours at a vertical cross section along the center in the silicon pillar at $V_G = 0.4$ V and 0.7 V. At $V_G = 0.4$ V (Region I), the potential in the body is equal to the gate voltage, and no electric field in the gate oxide has not arisen. At $V_G = 0.7$ V (Region II), the potential in the body are smaller than the gate voltage, and an electric field in the gate oxide exists.

These results show that the intrinsically-doped SGT has high gate controllability of the silicon body, and that they are consistent with the band diagrams shown in Fig. 2. Similarly, the operation mechanism just described can also be applied to an SGT with the lightly-doped silicon body since the number of impurity atoms is negligible.

### 3. Device Characteristics

#### 3.1 3D Device Simulation Conditions

The 3D device simulator [15] that we used takes into account a conservative Boltzmann carrier statistics model, Yamaguchi mobility model, and Shockley-Reed-Hall recombination model.
Table 1: Normalized channel current of NMOS, \( I_{on}(211) / I_{on}(100), I_{on}(322) / I_{on}(100), I_{on}(111) / I_{on}(100) \), in the pentode region as a function of effective channel length with Si surface orientation as a parameter from Ref. [16], and this work.

<table>
<thead>
<tr>
<th>( t_{ox} = 15 \text{ nm} )</th>
<th>( V_{GS} - V_{th} = 4 \text{ V} )</th>
<th>( V_{DS} = 5 \text{ V} )</th>
<th>( E_{SD} )</th>
<th>Normalized Channel Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0.5 \mu m )</td>
<td>( 5 \times 10^2 )</td>
<td>0.7</td>
<td>0.65</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Table 1 shows normalized channel current of NMOS, \( I_{on}(211) / I_{on}(100), I_{on}(322) / I_{on}(100), I_{on}(111) / I_{on}(100) \), in the pentode region as a function of effective channel length with Si surface orientation as a parameter from Ref. [16], and this work.

From Table 1, we can get that the channel currents do not depend on the surface orientation, when the average electric field from the source to drain \( E_{SD} \) is \( 1 \times 10^5 \text{ V/cm} \), and also that the carrier mobility do not depend on the surface orientation when \( E_{SD} \) is \( 1 \times 10^5 \text{ V/cm} \). Since \( E_{SD} \) in this work is \( 5 \times 10^5 \text{ V/cm} \) which is five times larger than that in Ref. [16], we can calculate the current of all orientation by using the condition that the carrier mobility of all orientation is the same value.

The simulated structures also have a uniform impurity concentration in the body region and in the source/drain regions. The diffusion layer impurity concentration in the source/drain regions are \( 10^{20} \text{ cm}^{-3} \) and the impurity concentration in the body region is zero. The diffusion layer within our simulated structures is made to have the same source/drain junction resistance. Quantum charge confinement effects were not considered in this study. As shown in Fig. 2, due to the intrinsically-doped body, the band bending near the gate oxide is small, indicating that quantum charge confinement effects along the Si-SiO\(_2\) interface are insignificant. For an SGT with an intrinsically-doped body at \( 2R = 10 \text{ nm}, t_{ox} = 5 \text{ nm}, V_{GS} = 1 \text{ V}, \) and \( V_{DS} = 0.05 \text{ V}, \) quantum mechanical effects result in drain currents that are 10\% less than those produced by the classical model [17]. A gate work function of 4.71 eV was used where 4.71 eV corresponds to the middle of the silicon band gap (midgap). The equivalent gate oxide thickness was set at 1 nm.

We simulated 11 kinds of devices with gate lengths varying from 10 nm to 200 nm and with silicon pillar diameters (or silicon body thicknesses) of 5 nm, 10 nm, and 25 nm.

3.2 Suppression of Short-Channel Effects

Figure 4 shows the dependence of the threshold voltage shift (\( \Delta V_{th} \)) on the gate length for the SGT, Tri-gate transistor, and DG MOSFET. The threshold voltage is defined as the gate voltage when the drain current per unit gate width equals to 0.1 \( \mu \text{A/\mu m} \). The threshold voltage shift is hence defined as the threshold voltage measured at \( V_D = 1.0 \text{ V} \) at any gate length minus the threshold voltage at \( L = 200 \text{ nm} \). It is calculated for \( W_{Tri} = 3t_{si} \) \( (t_{si} = W_{si}) \).

Figure 5 shows the dependence of the subthreshold
Dependence of the subthreshold swing on the gate length. Figure 6 shows the dependence of the drain-induced-barrier-lowering (DIBL) on the gate length. DIBL is defined as the threshold voltage at $V_D = 1.0$ V minus the threshold voltage at $V_D = 0.05$ V for any gate length. For $2R = t_{si} = 10$ nm, $L = 20$ nm, and $t_{ox} = 1$ nm, the SGT shows an excellent subthreshold swing of 63 mV/dec and a DIBL of $-17$ mV, whereas the Tri-gate transistor and the DG MOSFET show a subthreshold swing of 71 mV/dec and 77 mV/dec, respectively, and a DIBL of $-47$ mV and $-75$ mV, respectively. If we define acceptable values of the subthreshold swing and the DIBL as 65 mV/dec and $-25$ mV, respectively, it is found that the minimum gate lengths ($L_{min}$) of the SGT, Tri-gate transistor, and DG MOSFET are 20 nm, 25 nm, and 30 nm, respectively, at $2R = t_{si} = 10$ nm. Therefore, the SGT can suppress short-channel effects more effectively than the other non-classical MOSFET devices.

3.3 Optimized Gate Work Function for the 20 nm Gate Length

By adjusting the gate work function [18], we define the off current ($I_{off}$). Figure 7 shows the value of the gate work function required to design the $I_{off}$ of the SGT, Tri-gate transistor, and DG MOSFET. $I_{off}$ is defined as the drain current per unit gate width at $V_{G} = 0$ V and $V_D = 1$ V. For an n-type SGT, a gate work function from 4.35 eV to 4.73 eV is needed to produce a desired $I_{off}$ or threshold voltage. However, for an n-type Tri-gate transistor and an n-type DG MOSFET, a gate work function from 4.40 eV to 4.82 eV and a gate work function from 4.45 eV to 4.91 eV are needed, respectively. Thus, the SGT needs a lower gate work function value to get at the same off current.
Fig. 8 Electrical characteristics.

3.4 Drive Current and Standby Leakage Current

Figures 8(a) and (b) show $I_D$-$V_G$ characteristics of the SGT, Tri-gate transistor, and DG MOSFET. The on current ($I_{on}$) is defined as the drain current per unit gate width at $V_G = V_D = 1$ V. The off current ($I_{off}$) is defined as the drain current per unit gate width at $V_G = 0$ V and $V_D = 1$ V, and is controlled by adjusting the value of the gate work function. $I_{off}$ was chosen as 1 nA/µm. $I_{on}$ of the SGT is 9% larger than that of the Tri-gate transistor and 24% larger than that of the DG MOSFET. The 20 nm SGT exhibits higher current drivability when compared to the other non-classical MOS devices due to the fact that the SGT produces an ideal sub-threshold swing. In Sect. 3.2, the SGT shows a subthreshold swing of 63 mV/dec, whereas the Tri-gate transistor and the DG MOSFET show a subthreshold swing of 70 mV/dec and 77 mV/dec, respectively.

Figure 8(c) shows the $I_{on}$-$I_{off}$ characteristics of the SGT, Tri-gate transistor, and DG MOSFET. At $I_{off} = 1$ pA/µm, the SGT can realize a high $I_{on}$ value of 1020 µA/µm. In addition, $I_{on}$ of the SGT is 21% larger than that of the Tri-gate transistor and 52% larger than that of the DG MOSFET. However, the difference of $I_{on}$ among the SGT, Tri-gate transistor, and DG MOSFET decreases as $I_{off}$ increases. When $I_{off}$ is set at 0.1 µA/µm, $I_{on}$ of the SGT is only 3% larger than that of the Tri-gate transistor and 12% larger than that of the DG MOSFET. This is resulting from the fact that the ideal subthreshold swing is not used when a high $I_{off}$ is set. Thus, it is very important to design a lower $I_{off}$ in order to use the ideal subthreshold swing of the SGT.

In Table 2, the propagation delay ($\tau_{pd} = CV/I$) of the SGT and DG MOSFET at $I_{off} = 1$ nA is shown. The capacitance ($C$) is defined as the ideal gate capacitance per micron device width, in inversion. $C$ of the SGT and DG MOSFET can be calculated by Eq. (1) and Eq. (2).

$$C_{SGT} = \frac{\varepsilon_{ox}}{R \cdot \ln(1 + \frac{I_{ox}}{I_{off}})} \cdot L = 7.57 \cdot 10^{-16} \text{ [F/µm]}$$  \hspace{1cm} (1)$$

$$C_{DG \ MOSFET} = \frac{\varepsilon_{ox}}{I_{ox}} \cdot L = 6.9 \cdot 10^{-16} \text{ [F/µm]}$$  \hspace{1cm} (2)$$

The current is defined as the drain current per unit gate width at $V_G = V_D = 1$ V. The voltage is defined $V_D = 1$ V. $\tau_{pd}$ of the SGT is 10% less than that of the DG MOSFET.

4. Conclusion

In this paper we have demonstrated that the SGT will be able to realize a reliable scaling toward the decanometer gate length. In order to suppress the threshold voltage fluctuations and the decrease in carrier mobility, the silicon pillar channel was intrinsically-doped. The technique of gate work function engineering was adopted for adjusting the threshold voltage. We described the operation mechanism of the intrinsically-doped SGT and analyzed the short-channel effects and current characteristics

<table>
<thead>
<tr>
<th>Table 2</th>
<th>Propagation delay ($\tau = CV/I$) of the SGT and DG MOSFET.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$C_{on}$ [F/µm]</td>
</tr>
<tr>
<td>SGT</td>
<td>$7.57 \times 10^{-16}$</td>
</tr>
<tr>
<td>DG MOSFET</td>
<td>$6.90 \times 10^{-16}$</td>
</tr>
</tbody>
</table>
by using a three-dimensional device simulator. We compared the device characteristics of the SGT to that of the Tri-gate transistor and DG MOSFET. For $2R = t_{si} = 10 \text{nm}$, $L = 20 \text{nm}$, and $t_{ox} = 1 \text{nm}$, the SGT showed a subthreshold swing of $63 \text{mV/dec}$ and a DIBL of $17 \text{mV}$, whereas the Tri-gate transistor and the DG MOSFET showed a subthreshold swing of $71 \text{mV/dec}$ and $77 \text{mV/dec}$, respectively, and a DIBL of $-47 \text{mV}$ and $-75 \text{mV}$, respectively. By adjusting the value of the gate work function, we defined $I_{on}$ at $V_G = 0 \text{V}$ and $V_D = 1 \text{V}$. At $I_{off} = 1 \text{pA/\mu m}$, the SGT can realize a high on current of $1020 \mu A/\mu m$ at $V_G = 1 \text{V}$ and $V_D = 1 \text{V}$. Moreover, $I_{on}$ of the SGT is 21% larger than that of the Tri-gate transistor and 52% larger than that of the DG MOSFET. Therefore, the SGT can be reliability scaled down toward the decananometer gate length for high-speed and low-power ULSI.

**References**


Yasue Yamamoto was born on June 13, 1978, in Miyagi, Japan. He received the B.S. degree in applied physics and M.S. degree in electrical engineering from Tohoku University, Sendai, Japan, in 2002 and 2004, respectively. In 2004, he joined the System LSI Technology Development Center, Corporate System LSI Development Division, Semiconductor Company, Matsushita Electric Industrial Company, Ltd., Kyoto, Japan. He is currently working on the circuit design of embedded Nonvolatile Memories. His research interests include emerging memories and non-classical multi-gate transistors, such as SGT, Tri-gate transistor, and FinFET. Mr. Yamamoto is a member of the IEEE Solid State Circuits Society, the IEEE Electron Device Society.

Takeshi Hidaka was born on November 13, 1979, in Miyazaki, Japan. He received the B.E. degree in faculty of economics from Keio University in 2003, Tokyo, Japan, and M.E. degree degrees in electrical engineering from Tohoku University, Sendai, Japan, in 2005.

Hiroki Nakamura was born in Saitama, Japan, in 1976. He received his B.E. and M.E. and Ph.D. degrees in electrical engineering from Tohoku University in 1999, 2001 and 2004 respectively. In 2004, he has been a research associate of the Research Institute of Electrical Communication, Tohoku University. He is research interests include the low power and high density DRAM, especially NAND-type DRAM-on-SGT.
Hiroshi Sakuraba was born on November 5, 1961, in Akita, Japan. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tohoku University, Sendai, Japan, in 1987, 1989, and 1992, respectively. Since 1992, he had been a Research Associate of the Faculty of Engineering of Tohoku University, where he had been engaged in the research of the surface reaction mechanism of the semiconductor crystal growth. In 1996, he joined the Research Institute of Electrical Communication, Tohoku University. His current concern is the device and process technology of ULSI.

Fujio Masuoka was born on May 8, 1943, in Gunma, Japan. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tohoku University in 1966, 1968, and 1971, respectively. In 1971, he joined Toshiba Research and Development Center, Kawasaki, Japan, where, in 1972, he developed stacked gate avalanche injection-type MOS read-only memory (SAMOS) for the first time. SAMOS is the origin of current EPROM and Flash Memory. In 1976, he developed dynamic memory cell with double poly-Si structure. In 1977, he moved to Toshiba Semiconductor Business Division, where he developed 1-Mb DRAM, and in 1980, he applied a flash memory patent for the first time. In 1984, he presented flash memory for the first time at IEDM and, in 1985, at ISSCC. In 1987, he returned to Toshiba Research and Development Center, where he began to develop NAND structured Flash memory, which was presented in 1987 at IEDM. He moved to Tohoku University, Sendai, Japan, as a Professor in 1994. He has 170 registered patents in the United States, Germany, France, and Great Britain, 100 registered patents in Japan, and 71 pending patents. He authored or coauthored approximately 150 papers. Dr. Masuoka received the “IEEE Morris N. Liebmann Memorial Award,” in 1997 and The Ichimura Prizes in Industry (which is the main prize for the development of Flash Memory) in 2000.