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Under-gate defect formation in Ni-gate AlGaN/GaN high electron mobility transistors

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ABSTRACT

AlGaN/GaN high electron mobility transistors (HEMTs) represent a rapidly maturing technology plagued by reliability issues which are not well understood. One such issue is the relationship between gate leakage and the formation of reaction-based defects at the interface between the gate metal and the underlying epitaxial semiconductor layers. Here, the combination of chemical etching-based deprocessing and top-down scanning electron microscopy (SEM) to identify and quantify defects formed between the gate and the epitaxial layers of HEMTs with Ni gates is presented. This approach is used to demonstrate a direct relationship between gate leakage current density during off-state stressing and the percentage of gate contact area consumed by reaction-based defects in HEMTs with 100 nm and 1.0 μm gate lengths.
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1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) represent a rapidly maturing technology [1,2] which has been leveraged to great effect in circuit applications where high frequency [3–5], high power signals [6,7], and high operating temperatures are required [8,9]. HEMTs are effective in these applications due to the wide bandgaps of the materials and the formation of a two-dimensional electron gas (2DEG) at the AlGaN/GaN interface [10]. This 2DEG is a sheet of charge, which is formed as a consequence of polarization imbalances between the AlGaN and GaN material, leading to carrier concentrations in the HEMT structure which are uncharacteristically large for any wide-bandgap semiconductor. Combined with the high electron mobility of GaN, this large carrier concentration results in a high-conductivity channel for charge transfer [11]. A gate electrode modulates the 2DEG, which is capable of electrostatically "pinching off" the conducting channel. Typically, this gate electrode is comprised of a thin liner layer of metal such as Pt [12,13], Ir [14], Cu [15–17], and Ni [18] (most commonly) with a thicker Au layer on top of the liner layer to aid in conduction. The gate electrode is separated from the 2DEG layer by a layer of AlGaN; this layer reduces gate leakage by forming a Schottky contact with the gate and by possessing a wider bandgap than the underlying GaN layer to reduce the likelihood of thermally-driven electron conduction between the 2DEG and the gate [2].

One of the major challenges associated with AlGaN/GaN HEMTs is the issue of reliability [19,20]. In particular, changes to the physical structure of the HEMT during stressing can induce conditions, which could lead to additional leakage current through the gate electrode [11,21]. Several groups have reported a reaction between the Ni liner layer and the AlGaN epitaxial layer observed via high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) [21,22]. When stressing occurs in N_2 ambients, this reaction manifests itself as "sinking" whereby the Ni layer appears to diffuse down and consume the underlying AlGaN layer and make electrical contact to the 2DEG. However, when stressing occurs in O_2 or air, the O_2 present reacts with the Ni/AlGaN mixture to form an oxidized Ni phase as confirmed using HAADF-STEM combined with electron energy loss spectroscopy [23].

In contrast, HEMTs utilizing a Pt liner layer did not show the same gate sinking-related defects, which may be due to reduced reactivity of Pt in comparison to Ni [21,24]. However, recent work in HEMTs with Pt gates where top-down scanning electron microscopy (SEM) analysis was performed on devices with metallization and passivation layers removed via chemical etching (deprocessed) did demonstrate that high electric fields present at the drain side of the gate electrode can lead to a piezoelectric strain-induced cracking of the underlying AlGaN material [11]; this allows the Pt liner layer to seep into the resulting crack and make electrical contact to the 2DEG. Moreover, the gate leakage current appears to increase with increasing total area consumed by defects [25]. A similar combination of chemical etching to deprocess devices combined with top-down SEM has not yet been conducted in HEMTs with Ni gates, but such an analysis may be important considering the apparent differences in failure mechanisms compared to devices with Pt gates. The purpose of this work is to quantify the presence of under-gate defects in AlGaN/GaN HEMTs with Ni gates using a

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combination of chemical etching-based deprocessing and top-down SEM.

2. Experimental

For each device, an Fe-doped GaN buffer layer was grown on a 4H-SiC substrate via metal–organic chemical vapor deposition to a thickness of ~2.25 μm, forming a reasonably stress-free layer and trapping most crystallographic defects formed in the GaN buffer layer [26]. A ~20 nm-thick layer of $Al_{0.28}Ga_{0.72}N$ with an n-type GaN capping layer were grown on the epitaxial GaN layer via molecular beam epitaxy [27]; the n-type GaN cap was incorporated to reduce current collapse during biasing [28,29]. Further details regarding semiconductor epilayer growth are described elsewhere [30–32]. Ohmic contacts consisting of Ti/Al/Ni/Au were deposited and patterned on the surface and annealed for 30 s at 850 °C to improve conductivity [12]. The gate contact consisted of a ~20 nm-thick Ni liner layer deposited directly on the epitaxial layers with a thicker layer of Au; devices with gate lengths on the order of ~100 nm and ~1.0 μm were used in this work. In both cases, T-type gate structures were used [29]. Finally, a ~100 nm-thick SiN_x passivation layer was deposited via plasma enhanced chemical vapor deposition. More details regarding the device fabrication process are described in Johnson et al. in Ref. [18].

Stressing of devices was performed in air ambient using a Tektronix 370A curve tracer and an HP 4156 parameter analyzer. The devices were placed in a deeply pinched-off mode with gate voltage $V_G = -8$ V to ensure minimal current flow between the source and drain electrodes as well as to maximize the field present between the gate and the 2DEG. The drain voltage was then increased in 1 V increments every minute until the drain voltage exceeded 70 V or the device experienced catastrophic failure due to drain to gate shorting, which varied between 0.5 and 1.0 mA depending upon the device being stressed. Measurement of the increasing off current passing through the gate electrode was performed at the end of each stepped stress measurement. This measurement occurred over a 1 min time period, ensuring that the stressing was performed at a duty cycle of approximately 50%.

Fig. 1 demonstrates the device characteristics of a representative device both before and after the stepped stressing. Fig. 1a shows a plot of drain-to-source current (I_{DS}) versus applied drain-to-source voltage (V_{DS}) and indicates that the saturation I_{DS} of the representative device decreased for all values of applied V_G after stepped stressing beyond the critical voltage. Fig. 1b shows a plot of I_{DS} versus V_G and demonstrates that the threshold voltage at which the device shifted from a pinched off mode into its "on" state increased after stressing. Finally, Fig. 1c presents a plot of gate current (I_G) as a function of applied gate-to-source voltage (V_{GS}). A substantial increase was observed in the reverse-biased leakage current through the Schottky gate electrode after stressing. The degradation of the device characteristics post-stressing is typical of cases where high fields lead to defect formation under the gate electrode [19].

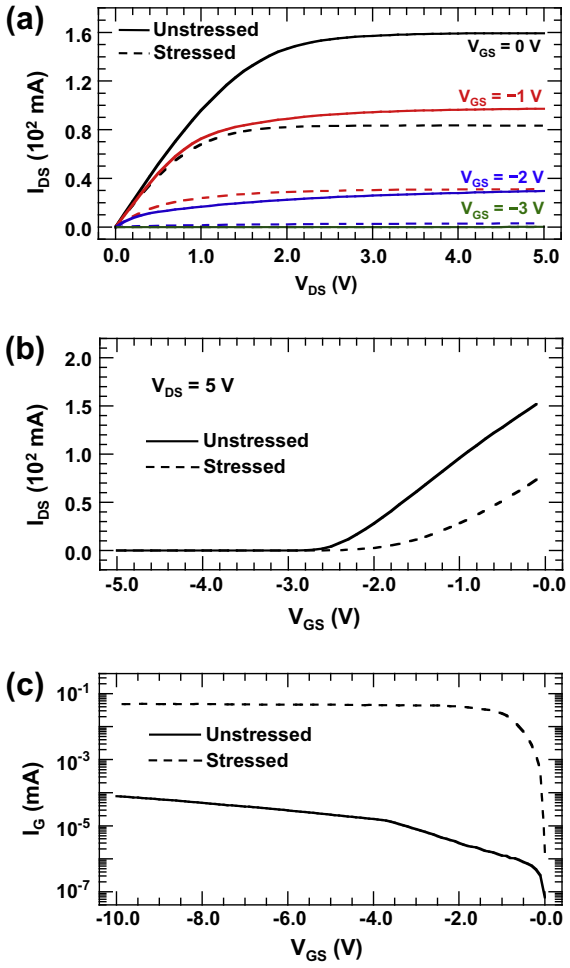

Fig. 1. Representative device characteristics of AlGaN/GaN HEMTs used in this work. (a) The I_{DS} versus V_{DS} family of curves both before and after stepped stressing to failure with V_G variable from 0 to −3 V. Stepped stressing appears to dramatically reduce the saturation I_{DS} in the device. (b) I_{DS} versus V_{GS} before and after stepped stressing to failure with V_{DS} = 5 V. Stepped stressing appears to shift the threshold voltage of the device to higher values of V_G. (c) I_G versus V_{GS} of the Schottky gate both before and after stepped stressing to failure. Stepped stressing appears to increase the reverse biased leakage current by over two orders of magnitude.

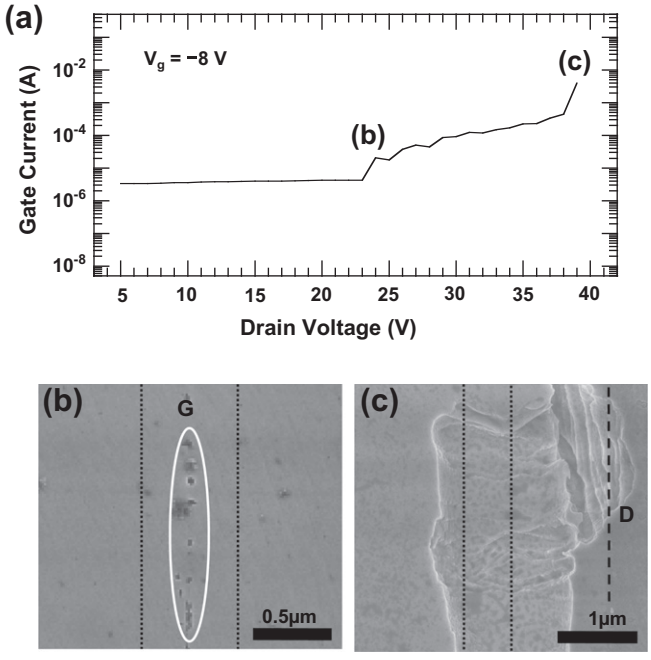

Fig. 2. (a) Typical gate current versus drain voltage behavior (gate voltage V_G = −8 V) for AlGaN/GaN HEMTs studied in this work (μm-scale gate device). (b) Top-down SEM micrograph of the near-gate region of a deprocessed device stressed to the point where a sudden increase in gate current was observed showing the generation of under-gate defects (drain voltage ~23 V as indicated in part (a)). (c) Top-down SEM micrograph of a device stressed to the point of failure such that the gate and drain catastrophically shorted out (drain voltage ~38 V as indicated in part (a)). The approximate locations of the edges of the gate (G) and source (S) metalization prior to deprocessing are indicated in parts (b) and (c) (dotted lines).

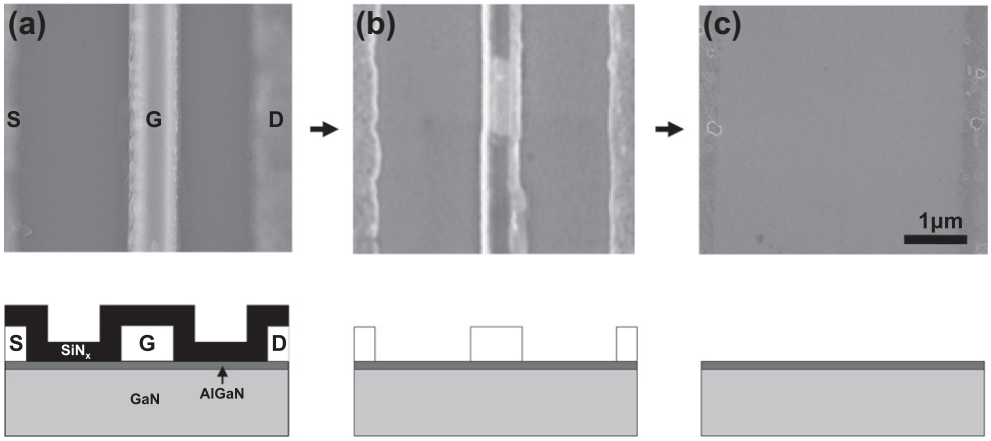

Fig. 3. Top-down SEM micrographs with corresponding schematic cross-sectional representations (not to scale) showing the etching strategy employed for deprocessing AlGaN/GaN HEMTs to allow quantitative under-gate defect analysis: (a) prior to deprocessing, (b) etched for 10 min with BOE, and (c) subsequently etched for 18 h with TFAC, etched for 10 min in BOE for a second time, and cleaned ultrasonically for 20 min in methanol. The locations of the source (S), gate (G), and drain (D) contacts for each image are indicated.

Typical gate current versus drain voltage behavior for a device with 1.0 μm gate length is presented in Fig. 2a. It is evident that the gate current increased significantly at a threshold drain voltage of ~22 V and continued to gradually increase with increasing drain voltage. A sudden onset of high current flow at a drain voltage of ~38 V was observed which was attributed to catastrophic shorting. No device failure was experienced during the gradual increase in gate current beyond the critical voltage. Furthermore, no observed recovery of the degraded transfer characteristics was observed. Representative top-down SEM images of the near-gate regions of deprocessed devices stressed to the threshold voltage and at the point of catastrophic failure are presented in Fig. 1b and c, respectively.

A deprocessing method combining chemical etching to remove the metallization and passivation layers (deprocessing) with subsequent top-down SEM was used to observe the presence of reaction-based defects under the gate area of devices with 100 nm and 1.0 μm gate lengths. This deprocessing method is similar to methods described previously for HEMTs with Pt gates [25], but utilizes a different etch chemistry more selective to AlGaN as well as a final cleaning method to improve the quality of the sample surface as presented in Fig. 2. The samples were first exposed to a 6:1 NH_4F:HF solution (buffered oxide etchant) for 10 min to induce thorough removal of the SiN_x passivation. Subsequently, the samples were exposed to a KI- and FeCN-based solution (TFAC, available through Transene Company, Incorporated) for 18 h; the TFAC etchant is more benign to the AlGaN/GaN epitaxial layers than the Aqua Regia chemistry used in previous studies [25]. Following the removal of the gate metal layers, the sample was exposed to a second etch in buffered oxide etchant for 5 min to remove any remnant SiN_x which may have been protected by the gate prior to exposure to the TFAC etchant. A final ultrasonic clean was performed in methanol for 20 min to remove any remnant contaminants which may have deposited on the sample surface during deprocessing. This deprocessing scheme is perfectly selective to the gate metal and SiN_x passivation layers and does not damage the underlying AlGaN/GaN epitaxial layers as shown in the HAADF-STEM images presented in Fig. 3 (samples prepared via site-specific focused ion beam milling).

After deprocessing, the defects along the full length of the gate region of each stressed device were analyzed by top-down SEM using an FEI dual beam BD235 Strate focused ion beam/SEM operated in ultra high-resolution mode. Using several top-down SEM images of each device, the areal percentage of the gate contact of each HEMT, which was rendered defective during stressing, was quantified as a function of gate current density (prior to failure) using ImageJ© analysis software.

3. Results and discussion

Typical top-down SEM images of pristine and defective gate regions of a stressed HEMT after deprocessing are presented in Fig. 4a and b, respectively. As shown in Fig. 4b, these defects manifest themselves as sharply-defined and generally ovoid structures which often occur in well-defined lines down the length of the device. In devices with 100 nm gate lengths, these defects generally appear to span the full length of the gate electrode, although they appear sporadically along the width of the gate. However, in the case of devices with 1.0 μm gate lengths, the defective region may only take up a small fraction of the total gate width at any point along the device width. Large-scale defects associated with catastrophic device shorting between the gate and drain, as shown in Fig. 1c, were not included in analysis and the gate area associated with these defects was removed from study.

ImageJ© analysis software was used to calculate the total area consumed by the under-gate defects by analyzing several top-down SEM images. The total defective area was then normalized to the total contact area of the device being analyzed to determine

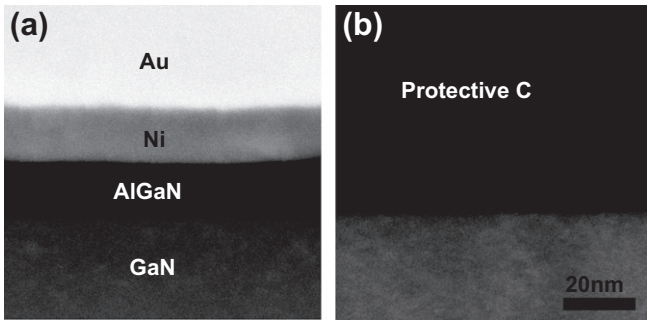

Fig. 4. HAADF-STEM images of the near-gate region of AlGaN/GaN HEMTs with nm-scale gates: (a) prior to deprocessing showing the Au and Ni metal layers and (b) after deprocessing showing thorough removal of the metalization layers with the AlGaN and GaN epilayers left completely intact. The protective C layer in (b) was deposited prior to sample preparation using focused ion beam milling to prevent surface damage.

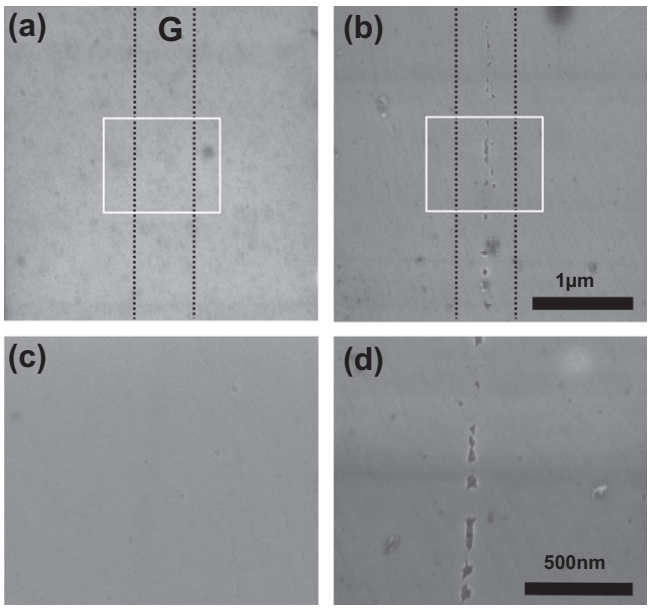

Fig. 5. Top-down SEM images of a stressed AlGaN/GaN HEMT (nm-scale gate device) after deprocessing: (a) a region without detected under-gate defects, (b) a region of the same device with a distinct line of under-gate defects, (c) high-magnification view from the boxed area in parts (a) and (d) high-magnification view from the boxed area in part (b). The approximate locations of the edges of the gate (G) metalization prior to deprocessing are indicated in parts (a) and (b) (dotted lines).

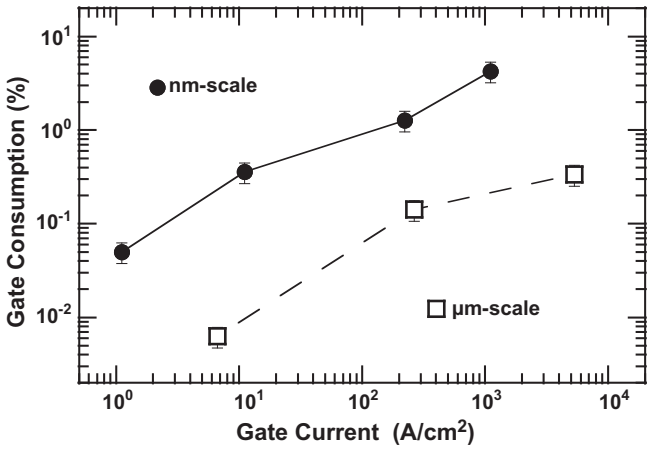

Fig. 6. Percentage of gate contact area consumed by under-gate defects as a function of gate leakage current density (prior to catastrophic failure) for both nm- and μm-scale devices.

the areal percentage of each gate consumed by defects. It should be noted that the gate length in contact with the epilayers rather than the lithographically defined gate length was used in for the normalization calculations.

Fig. 5 presents the calculated areal gate consumption percentage as a function of gate current density for both devices with both 100 nm and 1.0 μm gate lengths (calculated by dividing the gate current by the gate contact area). It is evident that the percentage of gate consumption increases with increase gate current density for both types of devices analyzed. Thus, the data appears to suggest that gate leakage current is strongly influenced by the presence of these defects, which may generate an electrical contact between the gate electrode and the underlying 2DEG (see Fig. 6).

The exact nature of the defects associated with gate sinking are still not understood, but we speculate it may be related to a change in the Ni liner layer in contact with the epilayers. Here, a simple O_2 diffusion-based argument is presented to explain the results [20]. A metallic Ni phase would be a more effective conductor than an oxidized Ni phase. Thus, the magnitude of the leakage current density should vary depending upon whether the defects present under the gate are comprised of metallic or oxidized Ni. This effect may be the cause of the difference between devices with 100 nm and 1.0 μm gate lengths with regards to the trends observed in gate consumption as a function of gate current density. In devices with 100 nm gate lengths, the diffusion length required for O_2 to permeate the entire gate length after diffusing through the SiN_x passivation layer is as little as ~100 nm, while the diffusion length required to permeate the entire gate length of a device with 1.0 μm gate length is ~550 nm. Therefore, for a device with 100 nm gate length, O_2 may diffuse enough during stressing such that the major of defects generated are oxidized Ni-based rather than metallic Ni-based. This would result in lower leakage current densities in these devices as compared to devices with 1.0 μm gate lengths, which may contain a combination of conductive metallic Ni defects in the center of the contact area with more insulating oxidized Ni-based defects close to the gate edges. Moreover, if the diffusion of O_2 results in an insulating oxidized Ni phase rather than a highly-conducting metallic Ni phase, the observed trend of increasing areal gate consumption with increasing current density would vary in devices with 1.0 μm gate lengths depending upon whether the devices are stressed in air ambient or a passivating environment.

4. Conclusions

Top-down scanning electron microscopy was perform on stressed Ni-gate AlGaN/GaN high electron mobility transistors deprocessed via chemical etching to remove the metallization and passivation layers to observe and quantify the presence of under-gate defects. The areal percentage of the gate contacts consumed by defects increased with increasing gate current density for devices with both 100 nm and 1.0 μm gate lengths, though devices with 100 nm gate lengths exhibited significantly more gate consumption than those with 1.0 μm gate lengths. The difference in gate consumption versus current density behavior between different gate lengths may be due to differences in the O_2 diffusion lengths required to generate insulating, oxidized Ni-based defects rather than conductive metallic Ni-based defects.

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