

A 500-MS/s, 2.0-mW, 8-Bit Subranging ADC with Time-Domain Quantizer

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Abstract

This paper describes a novel energy-efficient, high-speed ADC architecture combining a flash ADC and a TDC. A high conversion rate can be obtained owing to the flash coarse ADC, and low-power dissipation can be attained using the TDC as a fine ADC. Moreover, a capacitive coupled ramp circuit is proposed to achieve high linearity. A test chip was fabricated using 65-nm digital CMOS technology. The test chip demonstrated a high sampling frequency of 500 MHz and a low-power dissipation of 2.0 mW, resulting in a low FOM of 32 fJ/conversion-step.

Keywords

Time-Based ADC, Flash ADC, TDC, VTC, CMOS

1. Introduction

With CMOS scaling, the performance of digital circuits has been improved dramatically. Analog LSIs operating in the millimeter wave frequency and the THz region also appeared owing to the improvement in the cut-off frequency by scaling. On the other hand, negative aspects due to scaling, that is, the drop in the intrinsic gain, the increase in device variation, and the decrease in the signal-to-noise ratio due to low supply voltage, are revealed. Various techniques for overcoming these challenges have been studied. A time-domain approach that expresses an analog signal in the time domain has especially attracted much attention. Time-domain signal processing is advantageous in that the signal expression is not limited to the supply voltage and in that most circuits can use digital circuits; therefore, it can enjoy the benefit of CMOS scaling. For example, the implementation of a time amplifier was discussed in [1] [2]. The time am-

plifier with the gain of 4.8 was obtained using cross-coupled chains of variable delay cells. Moreover, a time adder and subtracter using a time register were reported in [3]. Inspired by this technology trend, many works have tried to introduce time-domain processing into analog-to-digital converters (ADCs). An ADC using time-domain processing is called a time-based ADC (TB-ADC). A few works using a VCO as the voltage-to-phase converter measured the phase in the time domain [4] [5]. They have a high resolution but a narrow band due to the noise-shaping property in time quantization. In [6] [7], a simple architecture based on a voltage-to-time converter (VTC) and a time-to-digital converter (TDC) were reported. The input voltage signal is converted into pulses with a delay between them, proportional to the input voltage by the VTC. Then the delay is measured by the TDC. This architecture can achieve a high sampling frequency; however, the nonlinearity of the VTC limits the resolution. In a recent publication, hybrid converters have been described that use both the conventional voltage-domain and the time-domain quantizers [8] [9]. These works successfully reduced the power dissipation using the time-domain quantizer; however, the sampling frequency was limited to less than 100 MHz.

As mentioned above, a TB-ADC with a high resolution and a high sampling frequency has never been developed; therefore, we aimed to realize an 8-bit, 500-MS/s TB-ADC. In this paper, the problems in the conventional TB-ADC are discussed in Section 2. Then, a novel TB-ADC combining a flash ADC and a ring-oscillator-based TDC is proposed in Section 3, followed by the measurement results of a test chip in Section 4. Finally, Section 5 concludes this work.

2. Challenges in Conventional TB-ADCs

Figure 1 shows a block diagram of a 5-bit TB-ADC using a VTC and a TDC [10]. The input signal is converted into a train of pulses by the VTC whose output is fed into the TDC, which converts the delay between pulse edges into a digital representation. This ADC uses a folding architecture to reduce the power dissipation of the TDC. The output signal of the VTC is also fed into the folding

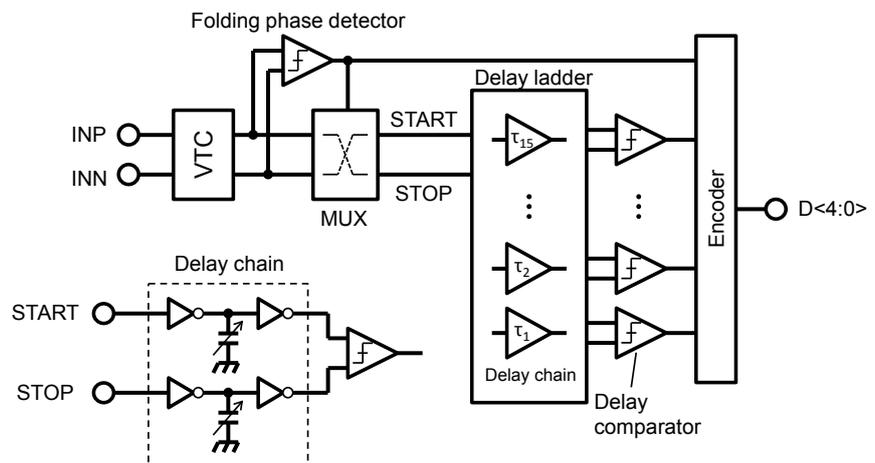


Figure 1. Block diagram of 5-bit TB-ADC using VTC and TDC [10].

phase detector (FPD), which detects the sign of the input signal. The PFD output is used as the most significant bit of the ADC output as well as the folding signal that controls a multiplexer (MUX). This enables to halving of the input range of the TDC, whose resolution can be reduced by 1 bit. The *START* signal is delayed by the delay chains, and 15 time-reference signals are generated. The *STOP* signal is compared to the time-reference signals by the delay comparators, which generate the 4-bit digital codes. The time difference between the adjacent time-reference signals is adjusted to be evenly spaced by the variable capacitor in the delay chain. The time resolution of the TDC (t_{res}) is approximately 3 ps, resulting in a high-speed operation of 5 GS/s. Moreover, the folding technique can reduce the power dissipation, resulting in a low-power dissipation of 21.5 mW. However, the number of the delay chains exponentially increases when the resolution increases; therefore, the power dissipation and the chip area are drastically increased. The conversion speed of the TDC also increases because the maximum delay of the delay chains is approximately $2^n \cdot t_{res}$, where n is the resolution of the TDC. Moreover, the VTC used in this work has large nonlinearity, which degrades the dynamic performance when the VTC is used in the high-resolution ADC. Therefore, this architecture cannot be used in the high-resolution ADC. Therefore, a high-resolution ADC architecture combining conventional voltage-domain processing and time-domain processing is proposed. **Figure 2** shows a block diagram of a 10-bit TB-ADC using subranging architecture [11]. The coarse conversion is performed by a VTC and a TDC, and the fine conversion is performed by the successive approximation register ADC (SAR ADC). The input signal is sampled by the capacitive digital-to-analog converter (CDAC) and is then converted into the time signal by the VTC. The time signal is converted into 3-bit coarse digital code by the TDC. The residue signal is generated by the CDAC using 3-bit code and is converted into 7-bit fine code by the SAR ADC. Coarse and fine codes are combined by the digital error correction circuit (DEC). The offset error of the TDC can be corrected by the DEC; therefore, calibration is unnecessary. A low TDC resolution of 3.5 bit enables low-power dissipation. However, the sampling frequency is low (100 MS/s) because the

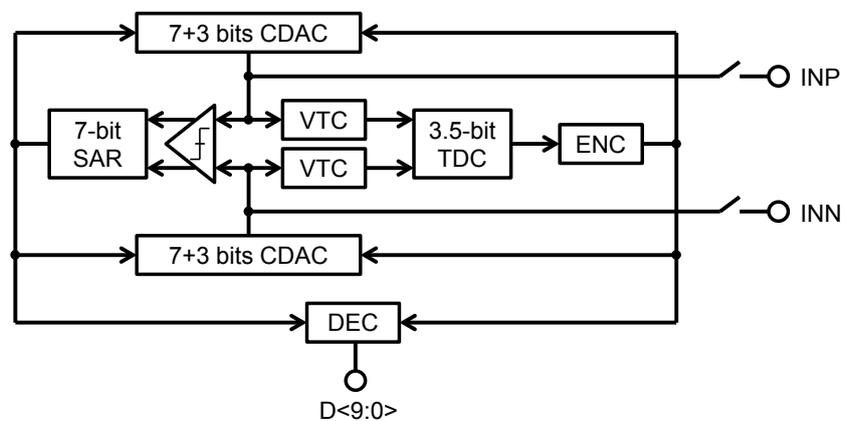


Figure 2. Block diagram of 10-bit TB-ADC combining voltage-domain and time-domain processing [11].

comparator and CDAC should operate seven times in the SAR ADC. Additionally, the VTC uses a high supply voltage (2.5 V) to improve the linearity performance, resulting in an increase in power dissipation.

3. Proposed ADC Architecture

As mentioned in Section 2, the high-resolution ADC can be obtained by a combination of the voltage-domain and the time-domain processing; however, the sampling frequency is low. This is because the SAR ADC is used as the voltage-domain ADC. Therefore, we propose a novel TB-ADC architecture combining a flash ADC and a TDC. A block diagram of the proposed 8-bit TB-ADC is shown in Figure 3. The input differential signals (INP and INN) are converted into upper 3-bit digital code by the flash ADC, and then the CDAC generates the residue signals (V_{resp} and V_{resn}). The residue signals are converted into the time signals (the time difference between $START$ and $STOP$), which are converted into lower 6-bit digital code. These digital codes are adjusted to obtain the digital output $D < 7:0 >$ by the encoder. A high conversion rate can be obtained owing to the flash coarse ADC. The TDC is used as a fine ADC because the time-domain quantizer has a low-noise nature and a low-power dissipation compared with the conventional voltage-domain quantizer [12]. Additionally, the input range of the VTC can be reduced to 1/8 of the full-scale range, resulting in sufficient linearity even at a supply voltage of 1 V because the VTC and the TDC are used as the fine ADC.

The resolution distribution to the coarse and fine ADCs is a critical challenge in this architecture. Figure 4 shows simulated relationships among the sampling frequency (f_s), the power dissipation, the conversion energy ($Power/f_s$), and the resolution of the flash ADC. The simulations are performed using 65-nm CMOS model. The simulation at a resolution of 0-bit expresses a VTC and TDC based ADC such as that in Figure 1, and that at a resolution of 8-bit expresses a pure flash ADC. The conversion time of the proposed ADC is determined by the sum of the conversion times of the flash ADC and the TDC based ADC. The flash

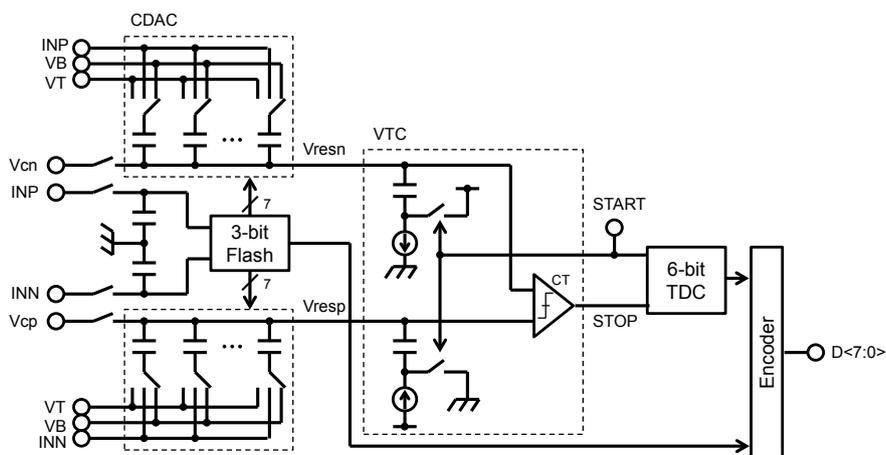


Figure 3. Block diagram of proposed 8-bit TB-ADC.

ADC has a constant conversion time regardless of the resolution. On the contrary, the conversion time of the TDC based ADC exponentially increases when the resolution increases. Therefore, the sampling frequency is improved as the flash resolution increases. The sampling frequency is limited by the TDC in this architecture. The power dissipation has a minimum value around a flash resolution of 2 to 4 bit. This is because the power dissipation of the flash ADC increases and that of the TDC decreases as the flash resolution increases. Therefore, the conversion energy has a minimum value around a flash resolution of 3 to 5 bit. The flash resolution of 3 bit is used to prioritize the circuit area in this design.

3.1. Flash ADC

A block diagram of the 3-bit flash ADC is shown in Figure 5. The flash ADC is composed of a resistor ladder, the discrete time comparators, the set-reset (SR) latches, the bubble-error-correction circuit, and the encoder. The resistor ladder generates the reference voltages $V_{refp} <1:7>$ and $V_{refn} <1:7>$. The differential input signals INP and INN are compared with the reference voltages by the discrete time comparators and the thermometer code $THM <1:7>$

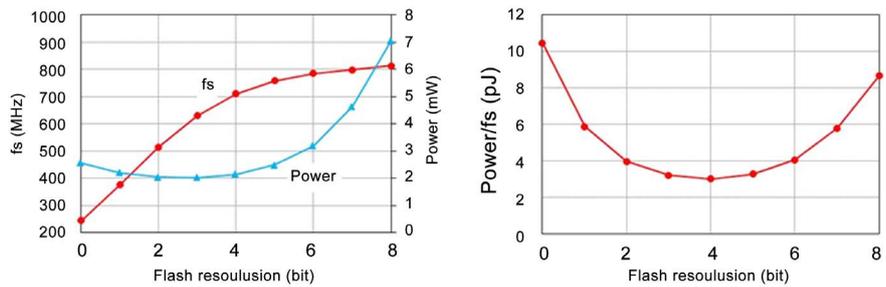


Figure 4. Simulated relationships among sampling frequency (fs), power dissipation, conversion energy (Power/fs), and resolution of flash ADC.

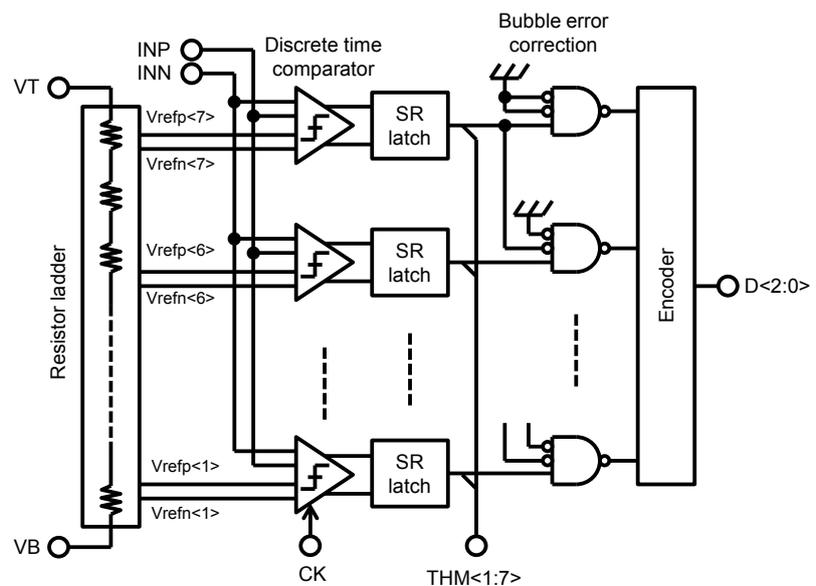


Figure 5. Block diagram of 3-bit flash ADC.

is generated through the SR latches. Then the bubble error contained in the thermometer code is corrected by the bubble-error-correction circuit and the thermometer code is converted into binary code $D < 2:0 >$ by the encoder.

A schematic of the discrete time comparator is shown in **Figure 6**. A comparator known as a Strong ARM latch, which enables the high-speed operation and the low-power consumption, is used. The voltage difference between the input signal and the reference voltage is converted into the differential current by the clocked differential pair (M1 - M4), then the current flows from the latch circuit (M5 - M8). The latch circuit determines the polarity of the voltage difference between the input signal and the reference voltage, and provides the polarity at *OUTP* and *OUTN*.

No offset calibration technique is used for the comparator because the area of the calibration circuit is often considerably large. The range overlapping technique [13] is used instead. The offset voltage of the comparator affects the residue generation as shown in **Figure 6**. The residue is in the range from 0 to $V_{FS}/8$ when the comparator has no offset, where V_{FS} is the input full scale range. However, the residue exceeds $V_{FS}/8$ when the comparator has a positive offset. On the contrary, the residue has a negative value when the comparator has a negative offset. Therefore, the TDC should cover more than $V_{FS}/8$. The input range of the TDC is extended to $V_{FS}/4$ and has 6-bit resolution in this implementation.

3.2. VTC

A schematic of the VTC is shown in **Figure 7**. The VTC is composed of a ramp circuit and a continuous time comparator (CT-CMP). The differential residue signals (V_{resp} and V_{resn}) generated by the CDAC are ramped by the cascode current mirrors with switches. The current mirror discharges (or charges) the capacitor in the CDAC when the *START* signal rises. The current mirror is connected to the residue signal through a capacitor (C_{rp} or C_{rn}). This alleviates the voltage headroom of the current mirror because the initial voltage of the current mirror output is always V_{DD} (or V_{SS}) when the ramp operation starts, resulting in highly linear ramp operation. The voltage headroom of the current mirror is compared with the conventional circuit in **Figure 8**. The common level of the

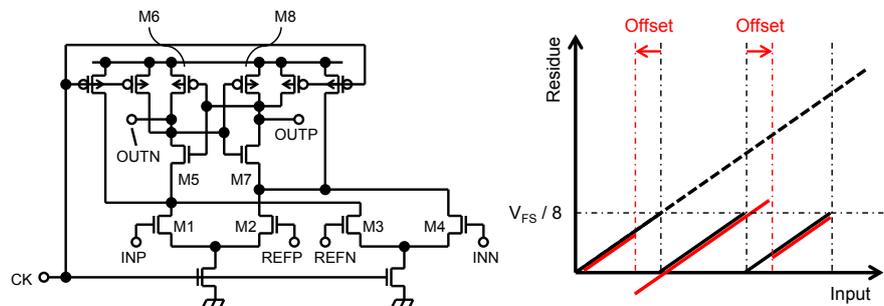


Figure 6. Schematic of discrete time comparator and influence of offset voltage upon residue signal.

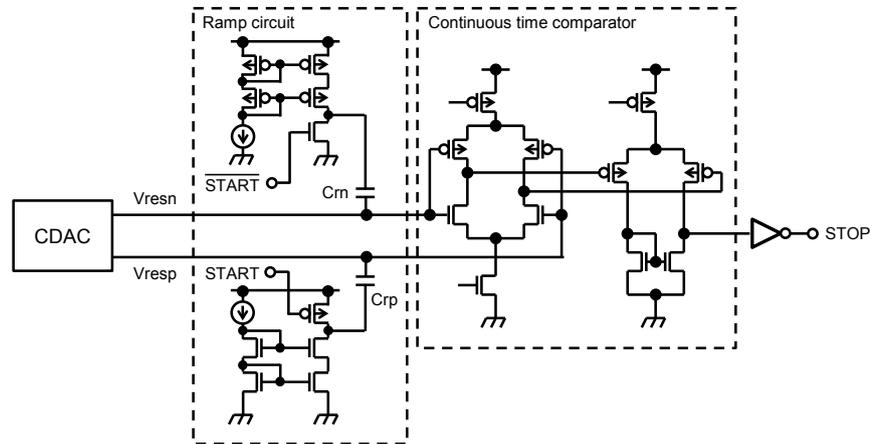


Figure 7. Schematic of VTC.

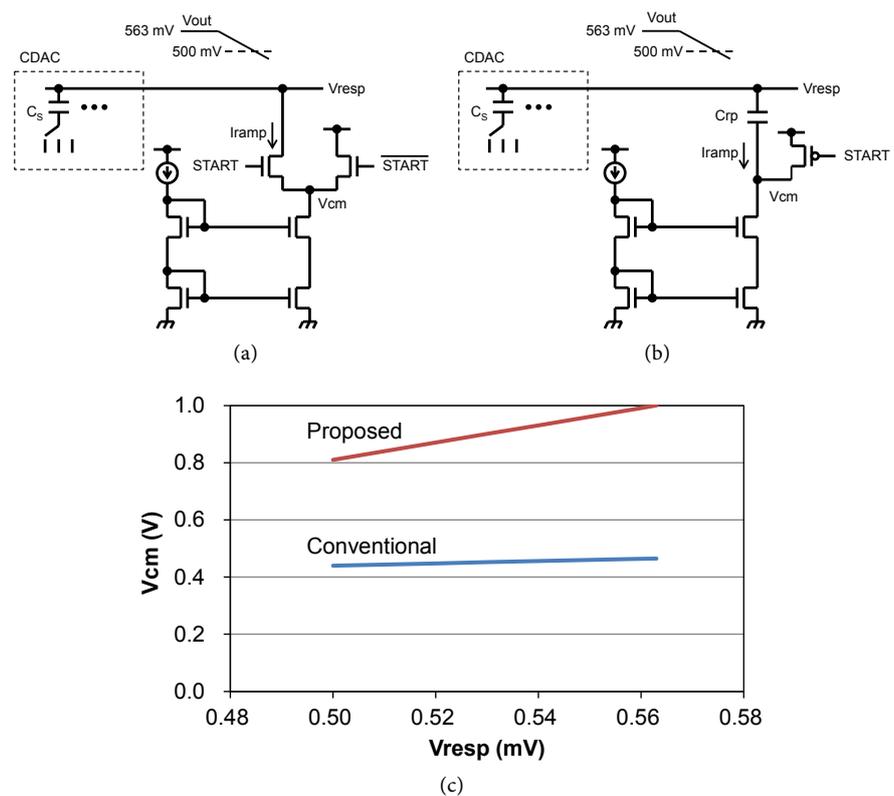


Figure 8. Voltage head room comparison. (a) Conventional ramp circuit; (b) Proposed ramp circuit; (c) Voltage headroom of current mirror.

residue signal is set to $V_{DD}/2$ (500 mV). The highest residue signal is 563 mV ($V_{DD}/2 + V_{FS}/8$) and is discharged to the common level and the STOP signal is generated by the CT-CMP when the residue signal reaches the common level. The current mirror circuit is connected to V_{resp} through a switch in the conventional circuit; therefore, the output voltage of the current mirror circuit (V_{cm}) is lower than V_{resp} . Therefore, V_{cm} is 440 mV, and the output resistance of the current mirror circuit is 30 k Ω when V_{resp} reaches 500 mV. On the other hand, the current mirror circuit is connected to V_{resp} through a capacitor C_{rp} and V_{cm} is

precharged to V_{DD} when the *START* signal is low; therefore, V_{cm} starts to ramp from V_{DD} . V_{cm} is 810 mV, and the output resistance of the current mirror circuit is 530 k Ω when V_{resp} reaches 500 mV. The C-coupled current mirror successfully enhances the output resistance, resulting in highly linear ramp operation.

The CT-CMP detects a cross point of V_{resp} and V_{resn} . Its output (*STOP*) rises when V_{resp} becomes lower than V_{resn} . The time between *START* and *STOP* is proportional to $V_{resp} - V_{resn}$; therefore, the voltage signal can be converted into the time signal. The CT-CMP is composed of a two-stage amplifier. The first stage is a high-gain differential inverter amplifier, and the second stage is a current-mirror-loaded pMOS differential amplifier. The high gain of the first stage successfully reduces the input referred noise to 5 nV/ $\sqrt{\text{Hz}}$.

A block diagram of the TDC is shown in **Figure 9**. A two-step architecture [14] is used; that is, a coarse time measurement is performed by counting the ring oscillator's (RO) output, and a fine time measurement is performed by looking at the RO's phase. The coarse and fine measurement results are combined by the TDC encoder, and the 6-bit binary code is output. The pMOS and nMOS gate widths of the RO are 1.2 μm and 0.4 μm , respectively, and the time resolution of the TDC is 11 ps. The nine-stage RO is used to get the minimum power dissipation. A power-hungry, high-frequency counter such as a common-mode logic circuit [15] is required when the number of stages is too small because the output frequency of the RO is too high. On the contrary, the power dissipation of latches becomes large when the number of stages is too large. The nine-stage RO is optimum in this design. The counter is composed of a true single-phase clock FF to reduce power dissipation.

The rising and falling delay times of the inverter in the RO are designed to be equal; however, the delay time changes because of the process deviation as shown in **Figure 10**. An ununiform delay time causes a conversion error. This can be alleviated by shifting the logical threshold voltage (V_{TH}). The delays are made uniform by increasing V_{TH} in the example shown in **Figure 10(b)**. A schematic of the latch circuit with the threshold-adjust function is shown in **Figure 11**. The output nodes of the regeneration latch *OR*, *OL* are precharged to

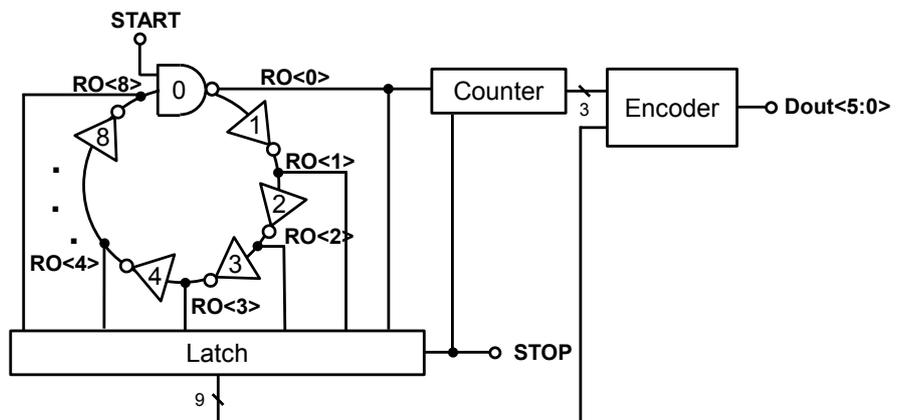


Figure 9. Block diagram of TDC.

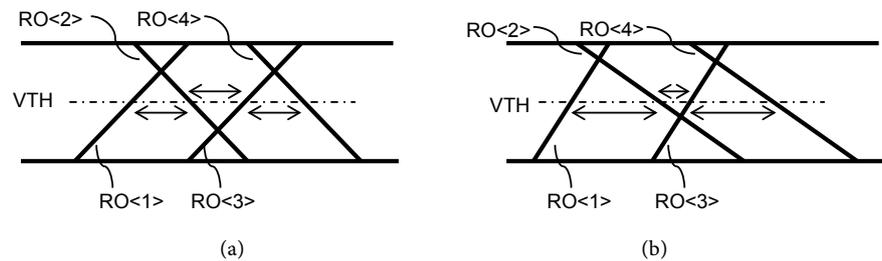


Figure 10. Delay time change due to process deviation. (a) Nominal design condition; (b) With process deviation.

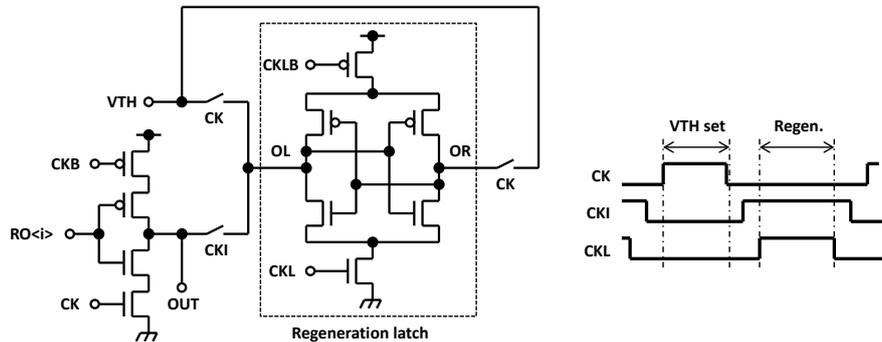


Figure 11. Schematic of latch circuit with threshold-adjust function.

V_{TH} in the V_{TH} set phase. Then, the $RO < i >$ is sampled at the falling edge of CK , which is synchronized to the $STOP$ signal. The sampled signal is transferred to the OL node, then the regeneration latch is activated; thus, the sampled voltage is compared with V_{TH} . The automatic V_{TH} adjustment circuit was not implemented in this version yet, and the V_{TH} was adjusted manually. The implementation of the automatic V_{TH} adjustment is planned for future work.

4. Experimental Results

A test chip was fabricated using 65-nm digital CMOS technology to demonstrate the effectiveness of the proposed architecture. **Figure 12** shows a photomicrograph and a layout plot of the test chip. The circuit area of the ADC core was $180 \mu\text{m} \times 190 \mu\text{m}$. The chip consumed 2.0 mW at 500 MS/s, and the supply voltage was 1 V. The chip was mounted on an evaluation board by using short bonding wire, resulting in a small parasitic inductance. The analog input signal and the clock signal were fed through SMA connectors. **Figure 13** shows the measured DNL and INL. The maximum values of DNL and INL were 0.9 and 1.0 LSB, respectively. The measured sampling frequency dependencies of SNDR are shown in **Figure 14**. The difference between the SNDR at low and Nyquist input frequency was about 1 or 2 dB; therefore, the bandwidth exceeded the Nyquist frequency. The SNDR maintained more than 40 dB up to the sampling frequency of 550 MHz when the V_{DD} was 1 V. The maximum operation frequency was improved to 650 MHz by increasing the V_{DD} to 1.1 V. The measured spectra at the sampling frequency of 500 MHz are shown in **Figure 15**. The ADC output data

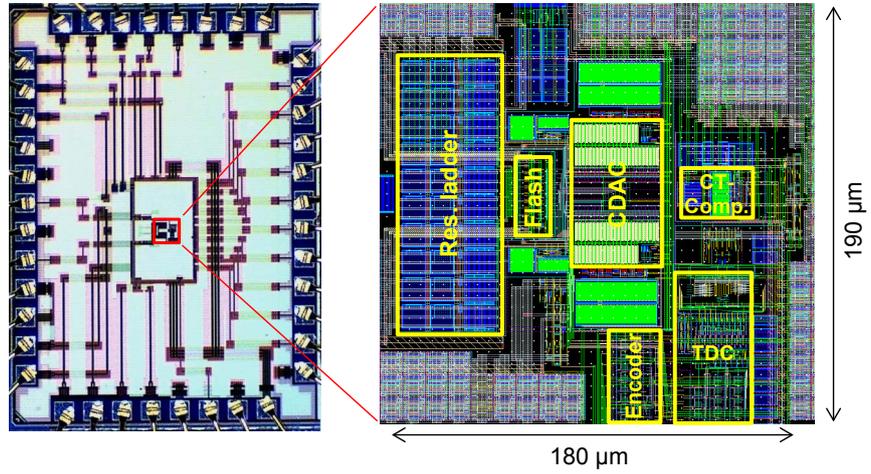


Figure 12. Photomicrograph and layout plot of test chip.

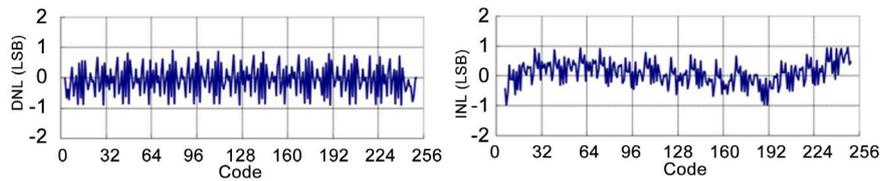


Figure 13. Measured DNL and INL.

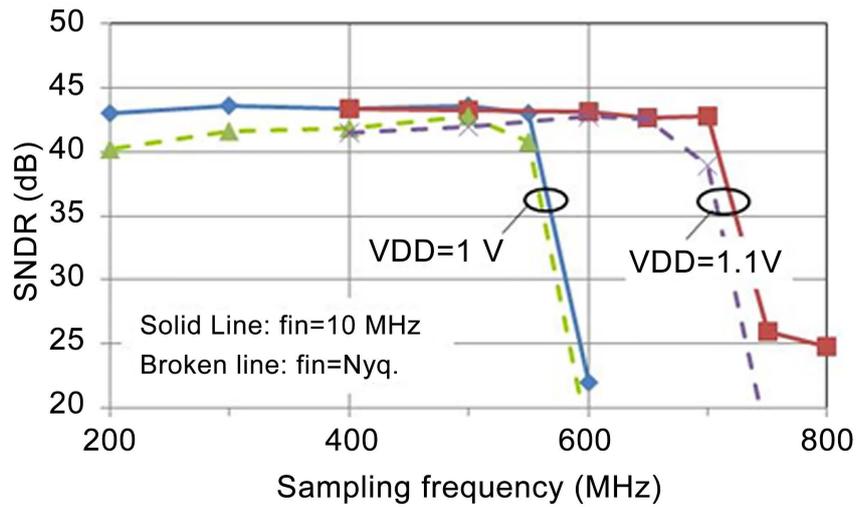


Figure 14. Measured sampling frequency dependencies of SNDR.

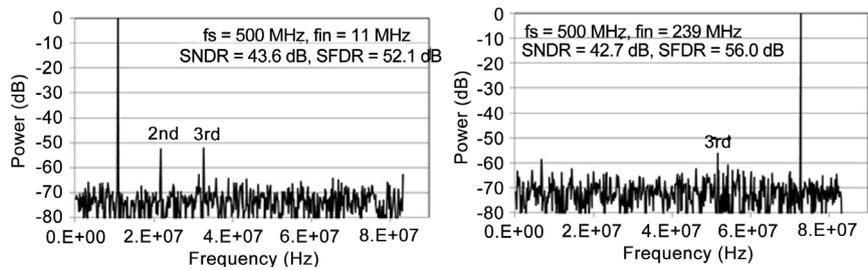


Figure 15. Measured spectra at sampling frequency of 500 MHz.

were down-sampled by a factor of 3 because of a limitation in the maximum bit rate of the logic analyzer used. The harmonic distortion was sufficiently small, and a high SFDR of 56.0 dB was observed. Relatively large harmonics was observed for the input frequency of 11 MHz. This is due to the signal generator for the input signal which has rather poor signal purity in the low frequency range. **Figure 16** shows the sampling frequency dependencies of the FOM. The minimum FOM of 32 fJ/conversion-step was obtained at the sampling frequency of 500 MHz and the supply voltage of 1 V. At the supply voltage of 1.1 V, the FOM increased to 43 fJ/conversion-step at 650 MHz. **Table 1** shows a performance comparison among the ADCs recently published [10] [11] [16] [17]. The FOM of this work is superior to other TB-ADCs. The FOM of [16] exhibits better value than this work; however, it used 45 nm CMOS technology.

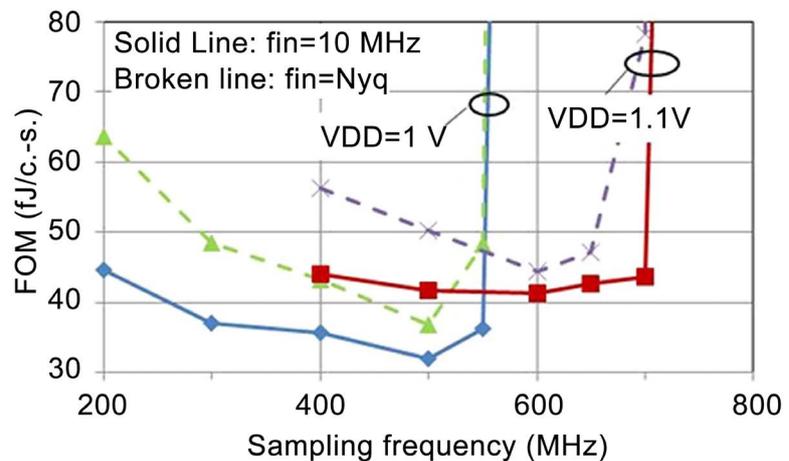


Figure 16. Measured sampling frequency dependencies of FOM.

Table 1. Performance comparison.

	This work	[10]	[11]*	[15]	[16]	
Resolution (bit)	8	5	10	10	10	
Sampling rate (MHz)	500	5000	100	40	1600	
Architecture	TB-ADC	TB-ADC	TB-ADC	TB-ADC	TB-ADC	
SNDR (dB)	Low freq.	43.6	30	59.7	55	?
	Nyquist freq.	42.7	26.7	?	53.8	56.1
SNDR (dB)	Low freq.	52.1	42.4	?	66.0	?
	Nyquist freq.	56	30.5	?	61.3	61.2
Supply voltage (V)	1.0	1.05	1.2	1.8	1.1	
Power (mW)	2.0	21.5	2.7	6.1	17.3	
FOM (fJ/c.-S.)	Low freq.	32	170.0	34.2	?	?
	Nyquist freq.	42	?	?	380	21
Active area (mm) ²	0.034	0.17	?	1.2	0.36	
Technology (nm)	65	65	65	180	45	

*Simulation results.

5. Conclusions

The TB-ADC has attracted much attention to solve various challenges in ADCs due to CMOS scaling. Thus far, an ADC using both voltage- and time-domain processing has been proposed; however, its operation speed was low. Therefore, we propose a novel TB-ADC architecture combining a flash ADC and a TDC. A high conversion rate can be obtained owing to the flash coarse ADC, and low-power dissipation can be attained using time-domain processing in the fine ADC. A capacitive coupled ramp circuit is also proposed to contribute to high linearity. Moreover, a latch circuit with the threshold-adjust function reduces a conversion error of the TDC due to the process deviation. A test chip was fabricated using 65-nm digital CMOS technology, and it demonstrated a high sampling frequency of 500 MHz and a low-power dissipation of 2.0 mW, resulting in a low FOM of 32 fJ/conversion-step.

The threshold voltage for the TDC was adjusted manually in this version. The implementation of the automatic adjustment is planned for future work.

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