Simplified Low-Voltage CMOS Syllabic Companding Log Domain Filter

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Abstract—This paper proposes a low-voltage syllabic companding log domain filter without state variable correction circuits, which is needed for externally linear and time-invariant operation of conventional filters. The proposed filter is simplified and has wide input range under low-supply voltage by varying a nodal voltage adaptively. The simulation results show 60-dB input range for over 40-dB signal to noise plus distortion ratio at a power supply of 0.6 V in a 0.18-μm CMOS process.

I. INTRODUCTION

The technique of low-voltage CMOS analog integrated circuit design is indispensable for implementing several portable applications such as sensing and telecommunication circuits because of requirement of low power consumption and degradation of device breakdown voltage. In the design of low voltage analog circuits, low headroom of an internal voltage makes difficult to achieve a required specification of dynamic range. Syllabic companding technique, especially dynamically adjustable biasing (DAB) technique combining with log domain circuits, is useful to realize wide dynamic range characteristic [1,2]. Although the DAB technique is modified for low voltage operation in Ref. [3], the complexity of the circuit increases compared with a filter based on the DAB technique of Ref. [2] because a state variable correction (SVC) circuit is needed to keep externally linear, time-invariant (ELTI) operation in the low-voltage version.

In this paper a novel syllabic companding log domain filter with no SVC circuit is proposed. Although an SVC circuit is not used, ELTI characteristic of the proposed filter is kept. Its circuit scale is comparable to that of the conventional DAB filter, while the dynamic range is higher than the DAB one at low supply voltage. Simulation results show the proposed filter is effective for dynamic range at low supply voltage.

II. LOW-VOLTAGE INTEGRATOR WITH NO STATE VARIABLE CORRECTION CIRCUIT

A schematic of an integrator based on the DAB technique is shown in Fig. 1(a). In this circuit it is assumed that all MOSFETs are in weak inversion region where a drain current $I_D$ is expressed as an exponential function of its gate-to-source voltage $V_{gs}$: $I_D = I_S \exp(V_{gs}/nU_T)$. A current $I_S$ is dependent on a fabrication process and proportional to the aspect ratio of the MOSFET, and $n$ and $U_T$ are a slope factor and the thermal voltage, respectively. The diode-connected MOSFETs $M_{inp}$ and $M_{imm}$ logarithmically convert input currents $I_{inp}$ and $I_{imm}$ into voltages $V_{ip}$ and $V_{im}$, respectively, which are inputs of a log-domain integrator core composed of a log-domain operational transconductance amplifier (OTA) shown in Fig. 1(b) and a capacitor $C$. An output voltage $V_o$ of the log-domain integrator core is exponentially converted to an output current $I_{out}$ through $M_{out}$ as an expander. Since a bias current $I_{bias}$ and a bias voltage $V_b$ are constant, a source potential $V_C$ of $M_o$ is also fixed. A control current $I_g$ is dynamically varied according to an envelop of the input current to achieve wide-dynamic range characteristic [1–3]. Furthermore, since $I_g$ is a common-mode current of $I_{inp}$ and $I_{imm}$, the differential structure eliminates the influence of this current for $I_{out}$ [2].

In Fig. 1(a), nevertheless, changing the bias current of $M_{inp}$ and $M_{imm}$ with $I_g$, the common-mode voltages of $V_{ip}$ and $V_{im}$ also change, leading to narrower dynamic range under low supply voltage because the input range of the log-domain OTA is limited.

Figure 1(c) shows a modified version of a DAB-based integrator for low voltage operation [3]. In this configuration, since the common-mode voltages of $V_{ip}$ and $V_{im}$ is kept constant by varying the source potential $V_C$ of $M_o$ with $I_g$, a required input range of the log-domain OTA may be narrower than that of the previous DAB-based integrator. Therefore, the schematic of Fig. 1(c) is suitable for low-voltage circumstances. However, a current $nU_TC I_g^2/I_g$, which is generated by an SVC circuit, is required in parallel with a capacitor $C$ in order to ensure ELTI relation between $I_{in}$ and $I_{out}$. In Ref. [3], the device size of two MOSFETs in an SVC circuit should be large due to limitation of its topology at a low supply voltage. Parasitic components of large devices in an SVC circuit make difficult to accurately obtain a required SVC current and then an output error arises. On the other hand, the integrator shown in Fig. 1(a) needs no SVC circuit. Therefore, the schematic of Fig. 1(a) is suitable from the viewpoint of complexity of circuits.

For the problem discussed above about both of low voltage and small circuit, a solution is proposed in Fig. 1(d). The proposed configuration is also a modified version of a DAB-based one in Fig. 1(a) where a terminal of $C$ is connected with the source terminal of $M_o$ and $I_{bias}$ in Fig. 1(a) is replaced with $I_g$. ELTI relation between $I_{in}$ and $I_{out}$ can be proved as follows. First, log-compression function of $I_{inp}$ at $M_{inp}$ and
M gives

Hence, Kirchhoff’s current law at the gate terminal of

respectively. An output current

Fig. 1(b) is given as

expansion function of $V_o$ at $M_{out}$ can be expressed as

$V_{ip} = nU_T \ln \left( 1 + \frac{I_{inp}}{I_g} \right) + V_b$   \hspace{1cm} (1)

and

$V_o = nU_T \ln \left( \frac{I_{outp}}{I_g} \right) + V_b$,   \hspace{1cm} (2)

respectively. An output current $I_1$ of the log-domain OTA in

Fig. 1(b) is given as

$I_1 = I_0 \left( \frac{V_{ip} - V_o}{nU_T} - \frac{V_{im} - V_o}{nU_T} \right)$.   \hspace{1cm} (3)

Hence, Kirchhoff’s current law at the gate terminal of $M_{out}$ gives

$I_0 \left( \frac{V_{ip} - V_o}{nU_T} - \frac{V_{im} - V_o}{nU_T} \right) = C \frac{d}{dt} (V_o - V_C)$.   \hspace{1cm} (4)

Substituting Eqs. (1), (2), and

$V_C = nU_T \ln \left( \frac{I_s}{I_g} \right) + V_b$   \hspace{1cm} (5)

into Eq. (4), a differential equation

$\Omega I_{in} = \frac{dI_{out}}{dt}$   \hspace{1cm} (6)

is obtained where $\Omega = I_g/(nU_TC)$ and $I_{in} = I_{inp} - I_{im}$. It is known that the proposed circuit of Fig. 1(d) is an ELTI integrator and does not require an SVC current. Furthermore, the common-mode voltages of $V_{ip}$ and $V_{im}$, which are input voltages of the log-domain OTA, can be kept constant by appropriately biasing $M_{inp}$, $M_{im}$, and $M_S$ with $I_g$ Therefore, the proposed integrator in Fig. 1(d) can operate at low supply voltage.

III. FILTER IMPLEMENTATION

The modification for simple low-voltage log-domain integrators is applicable to the log-domain filters. As an example of this proposed modification, the third-order Butterworth low-pass filter with a 100-kHz cutoff frequency is designed. In this example, a pseudo differential form of log-domain filter cores is employed to eliminate an influence of $I_g$ biasing $M_{inp}$ and $M_{im}$ [2]. A half pseudo differential log-domain filter core is synthesized in the log domain by leap frog simulation as shown in Fig. 2(b) [4]. The bottom terminals of the capacitors $C_1$, $C_2$, and $C_3$ are connected with the source terminal of $M_s$ to keep ELTI relation between $I_{in}$ and $I_{out}$ as expressed in the previous section. Letting all bias current $I_1$, $I_2$, and $I_3$ be 1.0 $\mu$A, the capacitances are set as $C_1 = C_3 = 50$ pF and $C_2 = 100$ pF for the desired cutoff frequency. All aspect ratios (width/length) of $M_{inp}$, $M_{im}$, $M_{outp}$, $M_{outm}$, and $M_S$ are set as 384 $\mu$m/0.42 $\mu$m, and that of $M_0$ is as 300 $\mu$m/0.18 $\mu$m. This filter is designed using a 0.18- $\mu$m CMOS process and a 0.6-V supply voltage $V_{DD}$.

A control circuit in Fig. 2(a) generates $I_g$ which determines dynamic range of the filter and must be designed for a wide dynamic range. A control circuit shown in Fig. 3 is used here [3] and $I_g$ takes any one of three discrete values $I_{ref1}$, $I_{ref2}$, or $I_{ref3}$ at a time by switching $S_1$ to $S_3$ according to an amplitude of input signal [5]. If $I_{ref1} < I_{ref2} < I_{ref3}$ is satisfied, for example, $I_g$ is set to $I_{refi}$ ($i = 1, 2, \text{ or } 3$) when the amplitude $|I_{in}|$ of an input current is in the region as $I_{ref(i-1)} < |I_{in}| \leq I_{refi}$ where $I_{ref0} = 0$. A circuit controlling the switches can be implemented by use of a peak detector, several comparators, and some reference current sources as described in Ref. [3]. The number of current sources in the control circuit is not limited to only three and this circuit can be easily extended according to a filter specification. A resistor $R_L$ and a capacitor $C_L$ compose a simple low-pass filter to avoid large disturbance at the input stage comprised of $M_{inp}$, $M_{im}$, and $M_S$. Here those values are chosen as $R_L = 100$ k$\Omega$ and $C_L = 50$ pF.

The number of current sources and their values are determined as follows. Figure 4 shows simulation results of
signal to noise plus distortion ratios (SNDRs) in multiples from 100-nA to 208-μA $I_g$.

Fig. 3. Control circuit.

Fig. 4. Signal to noise plus distortion ratios (SNDRs) in multiples from 100-nA to 208-μA $I_g$.

IV. SIMULATION RESULTS

The proposed syllabic-companding log domain filter is simulated to confirm the characteristics. The parameters determined in the previous section are used in this simulation.

First of all, frequency response of the proposed filter is verified. Figure 5 shows the simulation results where a control circuit used in Fig. 2(a) is replaced with a 3-output constant current source of Fig. 3. The filter has a 96.5-kHz cutoff frequency each $I_g$ as seen from Fig. 5.

Figure 6(a) shows the fundamental component of $I_{out}$, total harmonic distortion, and an RMS output current noise from DC to 400 kHz during one period, versus amplitude of a 100-kHz sinusoidal input current $I_{in}$. In Fig. 6(a), the fundamental output current increases in proportion to an input current, while output noise does stepwise. Figure 6(b) shows an SNDR characteristic obtained from results of Fig. 6(a). As seen from Fig. 6(b) the proposed filter can satisfy the specification of a 60-dB input range over 40-dB SNDR.

Figure 7(a) shows a 100-kHz sinusoidal input current $I_{in}$ with an envelope changed, and a control current $I_g$. In Fig. 7(b) waveform of the log-compressed voltage $V_{inp}$ of the proposed
filter is depicted. It is verified that the bias voltage of $V_{\text{inp}}$ keeps almost constant. Figure 7(c) shows the output current $I_{\text{out}}$ of the proposed filter. Table I shows summary of the filter characteristics. The proposed filter operates well for low voltage such as a 0.6-V $V_{DD}$. In addition, when $I_g$ changes from 400 nA to 50 $\mu$A, the current consumption is observed as 75 to 330 $\mu$A which corresponds to 45- to 198-$\mu$W power consumption. Finally, the proposed filter has 100-dB dynamic range, which is calculated from the ratio of the input current over 40-dB SNDR to minimum noise floor.

V. Conclusion

A low-voltage syllabic-comanding log domain filter with no state variable correction circuits has been proposed. The proposed filter is easily simplified by varying a terminal voltage of capacitors adaptively and still has wide dynamic range even at a low supply voltage. Simulation results show 60-dB input range and an over 40-dB signal to noise plus distortion ratio at a power supply of 0.6 V in a 0.18-$\mu$m CMOS process. Future works are fabrication and measurement.

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