At-Speed BIST for Board-Level Interconnect

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3. BIST for Static Faults and Boundary Scan
4. At-Speed Testing of Dynamic Faults
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PCB Testing Challenge

**Challenges**
- PCBs are getting complex
- Up to several k nets on PCB
- New faults getting involved
- Test access is getting limited
- Workforce factors

**How to cope?**
- ICT, X-ray, optical?
- Functional testing or BIST?
Limitations of Traditional Methods

Usage of traditional interconnect testing methods at different levels of technology:

<table>
<thead>
<tr>
<th></th>
<th>In-Circuit Test</th>
<th>Boundary Scan</th>
<th>X-Ray &amp; Optical Inspection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board level interconnect</td>
<td>Small boards, <em>static faults only</em></td>
<td>BS-compliant boards, multi-board systems, <em>static faults only</em></td>
<td>Limited interconnect fault coverage</td>
</tr>
<tr>
<td>Network-on-Chip</td>
<td>Not applicable</td>
<td>Applicable as a <em>concept only</em></td>
<td>Not applicable at this moment</td>
</tr>
</tbody>
</table>

Conclusions:
- *dynamic fault testing is not possible with traditional methods*
- *interconnect testing solutions for NoC are missing*
Introduction

• Characteristics of an interconnect self-test framework:

• Test pattern generation (TPG)
  - Fault models (static vs. dynamic faults) and fault coverage
  - Deterministic, pseudo-random, and weighted sequences
  - TPG hardware

• Test application
  - Test access mechanism (BS, in-circuit test, custom solutions, etc.)
  - Test-per-scan vs. test-per-clock
  - At-speed testing vs. low-speed testing

• Response analysis (RA) and diagnosis
  - RA hardware
  - Detection vs. diagnosis
  - Diagnostic resolution
A Dream

- Components generate test patterns themselves
- Test generation and application takes logarithmic time (e.g. 30 test vectors for 10,000 interconnect nets)
- Testing runs at operating speed and catches dynamic defects
- Components from different vendors compatibly operate
- Diagnosis is exact and performed by components themselves
- Simple hardware (of BS complexity) is used
Introduction

• Desired properties of an interconnect self-test framework:

  • Short test application time => using a good test set
  • Low hardware overhead => TG and RA must be simple
  • High fault coverage and relevant fault model
  • Aliasing-free response analysis & precise diagnosis
  • Compatibility with existing standards
  • Scalability
1. Introduction
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   • Modeling of interconnect faults
   • Classical test generation algorithms
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Modeling of Interconnect Faults

- Defect types and models
  - Short faults
  - Open faults
  - Delay faults
  - Noise/crosstalk
  - Ground bounce
  - ...

\[
\begin{align*}
\text{static behavior} & \quad \text{dynamic behavior}
\end{align*}
\]
Short Faults

- Possible shorts: bond wire, leg, solder, interconnect
- *Shorts are usually modeled as wired-AND, wired-OR faults*
Open Faults

- Misplaced bond wire
- Misplaced component

- Possible opens: bond wire, leg, solder, interconnect

- Opens usually behave like stuck-at or delay faults
Crosstalk Modeling: Noise and Skew

Overhead:
- overshoot
- ringing
- delay

Diagram:
- **V_{dd}**
- **V_{ss}**

Regions:
- **Noise-immune region**
- **Skew-immune region**
Kautz [1] showed in 1974 that a sufficient condition to detect any pair of short circuited nets was that the serial codes must be unique for all nets. Therefore the test length is $\lceil \log_2(N) \rceil$.
The Modified Counting Sequence

- All 0-s and all 1-s are forbidden codes because of open faults. Therefore the final test length is $\lceil \log_2(N+2) \rceil$
- This method was proposed in 1982 by Goel & McMahon [2]

Some of the observed error responses are allowed codes.

How to improve the diagnosis?
The True/Complement Code

- To improve the diagnostic resolution Wagner proposed the True/Complement Code in 1987 [3].
- The test length became equal $2^{\left\lfloor \log_2(N) \right\rfloor}$

• All-0 and all-1 codes are not forbidden anymore!
Important properties of the True/Complement Code are:
- there are equal numbers of 0-s and 1-s upon each line
- Hamming distance between any two code words is at least 2
# Summary of TG Methods

<table>
<thead>
<tr>
<th></th>
<th>Counting</th>
<th>Modified</th>
<th>True/Compl.</th>
<th>Walking</th>
<th>LaMa</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>001</td>
<td>111</td>
<td>000</td>
<td>1000000</td>
<td>00001</td>
</tr>
<tr>
<td>001</td>
<td>010</td>
<td>110</td>
<td>001</td>
<td>0100000</td>
<td>00100</td>
</tr>
<tr>
<td>010</td>
<td>011</td>
<td>101</td>
<td>010</td>
<td>0010000</td>
<td>00111</td>
</tr>
<tr>
<td>011</td>
<td>100</td>
<td>100</td>
<td>011</td>
<td>0001000</td>
<td>00110</td>
</tr>
<tr>
<td>100</td>
<td>101</td>
<td>010</td>
<td>100</td>
<td>0000100</td>
<td>01101</td>
</tr>
<tr>
<td>101</td>
<td>110</td>
<td>001</td>
<td>110</td>
<td>0000010</td>
<td>10001</td>
</tr>
<tr>
<td>110</td>
<td></td>
<td></td>
<td>000</td>
<td>0000001</td>
<td></td>
</tr>
<tr>
<td>111</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Length</th>
<th>$\log_2(N)$</th>
<th>$\log_2(N+2)$</th>
<th>$2\log_2(N)$</th>
<th>N</th>
<th>$\log_2(3N+2)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td>14</td>
<td>14</td>
<td>28</td>
<td>10000</td>
<td>15</td>
</tr>
<tr>
<td>(N=10000)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hamming distance</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Defects</td>
<td>Shorts</td>
<td>Shorts Opens</td>
<td>Shorts Opens /Delays/</td>
<td>Shorts Opens /Delays/</td>
<td>Shorts Opens</td>
</tr>
<tr>
<td>Diagnostic Properties</td>
<td>Bad</td>
<td>Bad</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
</tbody>
</table>
1. Introduction
2. Interconnect Faults: Models and TG Methods
3. BIST for Static Faults and Boundary Scan
   - Boundary Scan
   - Typical test generation hardware used with BS
   - Handling the bus contention problem
4. At-Speed Testing of Dynamic Faults
5. Deterministic Interconnect BIST
6. Discussion
• Early 1980’s – problem of test access to PCBs via “bed-of-nails” fixture
• Mid 1980’s – Joint European Test Action Group (JETAG)
• 1986 – US companies involved: JETAG -> JTAG
• 1990 – JTAG Test Port became a standard [4]:
  • IEEE Std. 1149.1: Test Access Port and Boundary Scan Architecture
    • comprising serial data channel with a 4/5-pin interface and protocol
Test Access Via Boundary Scan
A typical TPG for the Counting Sequence [5]
TPG for the Counting Sequence

- **Drawbacks of the solution**
  - Before a test vector can be applied it must be shifted into the BS register, which takes $L$ clock cycles, where $L$ is the length of the BS register.
  - For a test of length $T$ the total test application time is equal to $T \cdot L$.
  - Moreover, the at-speed testing is problematic here.
  - There is also a multiple driver contention problem.

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- Moreover, the at-speed testing is problematic here.
- There is also a multiple driver contention problem.
Multiple Driver Contention Problem

- A typical tri-state net in a board-level interconnect with several drivers and receivers on the same net.

There is a danger of damaging the circuits when several drivers are simultaneously activated by a mistake.
Solutions to the Contention Problem

- Partitioning of the generator into D-TPG & C-TPG [5-6]

- Compatible to the BS standard
Solutions to the Contention Problem

• Partitioning of the BS Register

- requires additional pins and routing

• Easy test application
• Good control over the bus contention issue
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   • Requirements of at-speed testing and BIST
   • PRPG based TPG methods
   • Crosstalk measurement
   • Common drawbacks of PRPG based methods
5. Deterministic Interconnect BIST
6. Discussion
At-Speed Interconnect Testing

- Required properties:
  - Vectors should be applied in parallel (test-per-clock)
  - Both 1→0 and 0→1 transitions must be activated
  - Responses should be captured without delay
Test Generation and Test Application

- Test-per-Clock instead of Test-per-Scan => BIST
- Relevant test generation algorithm
At-Speed Interconnect BIST

• LFSR-MISR based solutions

How many test patterns are enough to cover all delay faults and other dynamic effects?

• Texas Instrument’s SCOPE library [7]
• Implemented in IBM RISC 6000 processor [8]
• LFSR optimization technique based on graph coloring and genetic search proposed in [9].
• A modification to LFSR, which allows weighted pattern generation in [10]
At-Speed BIST for Delays and Crosstalk


- Resembles real life interconnect switching profiles
- Worst-case interconnect switching activities without overestimation and damaging the chip
- Designed with help of Markov chain theory

Cascaded structure of pre-characterized nonlinear feedback shift registers

0 0 1 0
0 1 0 0
1 0 1 0
0 1 0 1

Some Response Analyzer

- Comparatively high silicon area needed for TPG
- Test sequence might be long
- Response analysis is not discussed

0  010 0100 101 0 1 0 1
Cascaded structure of pre-characterized nonlinear feedback shift registers

Some Response Analyzer
At-Speed BIST for Delays and Crosstalk

• Response analysis: skew and noise detection [12]
At-Speed BIST for Delays and Crosstalk

• Alternative design of SD Cells
  - [13] is overly conservative with the unacceptable false detection level of 40%
  - Test sequence of [14] must be a regular clock-like signal -> bad coverage of shorts
  - [14] requires a counter and separate sampling clock -> high hardware cost per line
  - In most cases delay detection is enough (no need for precise measurement [14])

Double sampling data checker [12]

Statistical delay measurement unit [14]
• Drawbacks of non-deterministic BIST solutions

• Mutual cancellation of multiple stuck-at interconnect faults has a fatal impact on MISR’s ability to detect them (aliasing probability is very high) [15].

• Pseudo-random (PR) patterns are not optimized for specific interconnect faults, especially dynamic ones. This has either one or another following consequence:
  – The length of PR sequence necessary for sensitizing all the static and dynamic faults might be very long.
  – Defect coverage might be low [10].
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   • Shift register based TPG for ITCC code, RA
   • Other Deterministic BIST Solutions
6. Discussion
• Common advantages of deterministic interconnect BIST methods

• Much shorter test sequences
  – logarithmic in many cases
  – optimized accordingly to the fault model

• Explicit fault models
  – provable defect detection
  – good diagnostic properties of the solution
Deterministic Interconnect BIST

- Circular shift register based TPG [19]

The initial state of TPG is generated by an external LFSR.
• Interleaved True/Complement Code and corresponding TPG [19]

- Both 1-0 and 0-1 transitions always exist (delay fault testing)
- Both opposite value combinations (0/1 and 1/0) appear between any two lines (crosstalk testing)
- Hamming distance between two code words is at least 2
- Each code word consists of bit pairs having both 0 and 1 values
Deterministic Interconnect BIST

- On-chip at-speed response analyzer [19]

- Exact fault diagnosis without aliasing
- Complete testing and diagnostic solution
- Unlimited scalability and configuration independence
• If only fault detection is enough

Interleaved True/Complement Code & Corresponding Response Analyzer

If only fault detection is enough
The general structure of the framework

- Control Signals from C-TPG
- LFSR as the feeding device for the at-speed TPG
- Diagnostic Signature

- inputs
- outputs
- control
At-Speed Interconnect BIST with the Interleaved True/Complement Code

- Different operation modes

**At-Speed Testing Mode**

- Inputs
- Outputs
- Control

**Boundary Scan Mode**

- TDI
- TDO

From previous chip to the next chip
Properties of the Solution

- Test-per-clock – allows at-speed testing
- Exact on-chip at-speed fault diagnosis
- Detection of both static and dynamic faults
- Unlimited scalability
- Configuration independence
- Compatibility with Boundary Scan standard
Outline

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**Deterministic Interconnect BIST**

- Modification of counting and walking sequences by replacement 0->100 and 1->011 [16]

| 100000 | 011100100100100100 |
| 010000 | 100011100100100100 |
| 001000 | 100100011100100100 |
| 000100 | 100100100011100100 |
| 000010 | 100100100100011100 |
| 000001 | 100100100100100011 |

| 100 | 011100100 |
| 010 | 100011100 |
| 001 | 100100011 |
| 110 | 011011100 |
| 011 | 100011011 |
| 101 | 011100011 |

- Additional silicon area for TPG
- Every second vector is repeating
- Length is $3N$ and $3 \lceil \log_2(N) \rceil$

- Both static and dynamic faults covered
- The main goal is to distinguish between them
Deterministic Interconnect BIST

- Crosstalk testing using Maximum Aggressor fault model [17]

<table>
<thead>
<tr>
<th>Bit Positions in the Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ... i-1</td>
</tr>
<tr>
<td>000...000</td>
</tr>
<tr>
<td>111...111</td>
</tr>
<tr>
<td>111...111</td>
</tr>
<tr>
<td>000...000</td>
</tr>
<tr>
<td>111...111</td>
</tr>
<tr>
<td>000...000</td>
</tr>
</tbody>
</table>

- Quite expensive TPG hardware: counter, decoder, FSM, and a group of 2-1 multiplexers

- Code length is $6N$

- Best possible test for crosstalk
- Might be overly conservative however
Deterministic Interconnect BIST

- TPG based on Johnson counters [18]

- TPG must be divided into many separate parts. Each part must be uniquely initialized.

- Code length grows faster than logarithmically

- Very cheap TPG hardware!
- Generates true/complement code of length $2N/K$
Summary

• **Tasks and recommended methods**

  • Crosstalk testing (6N code + ND/SD cells)
  • Cheap hardware (LFSR/MISR, walking, Johnson, ITCC, ND/SD cells)
  • Aliasing free diagnosis (ITCC)
  • Short test sequence (ITCC, Johnson)
Referenced and Used Materials


Materials for Further Study


Materials for Further Study

- The Boundary Scan demo applet URL: http://www.pld.ttu.ee/dildis/automata/applets/bs/
Thank you!