PANEL SESSION - Who Is Closing the Embedded Software Design Gap?

Moderator: W. Ecker, Infineon, DE

Panelists:
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As pointed out in the ITRS roadmap, the level of embedded software complexity is greater than the pure HW complexity of SoCs when comparing, for example, lines of HDL and C code. Even worse, SW complexity grows faster than HW complexity (Moore’s Law) and SW productivity increases more slowly than HW productivity. A new design gap - the gap of embedded software – as appeared.

EDA has now identified ESL as a field with sufficient revenue and revenue growth, but do they really approach the SW productivity challenge?

This panel gives the answer by presenting recent EDS products and solutions in the area of ESW, contrasting them with needs of industry, and discussing ways out of the ESL productivity crisis.