Exploring Tunnel-FET for Ultra Low Power Analog Applications: A Case Study on Operational Transconductance Amplifier

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ABSTRACT
This work studies the potentials and challenges of designing ultra-low-power analog circuits exploiting unique characteristics of Tunnel-FET (TFET). TFET can achieve ultra-low quiescent current (~pA). In the subthreshold operation, TFET exhibit subthreshold swing lower than 60mV/decade, and hence higher transconductance per bias current than the MOSFET. TFET also exhibit very weak temperature dependence, and higher output resistance. Among several challenges, TFET demonstrate higher Shot noise at low biasing current. Through design of TFET based Operational Transconductance Amplifier (OTA) these challenges and opportunities are discussed. For implantable bio-medical applications, TFET OTA based neural amplifier design is studied.

Categories and Subject Descriptors
B.7.2 [Hardware, Integrated-circuits, Design Aids]: Simulation

General Terms
Performance, Design, Theory

Keywords
Tunnel-FET, ultra-low power designs, operation transconductance amplifier, bio-medical designs

1. INTRODUCTION
The ultra-low-power but low-throughput sensors find critical applications in various areas such as bio-medical electronics, environmental monitoring as illustrated in Table 1. Although, the speed/bandwidth requirements for such applications are relaxed, energy/power constraints are stringent. The low-throughput operation provides opportunities for energy/power reduction. Analog designs are integral part of the most sensor systems, and can consume appreciable portion of system power [16]. Power dissipation of analog components can be contained by subthreshold operation. Transconductance per bias current ($g_m/I_{DS}$) of N-MOSFET, in 90nm CMOS technology, is demonstrated across bias conditions in Fig. 1. In the subthreshold region, the $g_m/I_{DS}$ significantly enhances due to the exponential dependence of drain-current to gate voltage. However, due to lower drain current, the performance (such as $g_m$ itself) reduces.

Hence, when performance requirements are not stringent (as in bio-medical applications [19-20]) the subthreshold operation of MOSFET will be the energy optimal.

In the subthreshold operation, the subthreshold slope (SS) relates to the $g_m/I_{DS}$ as
\[ \frac{1}{SS} = \frac{\Delta \log(I_{DS})}{\Delta V_{GS}} = \frac{1}{\log(10)} \frac{\partial \log(I_{DS})}{\partial V_{GS}} = \frac{1}{\log(10)} \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}} \] (1)

Thus, even higher $g_m/I_{DS}$ in MOSFET is restrained by its SS. The SS in MOSFET is limited to 60mV/decade at room temperature. Novel device architectures are being explored with steeper SS (less than 60mV/decade) TFET [12], Ferroelectric FET [9], and Carbon Nano Tube transistors [10] to name a few. Ultra low quiescent current (~pA) of these devices is also attractive for low power analog applications. Hence, there is a pressing need for early design exploration of these technologies, and to comprehend their benefits and challenges in low power analog designs.

In this work, application of TFET for ultra low power analog designs is investigated using Technology CAD (TCAD) and circuit simulations. The electrical (current, capacitance, transconductance, and noise) characteristics of TFETs are studied using TCAD simulations. Another benefit of TFET is its reduced temperature sensitivity. This feature assists to the robustness of designs especially when compared to the subthreshold MOSFET

<table>
<thead>
<tr>
<th>Application</th>
<th>Frequency Range</th>
<th>Ref</th>
</tr>
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<tbody>
<tr>
<td>EEG Sensor</td>
<td>0.5 ~ 40 Hz</td>
<td>[19]</td>
</tr>
<tr>
<td>Hearing aids</td>
<td>6kHz</td>
<td>[20]</td>
</tr>
<tr>
<td>ENAP Sensor</td>
<td>0.1Hz ~ 10kHz</td>
<td>[19]</td>
</tr>
<tr>
<td>Seismometer</td>
<td>1kHz</td>
<td>[5]</td>
</tr>
</tbody>
</table>

Figure 1: Bias dependences of $g_m/I_{DS}$ for NMOS in 90nm technology.
Our analysis shows that power-bandwidth trade-off in TFET amplifier [7], neural network [18], and non-linear synthesis [13]. OTA is a key building block in analog filters [8], and based Operational Transconductance Amplifier (OTA) circuits are studied. TFET reaches to sub-nW regime, which is not exposed in MOSFET based designs due to MOSFET’s excessive leakage. The noise analysis suggests that eventually the Shot noise imposes the limit on the power reduction of the analog operation of TFET.

2. TUNNEL-FET (TFET)

In this work, CMOS compatible Vertical channel TFET (V-TFET) structures are investigated. V-TFET has benefits of smaller footprint, self-decoupled source/drain implants and paves way for gate-all-around structure [6]. The N-type vertical TFET device is shown in Fig. 2a. Unlike MOSFET, in TFET the drain and source junctions are doped with different dopant types. The channel is undoped. The P-type counterpart is similar except the source is doped with the N-type dopant, and drain with the P-type dopant. To enhance the limited on current of the TFET device, a Germanium doped thin Silicon layer is deposited at the source-channel interface. Various structural specifications are listed in Table-2.

### 2.1 Current Conduction Mechanism

The current conduction mechanism in TFET is band-to-band tunneling (BTBT). In N-TFET, electrons tunnel from the source valence band to the drain conduction band (in P-TFET, holes from the source conduction band to the drain valence band). The BTBT probability (and thus the current) is controlled by changing the gate potential. In Fig. 2b, the conduction and valence band-energies of N-TFET along a vertical cross-section [shown in Fig. 2a] is inverted. For V$_{GS}$=0V, and V$_{GS}$=1V. At V$_{GS}$=0V, the tunneling barrier width is ~45nm, and thus due to very low tunneling probability, TFET achieves extremely low off current. At higher V$_{GS}$ band energies in the channel are lowered, and the tunneling width reduces (~8nm for V$_{GS}$=1V). This increases the tunneling probability, and significant current conduction occurs. The temperature dependence of the BTBT current comes from the temperature dependence of the band-gap. However, since the temperature dependence of band-gap itself is weak, the TFET current demonstrates weak temperature dependence.

### 2.2 Electrical Characteristics

The electrical characteristics of N-TFET are shown in Fig. 3. The characteristics of P-TFET are similar. Key specifications of N&P-TFET are listed in the Table 3. Characteristics were simulated using TCAD simulator Synopsys Sentaurus. Non-local tunneling model is employed. Tunneling path is dynamically altered as per the bias conditions [14].

N-TFET device achieves ultra low off current (~fA), and the drain current increases exponentially with higher V$_{GS}$ [Fig. 3a]. Exponential drain current dependence results into the exponential transconductance increase with V$_{GS}$. The point SS across V$_{GS}$ is shown in Fig. 3b. The SS is steeper at low V$_{GS}$ and rapidly degrades at higher V$_{GS}$. Thus, better g$_m$/I$_{DS}$ benefits of TFET over MOSFET are limited to low gate biases [Eq. 2]. Characteristic against drain bias (V$_{DS}$) is shown in Fig. 3c. A near perfect saturation is observed. The correlation of the saturation voltage (V$_{DS,SAT}$) against the gate voltage is shown in Fig. 3d. At low V$_{GS}$, the V$_{DS,SAT}$ is more than the V$_{GS}$, and the saturation in the TFET is delayed than in the MOSFET [12]. Capacitive characteristics of the N-TFET are shown in Fig. 3e-f. The gate to drain capacitance (C$_{GD}$) is dominant over the gate to source capacitance (C$_{GS}$). With increasing V$_{DS}$, C$_{GD}$ enhances sharply when V$_{DS}$ is large enough to set pinch-off in the channel. Due to the dominant C$_{GD}$ in this region TFET will show enhanced Miller effect. A second rise of C$_{GD}$ occurs when the source region overlapped with the gate [Fig. 2a] is inverted.

### 3. CIRCUIT SIMULATION

To explore TFET’s capability for circuits, compact model is desired. Various compact modeling works for TFET’s electrical characteristics are underway [3,15,1]. Using Kane’s model for BTBT, a simplified description of the TFET’s drain current was given [3]. However, this model doesn’t account for the drain voltage dependence of the current. A more accurate analytical model with description of gate on-set voltage was given [15]. However, the inaccuracies of the model increase at higher gate voltage. Pseudo-two-dimensional model for double-gated Silicon channel TFET was given [1].

In this work we follow an alternative TCAD based approach. Electrical characteristics of TFET were extracted using two dimensional TCAD simulations with bias conditions finely varying over the operating range. Next, Verilog-A based table models were constructed by interpolating these values with quadratic spline. Based on these Verilog-A models, the spice simulations were performed to study analog characteristics of TFET based designs. Accurate correlation of I$_{DS}$-V$_{GS}$ [Fig. 4a] and C$_{GS}$-V$_{GS}$ [Fig. 4b] characteristics for N-TFET between Spice (by the above methodology) and TCAD simulations is shown in Fig. 4b. However, unlike a compact model, the above approach is not a
Figure 3: N-TFET electrical characteristics (a) $I_{DS}-V_{GS}$ (b) SS- $V_{GS}$ (c) $I_{DS}-V_{DS}$, (d) $V_{DS,SAT}-V_{DS}$, (e) $C_{GS}-V_{GS}$, and (f) $C_{GD}-V_{GS}$. scalable solution, and its utility is limited to designs consisting of fewer channel lengths/widths.

![Graphs](image)

**Table-3:** TFET Device Electrical Specifications [$V_{DD}=1V$]

<table>
<thead>
<tr>
<th>Specification</th>
<th>N</th>
<th>P</th>
</tr>
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<tbody>
<tr>
<td>$I_{DS,ON}$ ($\mu A/\mu m$)</td>
<td>38</td>
<td>41</td>
</tr>
<tr>
<td>$I_{DS,OFF}$ ($fA/\mu m$)</td>
<td>2</td>
<td>5.1</td>
</tr>
<tr>
<td>$I_{DS,LIN}$ ($\mu A/\mu m$)</td>
<td>0.97</td>
<td>3.2</td>
</tr>
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</table>

Figure 4: Correlation between TCAD and Spice characteristics (a) $I_{DS}-V_{GS}$ and (b) $C_{GS}-V_{GS}$.

4. TUNNEL-FET BASED OTA

OTA is an integral component of several low power analog designs. In many designs, OTA is the only active component, such as in Gm-C filter synthesis [8], Neural amplifier [7], cellular neural network (CNN) [18], and non-linear functional synthesis [13], and claims to active biasing/operating power. Due to its widespread utilization, we use OTA to demonstrate capability and challenges of TFET based design.

Circuit schematic of TFET-OTA is demonstrated in Fig 5a. Transistors M1 and M2 generate differential transconductance current ($i_d,1$ and $i_d,2$) proportional to the differential input gate voltage ($V_{AC}$), and the current $i_d,1$ and $i_d,2$ is mirrored by the current mirrors M3-M4 (=M5-M6). This mirrored current is added at the branch M6-M8 and supplied to the load at OUT. Due to its improved output resistance [Fig. 3c], TFET based design obviates the cascaded transistors at the output stage [7], and the associated biasing power. Various characteristics of the TFET-OTA are discussed below for varying power conditions, and compared to equivalent MOSFET-OTA designs. Power of the OTA design can be varied by changing $V_{DD}$ or its total bias current ($I_{OTA}$). Since, in a complete system other analog components such as floating switches, biasing elements can limit voltage scaling [16], we restrain our exercise to varying $I_{OTA}$ (and fixed $V_{DD}=1V$). To compensate its degraded output resistance, the channel length for MOSFET based designs was chosen to be $2 \times L_{min}$, where $L_{min}$ is the minimum channel length of the technology.

4.1 Transconductance ($G_m$)

The net trans-conductance gain ($G_{m}$) of OTA is given by

$$G_{m} = g_{m1} \times M$$

(3)

Here, $g_{m1}$ is the trans-conductance of the transistors $M_1$ ($=M_2$), $M_6$ is the current mirror ratio for the mirrors $M_1$-$M_4$ ($=M_2$-$M_6$). Hence, with respect to $I_{OTA}$
Hence, it is observed that the $G_m/IOTA$ for the TFET based MOSFET based OTA designs succumb to excessive leakage and barrier lowering (DIBL), the current of the branch M5-M7 and M6-M8 doesn’t follow the mirror ratio enforced by the design. At extremely low bias currents, due to drain induced barrier lowering (DIBL), the current of the branch M3-M4 and M7-M8 doesn’t follow the mirror ratio enforced by the design. Hence, with scaling $I_B$, for the TFET-OTA at lower power facilitates TFET-OTA to achieve better $f_0$. However, TFET based design suffers from TFET’s higher overlap capacitance (double gated structure with the gate overlapping the source, Fig. 2a) as well. At higher power scenarios, when TFET-OTA’s $G_m$ reduces with respect to MOSFET-OTA, MOSFET based design overtake. At lower bias current, the $f_0$ of TFET-OTA reduces. Nevertheless, near kHz $f_0$ at sub-nW power expense in TFET based designs will be useful for several applications [5,16,19,20].

4.3 Linearity

Although, the subthreshold analog designs enjoy benefits of lower power and greater efficiency, a fundamental deterrent is reduced linearity. For the MOSFET based designs, in the subthreshold, the differential current $i_{d1} (=-i_{d2})$ is reduced linearity. For the MOSFET based designs, in the subthreshold, the differential current $i_{d1} (=-i_{d2})$ is reduced linearity.

$$i_{d1} = \frac{1}{2} \tanh \left( \frac{V_{AC}}{2nV_T} \right)$$

Here, the linearity range is limited to the ac signal magnitude $V_{AC}$ satisfying

$$\frac{3V_{AC}^2}{(2nV_T)^2} \ll \frac{1}{2nV_T}$$

Depending on the $n$ and $V_T$, linearity range is a few mV. For processes with higher $n$ (and hence higher $SS$), the linearity range is higher. However, the fundamental challenge is that the linearity range is process limited. For TFET based designs, when operating region is modulated by the bias current, it exposes a different point $SS$ for transistors M1 (M2). And, it provides unique

$$G_m/IOTA = \frac{G_m}{IOTA} = \frac{G_m}{I_B} \times \frac{1}{M_R + 1}$$

For the TFET OTA design, $G_m/IOTA$ is analyzed by sweeping the $I_B$. With reduced $I_B$ the DC gate-source bias for M1 and M2 moves to lower values, and it enhances its point $SS$ and $g_m/I/O$ [Fig. 3b, Eq. 2]. Hence, it is observed that the $G_m/IOTA$ for the TFET based designs increases at lower $I_B$ (or $IOTA$) as in Fig. 5b.

On the other hand, for MOSFET in the sub-threshold region

$$\frac{G_m}{IOTA} = \frac{G_m}{I_B} \times \frac{M_R}{M_R + 1}$$

Here, $k$ is the Boltzmann constant, $T$ is the temperature, and $n$ is the ideality parameter related to its $SS$. Hence, with scaling $I_B$, for MOSFET based designs $G_m/IOTA$ stays relatively invariant as observed in Fig. 5b. At higher temperature, this ratio is degraded [Eq. 5]. At extremely low bias currents, due to drain induced barrier lowering (DIBL), the current of the branch M3-M4 and M7-M8 doesn’t follow the mirror ratio enforced by the design. MOSFET based OTA designs succumb to excessive leakage, and $G_m/IOTA$ ratio drops. Hence, operating region with the TFET based designs is extended to the ultra-low energy regime and beyond achievable by the MOSFET. Nevertheless, at high power (and performance) conditions, when TFET SS degrades worse than the MOSFET [point $SS$ in Fig. 3b], 90nm CMOS device outperforms TFET for power $> 200nW$, and 45nm for power $> 1\mu W$. 

4.2 Unity gain frequency ($f_0$)

OTA is single pole dominant design, and gain bandwidth product is determined by the unity gain frequency ($f_0$). The $f_0$ of the TFET-OTA was analyzed for a capacitive load of 100fF and for varying $IOTA$ and compared against MOSFET-OTA. Higher $G_m$ of TFET-OTA to MOSFET-OTA at lower power facilitates TFET-OTA to achieve better $f_0$. However, TFET based design suffers from
One of the popular low-power techniques to enhance the linearity of OTA is to use a cross-coupled structure as shown in Fig. 6a. Transconductance of each pair (i.e., \( G_{m1} \) and \( G_{m2} \)) is shown in Fig. 8b. The net transconductance (i.e. \( G_{m,T} \)) achieves a higher linear range, where \( G_{m,1} \) compensates for \( G_{m,2} \) roll-off. Linearity range of operation is extended to \( \sim 40\text{mV} \). However, a greater improvement is limited by intrinsic non-linearity of MOSFET in subthreshold region. Similar structure was experimented with TFET. By changing \( I_B \) several gate-source bias conditions (i.e., \( V_{CM,VM} \)) were enforced. At higher \( V_{CM,VM} \) linearity range is significantly increased [Fig. 6c].

5. TUNNEL-FET BASED NEURAL AMPLIFIER

Implantable neural amplifiers have found widespread utilization in health-care and monitoring. Non-invasive implementation of neural amplifier poses stringent energy limitations. Under these power constraints, OTA based neural amplifier design was proposed by Harrison et al. [7], where the OTA functions in the subthreshold region. Greater details of this design can be found in the work within. And, we limit the scope to emphasize benefits of TFET based implementation of this design.

The circuit schematic of OTA based neural amplifier is demonstrated in Fig. 7a. Feedback configuration of OTA is realized by the capacitance \( C_1 \) and \( C_2 \), and the Mid-band gain is set by \( C_1/C_2 \). Gate and source of p-transistors \( M_{1-8} \) are connected together to realize highly resistive pseudo-resistance. The low frequency cut-off (\( f_c, \text{low} \)) is designed to filter off Flicker noise, and it is set by \( 1/(R_{MC2}) \). Here, \( R_{M} \) is the incremental resistance generated by the pseudo-resistance \( M_{1-8} \). Design requirements for \( f_c, \text{low} \) to be in \( \sim \text{mHz} \) requires \( R_{MC2} \) time constant to be very large. However, limited chip area for implantable applications can impose restriction on the physical area of \( C_2 \) and hence use of transistors in high resistive configuration was proposed [7].

We realize the similar design with TFET. The mid-band gain was designed to be 50, with \( C_1=500\text{fF} \), and \( C_2=10\text{fF} \). Various other characteristics of this design are listed in Table 4. TFET based OTA design due to its ultra low energy operability pushes the power requirement to \( \sim 3\text{nW} \). Due to its lower off-current TFET based pseudo-resistance are more resistive, and even with \( C_2=10\text{fF} \) high pass cut-off frequency \( 36\text{mHz} \) is attained [Fig. 7b]. However, uni-directionality of TFET, requires two anti-parallel paths as shown. Lower size requirement on \( C_2 \) also relaxes power requirement for the OTA which is now required to drive smaller load (\( C_1 \) and \( C_2 \)).

6. NOISE CHARACTERISTICS

For the intended low frequency designs with TFET, the Thermal noise, Flicker noise, and Shot noise characteristics are important. Flicker noise characteristics of TFET were studied experimentally [4,17]. Similar to MOSFET, in V-TFET Flicker noise falls off exponentially with \( 1/f \) trend [4]. However, for horizontal TFET, \( 1/f \) roll off in frequency spectrum was observed [17]. The effect of Flicker noise can be minimized by incorporating a high pass filter to filter off excessive noise at lower frequencies [as in Neural amplifier design]. Also, large gate area can be chosen to minimize the impact of Flicker noise [7].

Thermal noise and Shot noise modeling and experiments of TFET have not received much attention. In the absence of relevant literature, we utilize tunnel diode noise studies to understand Thermal noise and Shot noise in TFET. Tunnel diodes have similar structure to TFET [except the gate terminal], where current conduction through degenerately doped junction occurs through BTBT. Shot noise in these structures occurs at the tunneling junction, where due to discreteness of carriers the number of electrons (holes) tunneling across the barrier fluctuates. Thermal noise occurs at the channel and drain region, where the carriers cross over the barrier with their thermal energy, and create fluctuation in the current. Equivalent noise models for the Tunnel diode was proposed [2] as seen in Fig. 8a. Here, \( i_{Th}^2 \) is the noise current density due to the Thermal noise, and \( i_{Th}^{22} \) is the noise current density due to the Shot noise. \( r_{Th} \) is the resistance associated with the Thermal noise, and \( r_s \) is the tunnel resistance associated with the Shot noise. The equivalent voltage noise at the drain terminal with load \( r_L \) can be given by

\[
\nu_{D,\text{noise}}^2 = \frac{i_{Th}^2}{r_L} + \frac{i_{Th}^{22}}{r_s} \Delta f
\]

Due to significant barrier height and width \( r_s \gg r_{Th} \), Hence,

\[
\nu_{D,\text{noise}}^2 = \frac{i_{Th}^2}{r_L}
\]

Thus, the effect of Shot noise in these structures becomes more prominent. By similarity of current conduction mechanism in TFET to Tunnel-diode, we argue that equivalently the TFET Shot noise can be modeled as [2]

\[
i_{Th}^{22} = 2qG_{DS}\Gamma(V_{GS},V_{DS})
\]

Here, \( I_{GC} \) is the bias current through device. \( \Gamma(V_{GS},V_{DS}) \) is termed as Fano factor [11], and it depends on the biasing conditions. Through modeling and experiments in Tunnel-diode, it was shown that \( \Gamma \) significantly increases at low bias current [11].
referred noise of the OTA [as in Fig. 7a] can be obtained analytically. Utilizing Shot noise model [Eq. 11], the input referred noise increases. Thus, Shot noise imposes a simplistic assumption (\(s\)ensors for low-throughput applications. The noise study shows intriguing opportunities for ultra-low-power analog circuits and TFET based pre-amplifier design with \(\sim\)nW power raises.

Additional benefits of subthreshold-TFET based design are shows sub-nW operation is possible at kHz of bandwidth.

The bandwidth-power trade-off in ubiquitous sensors with an low off-current and higher \(g_m/\overline{I_d}\) are promising for such applications. An early design exploration of TFET based OTA shows sub-nW operation is possible at kHz of bandwidth. Additional benefits of subthreshold-TFET based design are reduced temperature sensitivity and higher output resistance. TFET based pre-amplifier design with \(-nW\) power raises intriguing opportunities for ultra-low-power analog circuits and sensors for low-throughput applications. The noise study shows that the Shot noise can become an obstacle to greater power reduction in TFET based designs.

7. CONCLUSIONS

The bandwidth-power trade-off in ubiquitous sensors with an ultra-low energy demand can be limited by excessive leakage and limited SS in MOSFET. Steep-subthreshold devices with ultra low off-current and higher \(g_m/\overline{I_d}\) are promising for such applications. An early design exploration of TFET based OTA shows sub-nW operation is possible at kHz of bandwidth. Additional benefits of subthreshold-TFET based design are reduced temperature sensitivity and higher output resistance. TFET based pre-amplifier design with \(-nW\) power raises intriguing opportunities for ultra-low-power analog circuits and sensors for low-throughput applications. The noise study shows that the Shot noise can become an obstacle to greater power reduction in TFET based designs.

8. ACKNOWLEDGMENTS

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