ELEN 689 – 606
Techniques for Layout Synthesis and Simulation in EDA
Project Report

On Chip Active Decoupling Capacitors for Supply Noise Reduction for Power Gating and Dynamic Dual Vdd Circuits in Digital VLSI

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ABSTRACT

An active decoupling circuit is proposed to suppress on-chip power supply noise in digital VLSI circuits with focus on circuits using low power methodologies like power gating and Dual Vdd. The circuit is designed using 180nm technology and is tested for an ISCAS benchmark for effectiveness in suppressing noise effects as compared to passive decoupling capacitors and previous works. We show a boost of around 33X in the decoupling capacitance values over conventional passive capacitors. The noise rejection is shown to be around 8dB.

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I. INTRODUCTION

On-chip supply voltage fluctuations in digital VLSI circuits pose a major threat to robust circuit operation affecting speed, power, noise margin, and long term reliability [1]. In today's deep sub-micron CMOS technology, as devices scale down to smaller feature sizes, have faster switching speeds, and higher integration density, large current spikes due to a large number of "simultaneous" switching events in the circuit within a short period of time can cause considerable current–resistance (IR) drop and Ldi/dt noise over the power-supply network [2]. The wire impedance however does not scale as desired. Power-supply noise degrades the drive capability of transistors due to the reduced effective supply voltage seen by the devices. Power-supply noise may also introduce logic in VLSI circuits, since the noise margin gets lower as the supply voltage scales with the technology.

One solution to the power signal integrity issue, as many call it, has been to apply passive decoupling capacitors (Passive Decaps for short). However, now, again with scaled technologies, problems have started creeping up with Passive Decaps [1]. The problems are as under:

- Gate tunneling leakage: Gate oxide breakdown (10% of Leakage Power)
- Large die area consumption (15 – 20% High End Microprocessors).

These problems call for a better scheme for noise reduction: **Active Decoupling Capacitors (Active Decap).**

The concept of Active Decap was first used effectively for suppressing crosstalk in deep sub-micron CMOS Mixed-Signal SOCs [3]. Very recently, distributed Active Decaps were used for On-Chip Power Supply Noise Reduction [1]. However, the design used by them was a more general design and we in this project seek to design an Active Decap circuit with noise caused due to power gating and voltage switch in Dual Vdd circuits.

Next, we discuss the principle behind the Active Decoupling and how it differs from Passive Decoupling. A concept which is very core to the principle of Active Decoupling is Miller effect is also described.

A. Active Decoupling Principle & Miller Effect

As shown in figure 1, the capacitor Cload in the feedback loop acts as the Decoupling Capacitor. This capacitance is multiplied by the gain A(ω) through Miller Effect, and therefore, increases the effective capacitance seen between the input terminals.

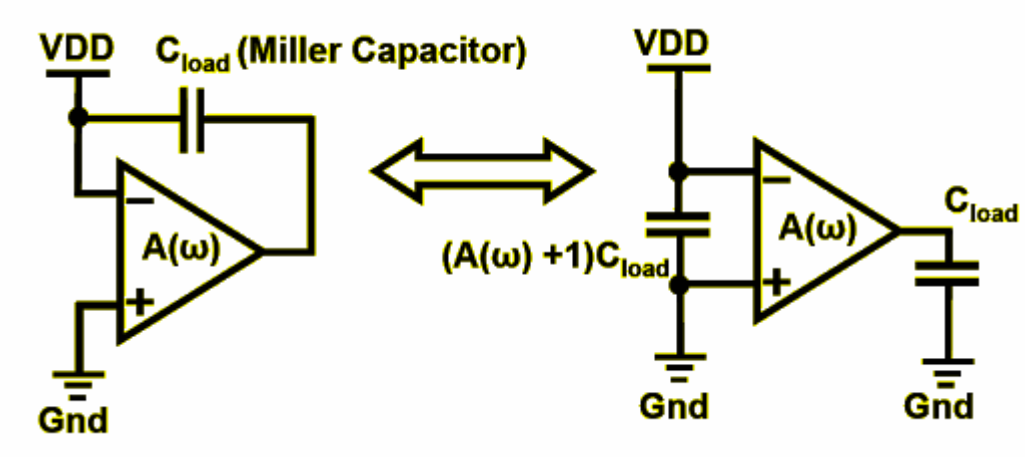

Figure I: Concept of Active Decoupling and Miller Effect

The Miller Effect is as described below with reference to figure 2 [4]:

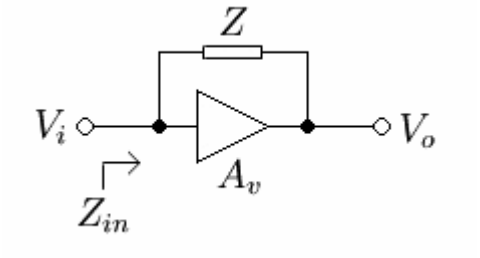

Figure II: Miller Effect

Consider an ideal voltage amplifier of gain A_v with an impedance Z connected between its input and output nodes. The output voltage is therefore $V_o = A_v V_i$ and the input current is

$$I_i = \frac{V_i - V_o}{Z} = \frac{V_i(1 - A_v)}{Z}$$

and the input impedance is

$$Z_{in} = \frac{V_i}{I_i} = \frac{V_i Z}{V_i(1 - A_v)} = \frac{Z}{1 - A_v}.$$

If Z represents a capacitor, then

$$Z = \frac{1}{j\omega C}$$

and the resulting input impedance is

$$Z_{in} = \frac{1}{j\omega C(1 - A_v)} = \frac{1}{j\omega C_{eff}} \quad (C_{eff} = C(1 - A_v)).$$

Thus the capacitance is effectively multiplied by the factor $(1 - A_v)$. However, since we are using the op-amp in negative feedback configuration, the effective capacitance for our design is $(1 + A_v)$ times C.

B. Active Decoupling Versus Passive Decoupling

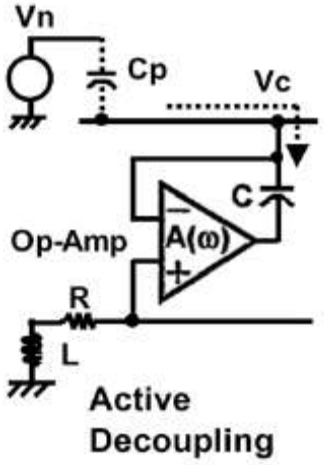

Figure III: Active Decoupling

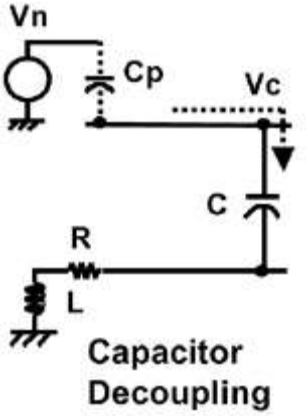

Figure IV: Passive Decoupling

Here we shall demonstrate the difference between Active Decoupling and Active Decoupling with the aid of simple configurations shown in Figures III and IV. The noise voltage Vn is coupled through capacitance Cp to node voltage Vc to which decoupling capacitor C is connected [3].

Level of Noise Coupling is given by the ratio Vc / Vn.

$Vc/Vn = (Cp/C)\{1+j\omega C(R+j\omega L)\}/\{1+j\omega Cp(R+j\omega L)\}$……..for passive decoupling

$Vc/Vn = Cp/[\{1+A(\omega)\}C]$……...for active decoupling

where R and L are parasitics.

Thus, Active Decap suppresses Vn more by a factor of $(1+A(\omega))$ than Passive Decap at low frequencies

At high frequencies, above parasitic resonant frequencies, the noise coupling increases.

C. Contributions

By the means of this project, we design a Distributed Active Decoupling Circuit that effectively suppresses power noise with special attention to Power Gating. We also propose ideas that might be effective for the case of Dual Vdd circuits. The reduction power noise is a necessity now, as we scale down to lower technologies and also make the Noise Margins slimmer. Of course, we begin by showing the effectiveness of Active Decoupling Circuits compared with passive decoupling circuits.

The rest of the report is organized as follows: Chapter 2 discussed some previous work. Then, in Chapter 3, we describe the designing of the op-amp based on the parameters given in [1] and then suggest ways to modify it to suit our application. Here we also describe out simulation methodology. Based on this background, we discuss the results in Chapter 4 and conclude with suggested future work and conclusions drawn in Chapter 5.

II. PREVIOUS WORK

As touched upon in Chapter 1, Active Decaps are expected to be used first for noise reduction by [3] to suppress crosstalk in deep sub-micron CMOS Mixed-Signal SOCs.

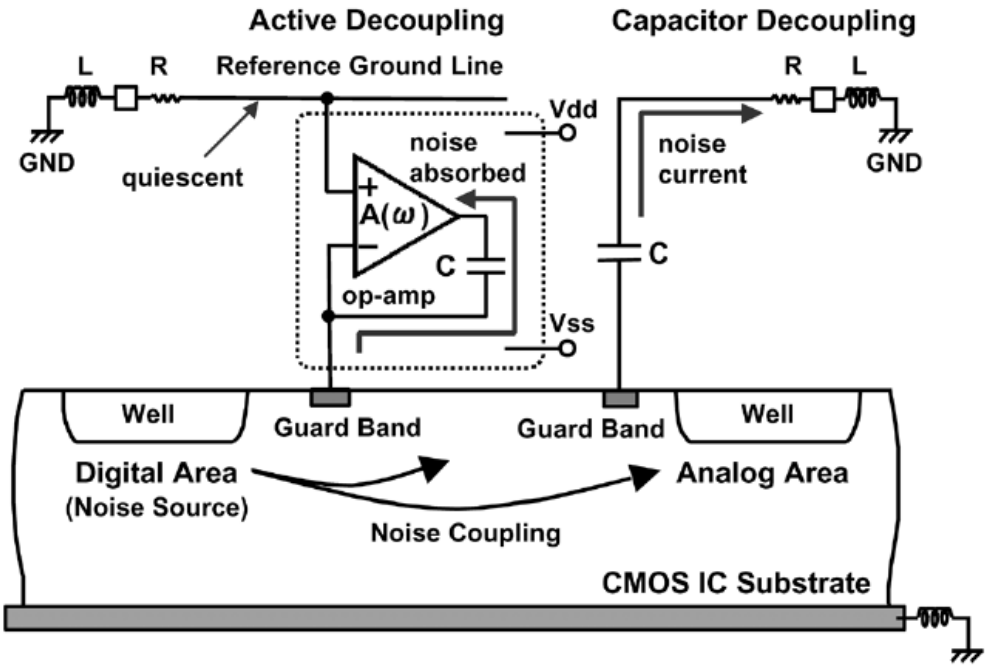

Figure V: Suppression of Substrate Cross-talk using Active Decoupling, *Source: [3]*

Their work can basically be described as: In active decoupling, a guard band suppresses the spread of substrate crosstalk from the digital area to the analog one. The negative input of the op-amp is connected to the guard band, and the positive input is connected to the reference ground line, which leads to the off-chip common ground. The capacitor, C, in the feedback loop of the op-amp acts as a decoupling capacitor. Its capacitance is multiplied by the gain, A(ω), through the Miller effect. The resulting negative feedback causes the guard band to be virtually shorted to the reference ground line. The noise current from the substrate, which is the crosstalk, is thereby absorbed in the op-amp and flows into the pair of power supply lines, Vdd and Vss, rather than into the reference ground line. The ground line is thus kept quiescent, and the guard band is virtually

grounded by this stable ground line. In contrast, the noise current does flow into the ground line in capacitor decoupling, often causing a large ground bounce at high frequencies due to the parasitic inductance, L. Therefore, effective decoupling is usually not attained at higher frequencies.

Active Decaps were used recently by [1] for reducing power supply noise in Digital VLSI effectively. We shall be using their design specifications as a starting point. We summarize their work here with a diagram.

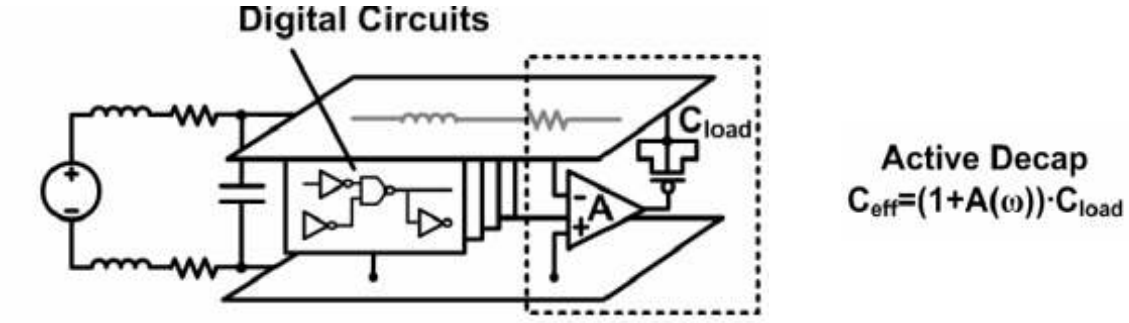

Figure VI: Reduction of power supply noise in Digital VLSI circuits, *Source: [1]*

III. DESIGN METHODOLOGY AND RESULTS

The main element of the Active Decoupling Circuit, as far as the designing challenge goes, is the operational amplifier with the desired gain and phase response. We use the same specifications as in [1] for an initial design and then modify it as and when needed.

We again state what we seek to achieve. We use the same principles for noise reduction with specific reference to reducing noise in power gating and Dual Vdd VLSI circuits.

- Power Gating: Noise when transitions in control signal to the power gating transistors
- Dual Vdd: Noise when there is a switch from one Vdd (say Vdd high / Vddh) to other (say Vdd low / Vddl)

As described before, a major part of the noise is produced due to a sudden loading after a clock gating or a power gating event. Henceforth, we address the power gating issue and propose a methodology for the Dual Vdd noise reduction.

A. Op-Amp Design

The Specifications for the design of the op-amp are:

Current: 3.8mA

DC Gain: ~20dB

BW: ~500Mhz

UGF: 2.2 Ghz

PM = 40 degrees

A signal to function as the On / Off switch

Figure VII illustrates a top-view of the design and the figure VIII gives the schematic of our design

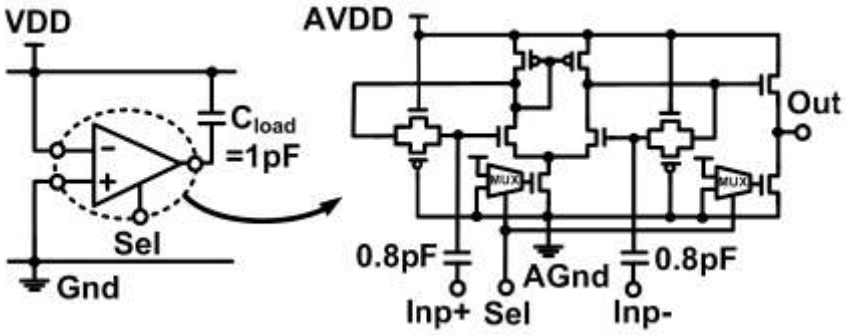

Figure VII: Top-view of the op-amp schematic

The first stage of the op-amp is simply a differential amplifier with a differential pair and a current mirror. The next stage is a source follower which functions as a simple output stage because some of its interesting design parameters. The first step in the designing is to distribute current between the tail of the differential stage and the tail of the source follower. Then, the task remains is to size the other transistors accordingly, ensuring at each step that all the transistors of the op-amp are in saturation region at all times. The Muxes shown in the schematic are to facilitate the on-off facility. When Sel = 0, no biasing goes to the tails and so the active decoupling circuit shuts down.

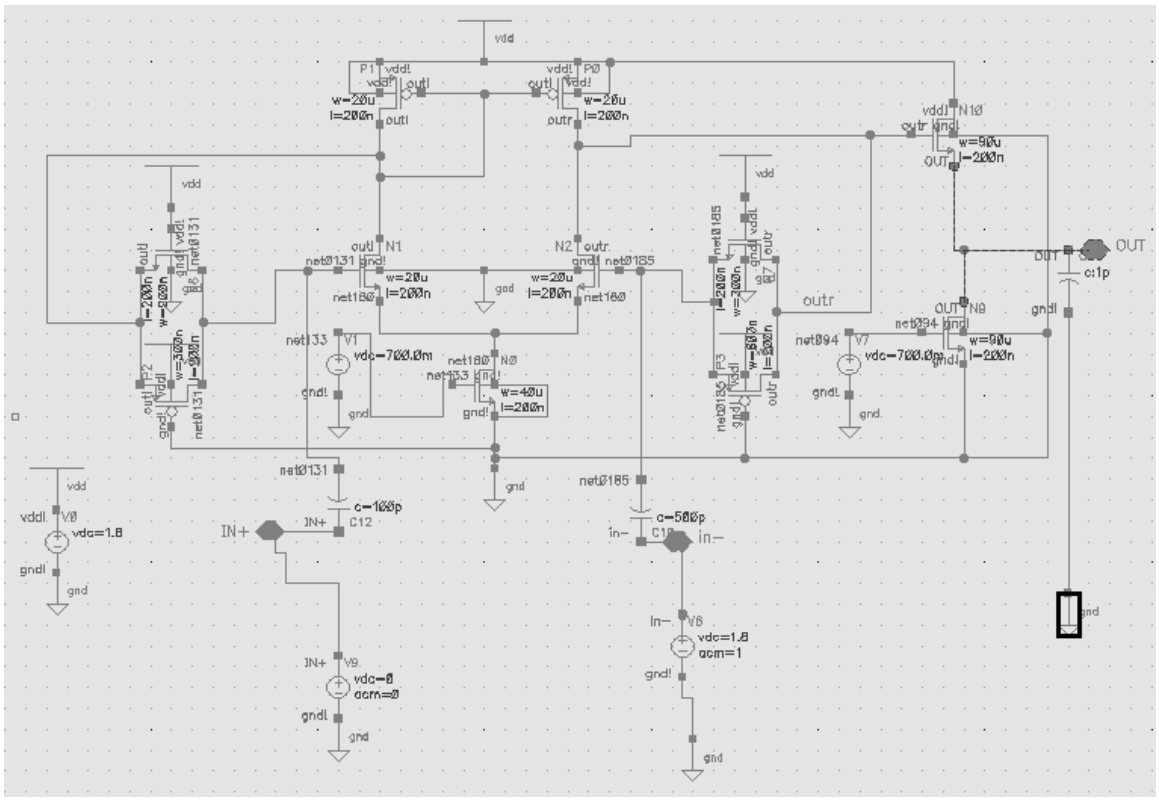

Figure VIII: Schematic of the designed op-amp

Figure IX gives the gain and phase plots of the designed op-amp.

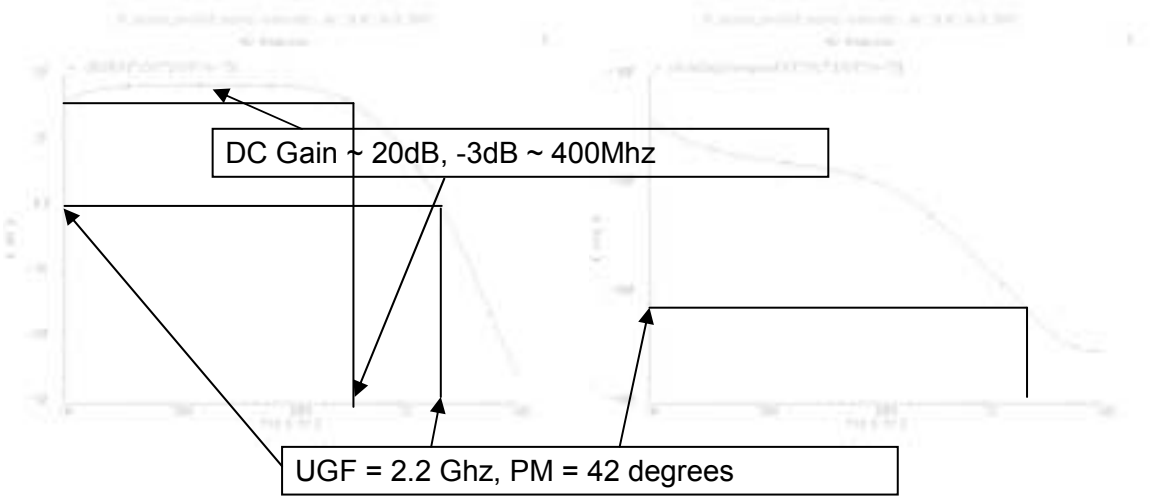

Figure IX: Gain and Phase Plots of the designed op-amp

B. Simulation Methodology

The main points of the simulation methodology are as under:

- Tested for ISCAS85 Benchmark C432 (160 Gates)
- Methodology easily scalable to other benchmarks
- Tests carried out
    - Random noise generated by power gating control signal, clock like signal given, rise time 50ps - 1nS, period 16ns, tests for other values also carried out, noise generally occurs during rise/fall
    - Random noise as above + sine wave superimposed on the Vdd signal
- Benchmark placed and routed using Silicon Ensemble and merged extracted spice netlist with dspf extracted parasitics.
- Op-amp designed using Virtuoso Schematic
- Op-amp tested for open loop parameters using cdsSpice
- Whole test-case simulated using Hspice
- For dual Vdd assumed grid routing for power routing.

Figure X summarizes the experimental setup graphically.

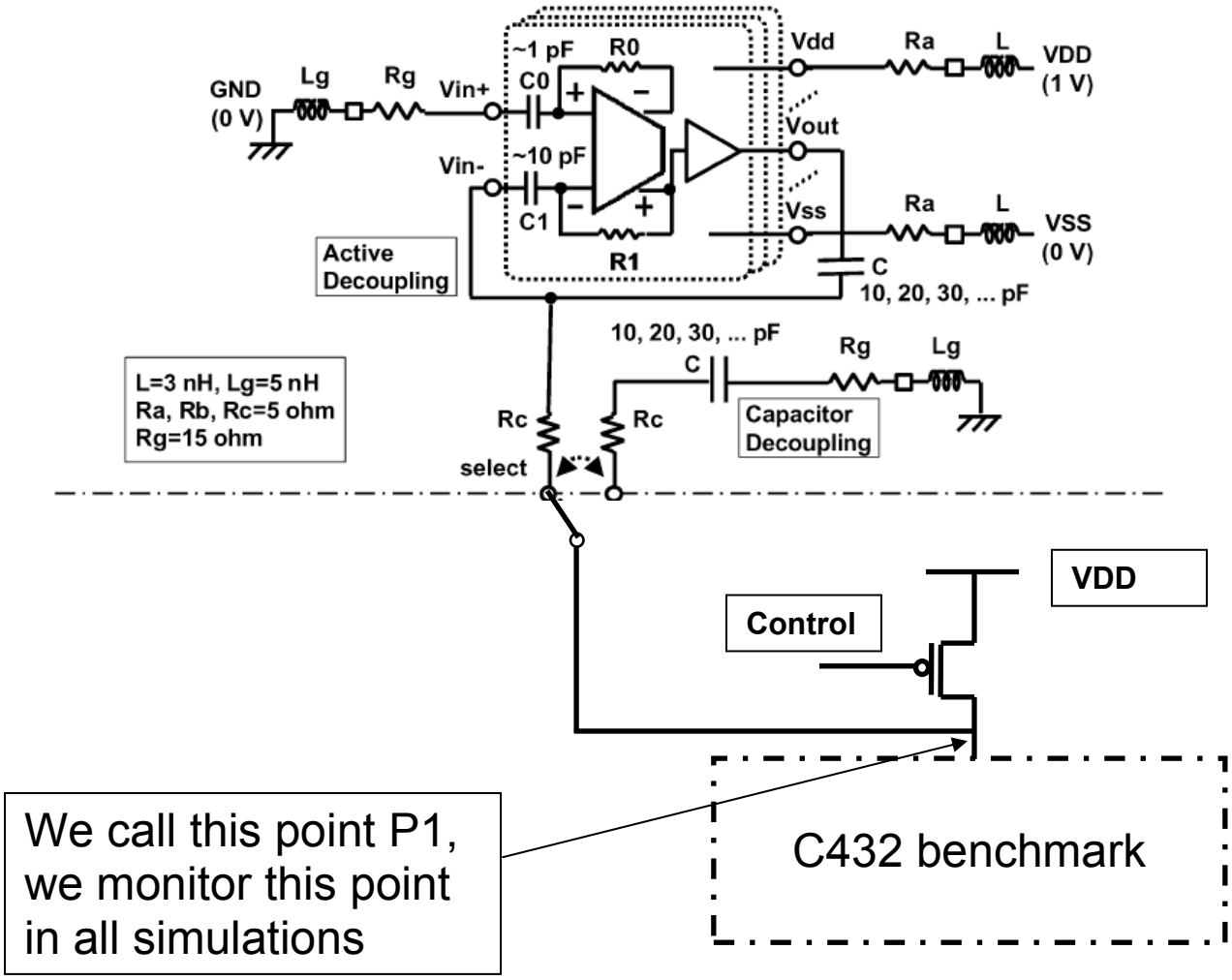

Figure X: Experimental Setup

C. Results

We now summarize the simulation results.

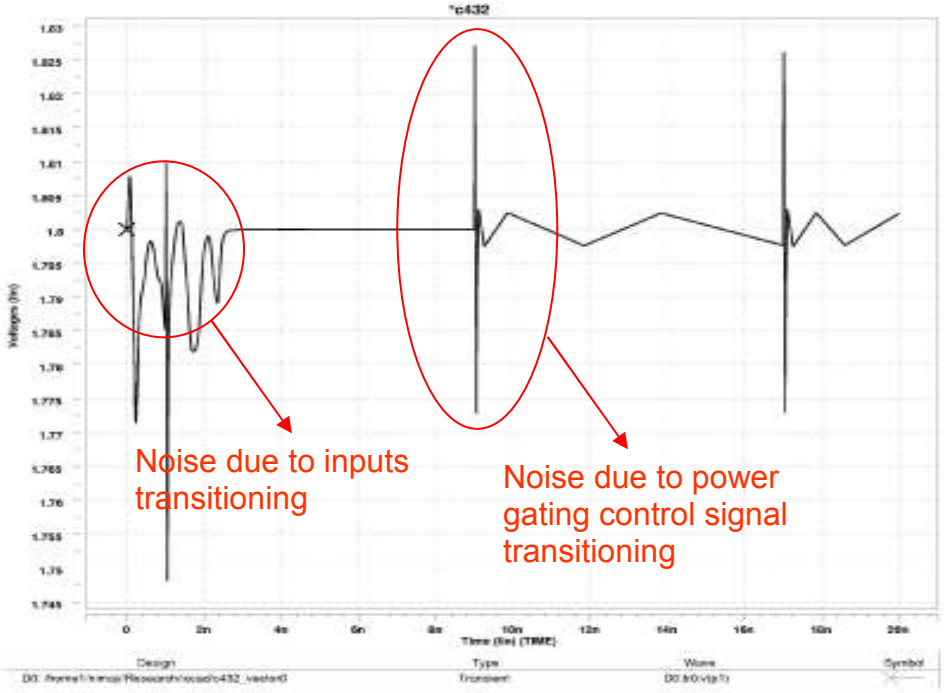

Figure XI: Figure showing the different noise present in simulation

The waveform in figure XI shows noise generated due to a) inputs transitioning and b) power gating. The approximate value of the noise signal is 0.06Vpp.

The next waveform distinguishes the noises present in to high frequency and low frequency noises. The next waveform in figure XIII shows that if we use the same design as [1], we can effectively filter out the low frequency noise components. However, there is not much effect on the high frequency noise components. This tells us that we need to improve the design so that we can apply it to the power gating noise reduction application.

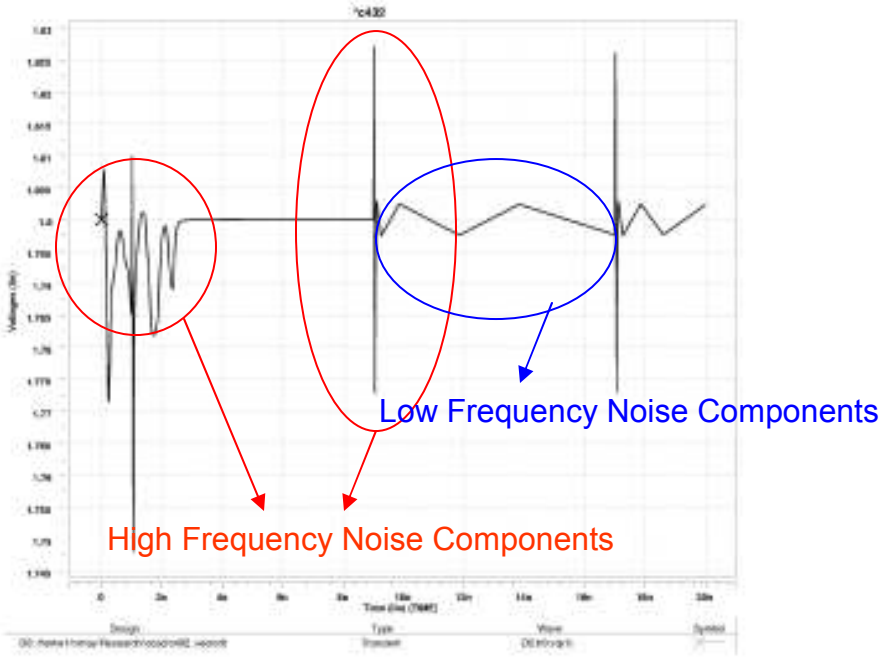

Figure XII: Figure distinguishing between the different noise components

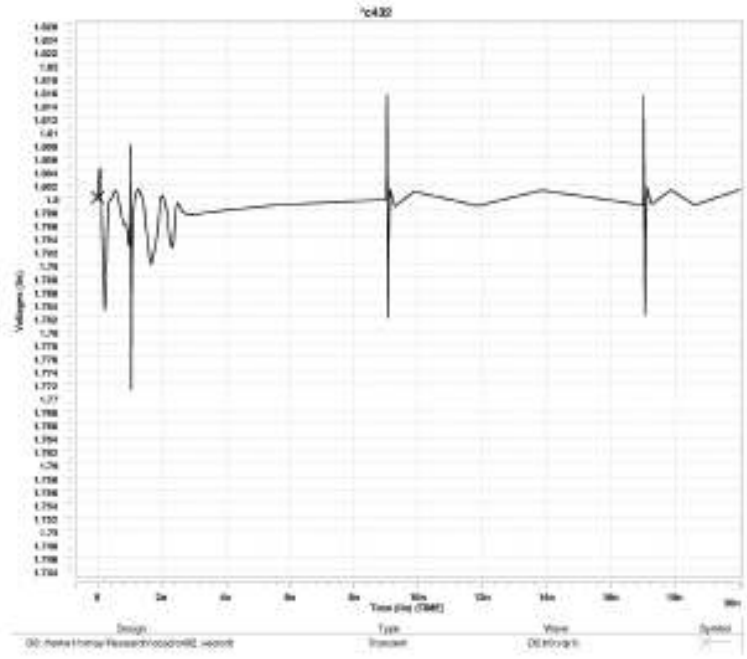

Figure XIII: The filtering result of waveform of figure XII

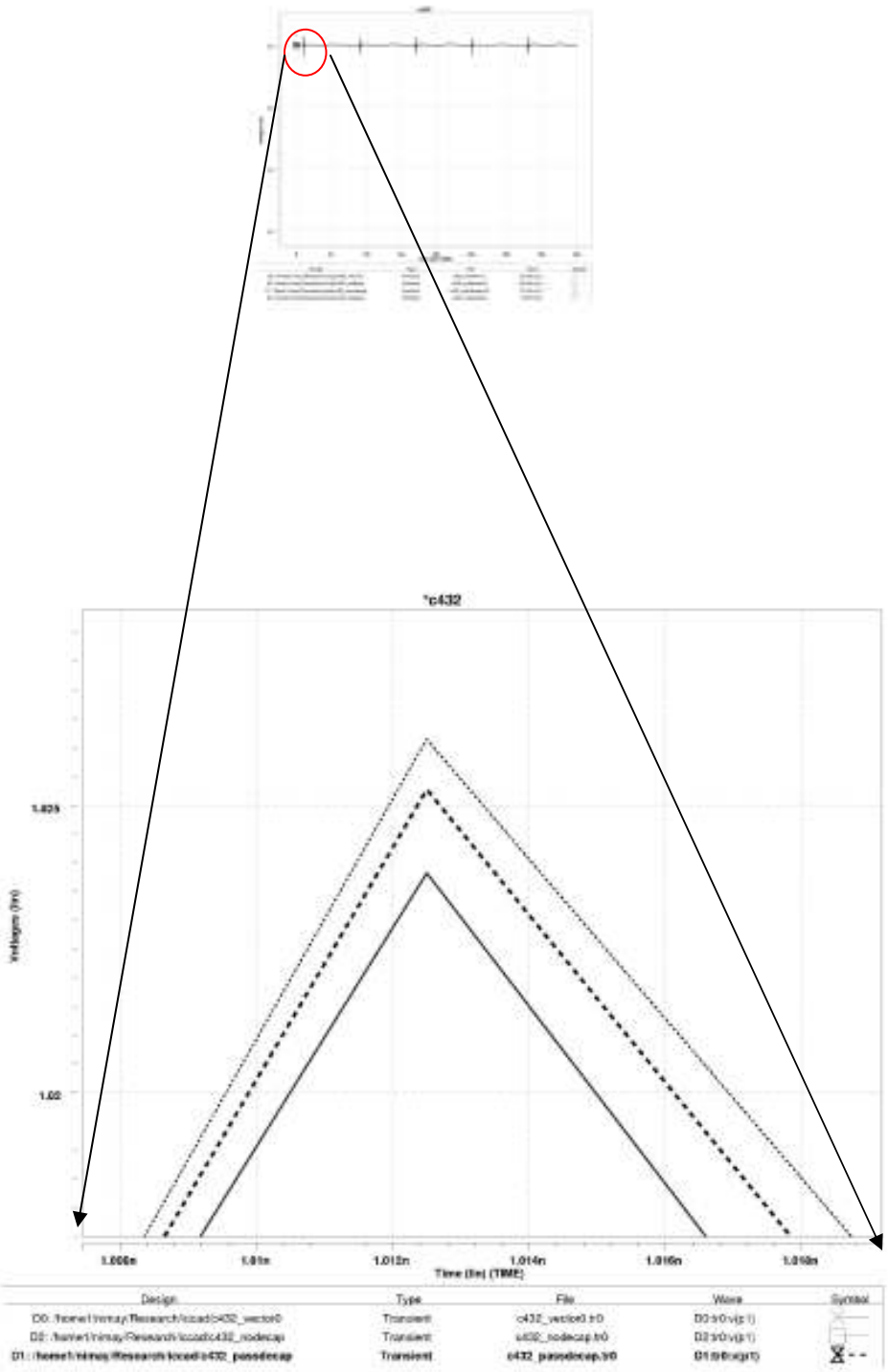

Figure XIV: Higher effectiveness of Active Decap as compared to Passive Decap as compared to No Decap.

In Figure XIV, we consider a noise peak and compare active and passive decoupling. As indicated by the legend, the topmost curve is original noise, the one below it is noise after passive decap and the last one is with active decap.

Now, we quantitatively show the higher effectiveness of Active Decoupling. In figure XV, we calculate the noise rejection in dBs. Quantitatively, noise rejection for active decap case = -7.95dB and for passive decap = -1.93dB

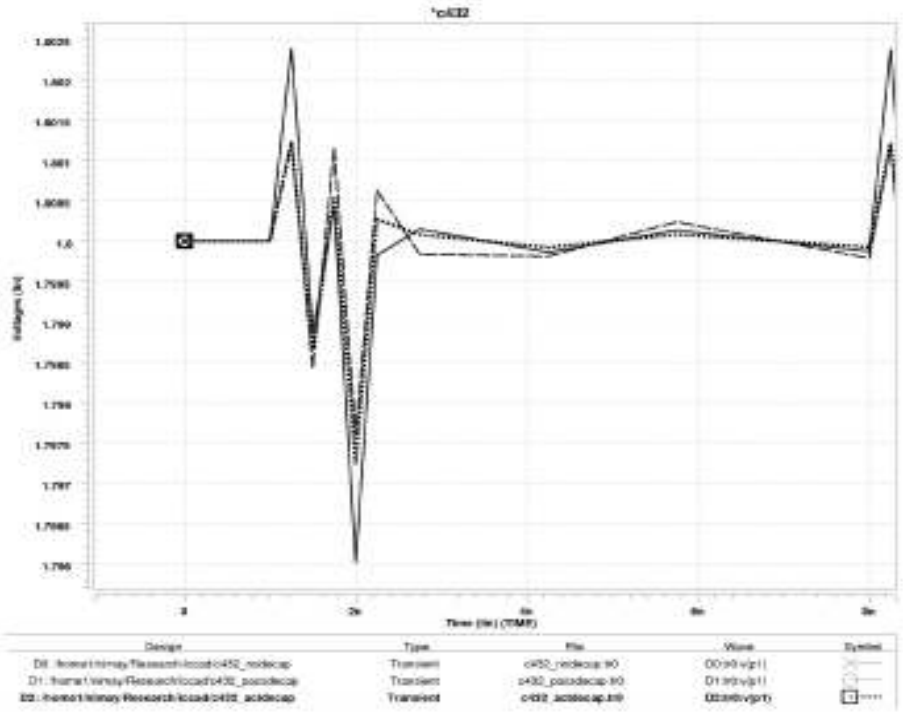

Figure XV: Quantitative formulation for noise rejection by the two different methods

Finally in figure XVI, we show the 33X reduction in capacitor size which leads to considerable area savings. Here we see that a Passive Decap of 1000fF is almost as effective as an Active Decap with a capacitor of 30fF in its feedback loop. An approximate calculation using Vc/Vn equations discussed before indicates an A(ω) of 15dB

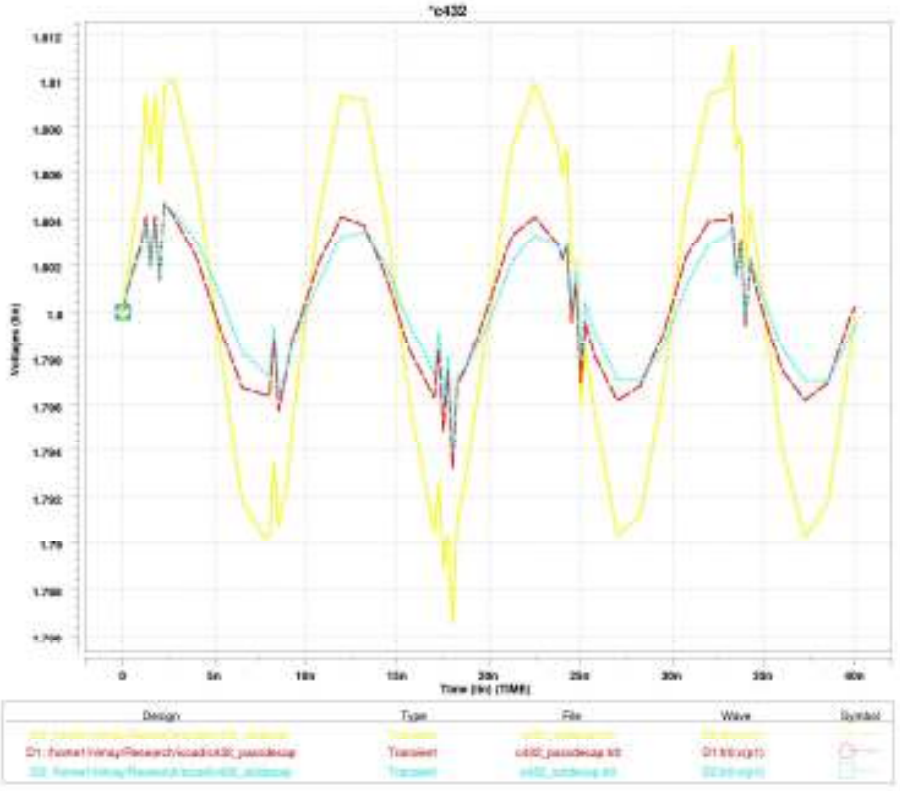

Figure XVI: Waveform showing a 33X reduction in capacitor size

IV. CONCLUSION AND FUTURE WORK

To summarize, we can conclude the following:

- Active Decoupling reduces noise more effectively and with lesser area overhead in case of power gating
- Op-Amp design needs modifications for accommodating high frequency noise rejection
- This is brought about by a gain and bandwidth tradeoff by adjusting the feedback resistance of second pass transistor
- Gain can be increased by replacing the output stage (source follower right now) to some other stage like a common source configuration

Also, we can say that the Dual Vdd noise rejection is a bigger challenge based on the following observation:

If the active decap is kept always ON, it will sense the transition from one Vdd to the other as noise too and because of the large RC time-constant this transition will be slowed down

A possible solution to this problem can be to use a signal to selectively switch on and switch off the active decap circuit. A straightforward signal could be a delayed version of the control signal used for Vdd switching and have different active decap circuits for both Vdds. However, we have to be careful. We also need to take steps to avoid crosstalk between the two active Vdd circuits. The ‘ON’ / ‘OFF’ concept can be taken from [1], also used for power optimization of the active decap circuits. Also we can try and make the circuit more active by trying out the ‘Charge Pump’ method. That also might be a candidate solution to the Dual Vdd challenge.

REFERENCES

[1] J. Gu, et al., “Distributed Active Decoupling Capacitors for On-Chip Supply Noise Cancellation in Digital VLSI Circuits,” in *2006 Symposium on VLSI Circuits Digest of Technical Papers*

[2] S. Zhao, et al., “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Floorplanning,” in *IEEE Trans. On Computer Aided Design of Integrated Circuits and Systems*, Vol. 21, No. 1, January 2002, pp. 81 – 92

[3] T. Tsukada, et al., “An On-Chip Active Decoupling Circuit to Suppress Crosstalk in Deep-Submicron CMOS Mixed-Signal SoCs,” in *IEEE J. of Solid-State Circuits*, vol. 40, no. 1, pp. 67−79, Apr. 2005

[4] www.wikipedi.org