Phase Noise Modeling for Integrated PLLs in FMCW Radar

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Abstract—The effect of frequency modulation on the phase-noise spectrum of a charge pump (CP) phased-locked loop (PLL) for FMCW radar is investigated. The static phase error is calculated as a function of frequency ramp slope and basic PLL design parameters. The phase-noise spectrum under frequency modulation is deduced from the spectrum in the steady state. Design guidelines for integrated PLLs to be used in FMCW radar are derived from theoretical considerations and experimental results from the literature.

Index Terms—frequency synthesizer, phase-locked loop, FMCW radar, phase noise

I. INTRODUCTION

INTEGRATED transceivers are needed for low-cost ranging systems. Several ranging methods such as pulse-radar, UWB radar and frequency modulated continuous wave (FMCW) radar are possible candidates. FMCW has the advantage of not requiring a high peak-to-average power ratio (PAPR) or wideband operation. A 77 GHz FMCW radar transceiver IC with an accurate FMCW chirp signal generator using a 90 nm CMOS process was presented in [1]. Here, a direct digital frequency synthesizer (DDFS) drives a 77 GHz integer-N PLL. As an alternative, a fractional-N PLL can be used in conjunction with a constant input frequency as the FMCW generator [2], [3].

Regardless of the method used, FMCW radar requires a linear frequency ramp at high frequencies. When realized as a PLL, its output frequency \( f(t) \) must be swept over a sweep bandwidth \( b_s \) within a sweep duration \( T_s \). For a high resolution and short-range radar, the ramp slope \( b_s/T_s \) must be large, which drives the PLL away from the steady state. This raises the question of how frequency error and phase error at the PD input are affected by the frequency drift. Moreover, the dependence of the phase-noise spectrum on the ramp slope and on PLL design parameters must be understood in order to find a good compromise between spatial resolution and noise performance.

In this paper, we deduce the phase-noise spectrum under frequency modulation (FM) approximately from a steady-state situation without FM and derive PLL design guidelines.

II. CALCULATION OF PHASE ERROR

A. Derivation of differential equation

For our calculation we consider a standard second-order charge pump (CP) PLL as depicted in Fig. 1. The PD is composed of a phase-frequency detector (PFD) and a CP. The UP input of the PFD is driven by a reference signal with phase \( \phi_{REF}(t) \). The VCO output frequency is divided by \( N \) and the divider output is connected with the DOWN input of the PFD. Assuming that the phase \( \phi(t) \) of the divided signal lags the reference phase, the CP will generate a positive current flowing through the first-order loop filter. This will increase the VCO control voltage \( V(t) \) and the VCO output angular frequency \( \omega(t) \).

A frequency drift of \( \omega(t) \) can be obtained by changing the reference (angular) frequency \( \omega_{REF}(t) = d\phi_{REF}/dt \) as in [1], or by changing the divider ratio \( N \) in small steps as in [2], [3]. The latter approach requires a fractional-N PLL with fine frequency steps. We consider a PLL with a reference frequency ramp in the remainder:

\[
\phi_{REF}(t) = \omega_{REF}(0) + \alpha_{REF} t,
\]

where \( \alpha_{REF} = 2\pi \left( df_{REF}/dt \right) \) is the angular acceleration. We define the phase error at the PD input by

\[
\phi_e(t) = \phi_{REF}(t) - \phi(t).
\]

Its first derivative is given by

\[
\frac{d\phi_e(t)}{dt} = \omega_{REF}(t) - \frac{d\phi(t)}{dt}.
\]

Substituting (1) in (3) we obtain the second derivative given by

\[
\frac{d^2\phi_e(t)}{dt^2} = \alpha_{REF} - \frac{d^2\phi(t)}{dt^2}.
\]

Fig. 1. Schematic of second-order charge-pump PLL.
This equation will be useful to eliminate $\phi(t)$ from the differential equation describing the loop dynamics.

In the following, we consider a linear, time-invariant continuous-time model (CTM) to keep the analysis of the FM-induced phase error as simple as possible. In reality, a CP-PLL behaves like a time-discrete system as shown in [4] for integer-N PLLs. The time-varying behavior of all-digital PLLs has been discussed in [5]. A CTM combined with linear for integer-N PLLs. The time-varying behavior of all-digital continuous-time model (CTM) to keep the analysis of the differential equation describing the loop dynamics.

Replacing the current by the phase error using (6) we find

$$\frac{d^2\phi_e(t)}{dt^2} = \frac{2\pi K_{PD} K_{VCO} R}{N} \frac{d\phi_e(t)}{dt} + \frac{2\pi K_{PD} K_{VCO}}{CN} \phi_e(t).$$

Finally, we eliminate $\phi(t)$ by using (4) and obtain an inhomogeneous second-order differential equation

$$\frac{d^2\phi_e(t)}{dt^2} + \frac{2\pi K_{PD} K_{VCO}}{N} \frac{d\phi_e(t)}{dt} + \frac{2\pi K_{PD} K_{VCO}}{CN} \phi_e(t) = 0. \quad (14)$$

B. Solution of differential equation

In a first step, we consider the steady state defined by $\frac{d\phi_e(t)}{dt} = 0$. Strictly speaking, a steady state cannot exist due to the finite sweep duration $T_s$. However, if $T_s$ is larger than the PLL settling time $t_s$, we can approximately assume a steady state for the time interval $T_s > t > t_s$. In this case, we obtain from (14) the steady-state phase error

$$\phi_e^0 = \frac{CN_{\text{REF}}}{2\pi K_{PD} K_{VCO}}. \quad (15)$$

Substituting (5) into (15) we obtain

$$\phi_e^0 = \frac{CN_{\text{REF}}}{I_{CP} K_{VCO}}. \quad (16)$$

Replacing $\alpha_{\text{REF}}$ with sweep bandwidth $b_s$ (in units of Hz) and sweep duration $T_s$ according to

$$N\alpha_{\text{REF}} = \frac{2\pi b_s}{T_s} \quad (17)$$

we obtain

$$\phi_e^0 = \frac{2\pi C b_s}{I_{CP} K_{VCO} T_s}. \quad (18)$$

In order to solve (14) for the general case, we define the dynamic phase error $\phi_e^d(t)$ by

$$\phi_e(t) = \phi_e^d(t) + \phi_e^0. \quad (19)$$

Substituting (19), (15) and (5) into (14) we obtain the homogeneous differential equation

$$\frac{d^2\phi_e^d(t)}{dt^2} + \frac{I_{CP} K_{VCO} R}{N} \frac{d\phi_e^d(t)}{dt} + \frac{I_{CP} K_{VCO}}{CN} \phi_e^d(t) = 0. \quad (20)$$

This is the well-known differential equation describing a damped harmonic oscillator [7]. Introducing the damping constant $\gamma$ and the angular frequency $\omega_0$ by

$$\gamma = \frac{I_{CP} K_{VCO} R}{2N} \quad (21)$$

and

$$\omega_0 = \sqrt{\frac{I_{CP} K_{VCO}}{CN}}, \quad (22)$$

we can write (20) as

$$\frac{d^2\phi_e^d(t)}{dt^2} + 2\gamma \frac{d\phi_e^d(t)}{dt} + \omega_0^2 \phi_e^d(t) = 0. \quad (23)$$

For $\gamma < \omega_0$, the solution is a damped oscillation

$$\phi_e^d(t) = A \exp(-\gamma t) \sin \left[ \sqrt{\omega_0^2 - \gamma^2} t + B \right], \quad (24)$$

where the constants $A$ and $B$ are to be determined from the initial conditions. The settling requirements depend on the
system. An approximate expression for the settling time is given by
\[ t_s \approx \frac{20N}{I_{CP}K_{VCO}R}. \]  
(25)

In this case, the exponential factor \( \exp(-\gamma t) \) of the solution (24) is as small as \( 4.5 \times 10^{-5} \). Assuming an initial phase error of \( \phi_\ell(0) = 180^\circ \), the dynamic phase error \( |\phi_\ell(t)| \) is smaller than 0.008° for \( t > t_s \). This value is on the same order as typical rms phase errors at the PD input for integrated PLLs.

To minimize VCO phase noise, \( K_{VCO} \) should be large enough to cover the required tuning range under all conditions with sufficient margin, but not larger. By contrast, the charge pump current should be as large as possible. This will minimize the static phase error and the PLL settling time, as evident from (16) and (25). The only limitations are the available power budget for the CP and, possibly, signal integrity.

Summarizing this section, for a linear input frequency ramp the PLL phase error at the PD input converges to a steady-state value describing the phase lag of the PLL. This value is proportional to the ramp slope and can be minimized by using a large CP current. The remaining part of the phase error obeys the same differential equation as for the case of constant reference frequency.

III. PHASE NOISE CONSIDERATIONS

Obviously, a large static phase error at the PD input implies a high CP activity. This increases the CP duty cycle \( \alpha_{CP} = T_{ON}/T_{REF} \), where \( T_{ON} \) is the CP activation time and \( T_{REF} \) is the reference period. In the steady state, the CP duty cycle is related to the static phase error via
\[ \alpha_{CP} = \frac{\phi_\ell^0}{2\pi}. \]  
(26)

In a charge-pump PLL, the in-band phase noise is usually limited by thermal noise and 1/f noise of the CP transistors [8]. The white noise power spectral density (PSD) of the charge pump output current due to thermal noise and shot noise is proportional to \( \alpha_{CP} \), whereas 1/f noise is proportional to \( \alpha_{CP}^2 \) [9]. Adding the two noise contributions, we obtain for the PSD of the CP output current [10]
\[ S_{CP} = S_{CP}^{white} \alpha_{CP} \left( 1 + \frac{\alpha_{CP} f_c}{f} \right), \]  
(27)

where \( f_c \) is the 1/f noise corner frequency of the transistor. The parameter \( S_{CP}^{white} \) corresponds to the CP current noise PSD due to white noise sources at 100% CP duty cycle. Transforming the noise current PSD to the PD input using (5), we obtain for input-referred phase PSD
\[ S_{\phi, in} = S_{CP} \left| \frac{1}{K_{PD}} \right|^2. \]  
(28)

Substituting (27) and (5) into (28) yields
\[ S_{\phi, in} = S_{CP}^{white} \alpha_{CP} \left( 1 + \frac{\alpha_{CP} f_c}{f} \right) \left| \frac{2\pi}{I_{CP}} \right|^2. \]  
(29)

For a given CP topology with programmable CP current \( I_{CP} \), \( S_{CP}^{white} \) is proportional to \( I_{CP} \). From this we conclude that doubling the CP current ideally reduces the corresponding PLL phase noise contribution by 3 dB.

The measurement of a PLL phase-noise spectrum for a ramped input frequency is very difficult, since the PLL is not in steady state. The main goal of our paper is to define a steady-state situation, where the PLL spectrum is similar. This will allow the phase-noise spectrum under frequency modulation to be deduced from measurements or simulations with constant input frequency. In [11] an offset current to ground was used to generate a static offset at the PD input. The motivation for this was to improve the linearity of the PD in the fractional-N PLL used there. If the offset current is a sufficiently large down current, then only the UP current will respond to phase error changes in the steady state. This improves the linearity of the phase detector and reduces phase noise significantly. In this case, the output current \( I \) of the CP is a continuous function of the phase error \( \phi \) at the PFD input, ideally a linear function. This idea was used in the integer-N 10 GHz PLL presented in [8], where the measured phase noise was monitored as a function of the offset current. With a CP current \( I_{CP} \) of 8 mA the offset current \( I_{OS} \) was varied between 0 and 2 mA, corresponding to a CP duty cycle \( \alpha_{CP} = I_{OS}/I_{CP} \) between 0 and 25%. According to (26), this corresponds to a static phase error between 0 and 90°. The measured in-band phase noise was increased by typically 4 dB in this duty cycle range, from -105 dBc/Hz to -101 dBc/Hz at 100 kHz frequency offset. With a larger static phase error, the in-band noise will further increase. This is especially troublesome for CMOS implementations, since the relatively high 1/f noise increases in proportion to the squared phase error according to (27). The allowable phase noise depends on the application and must be carefully determined from system simulations, which are beyond the scope of our paper. Such simulations have been performed in [6], where the impact of phase noise parameters on target signal detection in FMCW-radar systems for automotive applications was investigated. The spatial resolution was shown to depend strongly on the VCO phase noise, especially for multi-target scenarios. This suggests that the VCO phase noise be reduced by PLL high-pass filtering using a large loop bandwidth and a large CP current [8].

Let us assume, as an example, that a CP duty cycle of 1% is allowed from the phase noise point of view. For a fractional PLL this phase offset is usually sufficient to linearize the PD, reducing in-band phase noise and spurs due to folding of quantization noise [11]-[14]. Since \( \alpha_{CP}=10\% \) corresponds to \( \phi_\ell^0 = 2\pi/10 \) according to (26), we obtain from (16) an upper bound for the angular acceleration
\[ \alpha_{REF} < \frac{2\pi I_{CP}K_{VCO}}{10CN}. \]  
(30)

According to (18), this corresponds to the recommendation
\[ T_s > \frac{10C b_s}{I_{CP}K_{VCO}}. \]  
(31)

For a numerical illustration, we consider the following parameter set: \( b_s = 1 \text{ GHz}, C = 1 \text{ nF}, K_{VCO} = 1 \text{ GHz/V}, I_{CP} = 2 \text{ mA} \). From (31) we obtain the recommendation \( T_s > 5 \mu \text{s} \) for these PLL parameters. This means that the sweep duration...
PLLs is suggested: power consumption at a reasonable level. Resulting from these, 10%, the DC current of the CP is below 1 mA, keeping CP current as high as 8 mA. Note that for a CP duty cycle of [10]. In [8] a very low phase noise was achieved by using a phase noise, a large CP current minimized by increasing the CP current and by reducing the loop capacitance $C$. While a small $C$ may increase the PLL phase noise, a large CP current $I_{CP}$ reduces the phase noise [10]. In [8] a very low phase noise was achieved by using a CP current as high as 8 mA. Note that for a CP duty cycle of 10%, the DC current of the CP is below 1 mA, keeping CP power consumption at a reasonable level. Resulting from these observations, the following design procedure for integrated PLLs is suggested:

- use a relatively large filter capacitance $C$ limited by the available chip area only;
- use a large CP current;
- use a proper loop resistance $R$ such that the settling time according to (25) is short enough.

Note that the use of a large CP current may conflict with the linear model used here, which requires small changes of the VCO control voltage in the steady state. In reality, this can be achieved by using small $R$, large $C$ and a small bypass capacitor $C_2$ from the CP output to ground. The latter was not included in our second-order PLL model to facilitate the analysis of the phase error. In a well-designed PLL $C_2$ would reduce the reference spurs, but it would hardly change the in-band phase noise discussed in this paper.

V. MODELING RESULTS

In this section, we investigate the steady-state phase-noise spectrum as a function of the ramp slope. The analysis is based on the linear phase noise model described in [19]. This model includes the noise of the CP, the VCO, the reference input, reference buffer, and the loop filter. It is based on an analytical description of the noise sources and transfer functions, where the model parameters are to be determined from measurements or simulations. The model has been verified for the 24 GHz PLL in [19] by comparing measured and simulated phase noise spectra. In this paper, we are targeting higher frequencies of 80 GHz and above, where experimental results are not yet available. However, since CP, PFD and reference input buffer will not be changed, the corresponding noise parameters are the same and will be used for noise prediction. The incorporation of quantization noise generated in the sigma-delta modulator (SDM) of a fractional-N PLL has been described in [10]. This also includes noise folding in the nonlinear PD. Here we assume that a DDFS drives an integer-N PLL, where quantization noise within the PLL is not an issue.

As an example, we investigate a 78 GHz integer-N PLL driven by a 100 MHz reference using a CP current of 2 mA. The filter parameters are $C=1$ nF and $R=10$ kΩ. The charge pump noise parameters $S_{CP}^{white}$ and $f_c$ were extracted from measurements on a previous design [19], where a low CP current was used to maximize CP induced phase noise. The reference buffer noise parameters were deduced from phase noise measurements with very small input amplitudes to maximize buffer-induced phase noise. The VCO phase noise parameters were extracted from a recently published 61 GHz VCO [20] manufactured in a 130 nm SiGe BiCMOS technology. Fig. 2 shows the measured phase-noise spectrum of this VCO. The phase noise measurement was performed after 1:16 division at 3.8 GHz output frequency. In our model,
an estimate for the VCO phase noise is obtained by adding
20 \log_{10}(78\text{GHz}/3.8\text{GHz})=26.2 \text{ dB to the measured values.}

As discussed at the end of Section III, a sweep duration of
T_s = 5 \mu s corresponds to a static phase error at the PD
input of \phi_0 = 36^\circ. Similarly, the sweep durations T_s = 50 \mu s
and T_s = 1 \mu s correspond to \phi_0 = 3.6^\circ and \phi_0 = 180^\circ,
respectively. By using (26) we obtain an equivalent CP duty
cycle \alpha_{CP} = \phi_0/360^\circ, where the phase error is given in
degrees. The parameter \alpha_{CP} serves as an input to the phase
noise model in [19]. In this way, we can approximately
deduce the phase-noise spectrum under FM from the well-
known steady-state case. Fig. 3 shows the modeled phase noise
spectra for the three different static phase errors. Here we

![Graph showing modeled phase noise spectra for different static phase errors]

Fig. 3. Modeled phase noise spectra of a 78 GHz PLL for different static
phase errors at the PD input.

used the following parameters: \gamma = 10 \text{ kO}, C = 1 \text{nF}, I_{CP} = 2 \text{ mA},
K_{VCO} = 1 \text{GHz/V}, and N = 780. Using (21), we obtain the loop
bandwidth f_L in units of Hz given by

\[ f_L = \frac{2\gamma}{2\pi} = \frac{I_{CP}K_{VCO}R}{2\pi N} \approx 4 \text{ MHz}, \]

consistent with Fig. 3. If the settling time of t_s = 780 ns must
be further reduced, the CP current I_{CP} should be increased
rather than \phi_0 = 0. This will keep static phase error
and phase noise low, as discussed in Sections II and III. The
ideal case \phi_0 = 0 is also depicted in Fig. 3 for comparison.
According to (27), this corresponds to a noise-less CP in
our model. For \phi_0 = 3.6^\circ, the phase noise spectrum is a
few dB higher in the kHz range, showing that the CP noise
contribution is similar to the other phase noise contributions.
By contrast, for \phi_0 = 36^\circ the phase noise spectrum is more
than 10 dB higher than for the ideal case. This demonstrates
that the FM-induced CP noise dominates the phase-noise
spectrum in this case. The effect of FM is most pronounced
at low frequencies, where 1/f noise dominates the spectrum.
This is due to the quadratic dependence of the 1/f current noise
PSD on the CP duty cycle according to (27).

VI. CONCLUSIONS

We have calculated the static and dynamic phase error at
the phase detector input for a PLL driven by a linear
frequency ramp. The effect of the static phase error on phase
noise spectrum and linearity was discussed. We have presented
design guidelines for integrated PLLs to be used in FMCW
radar. Finally, we have calculated the steady-state phase noise
spectra for different ramp slopes corresponding to different
static phase errors. In summary, we believe the major impact
of our work will be to reduce the number of design cycles
when developing FMCW radar systems.

REFERENCES

[1] T. Mitomo, N. Ono, H. Hoshino, Y. Yoshihara, O. Watanabe, and I. Seto,
"A 77 GHz 90 nm CMOS transceiver for FMCW radar applications,”
77-GHz FMCW radar transmitter in 65-nm CMOS technology,”
FMCW radar circuit using a SiGe bipolar transceiver chip stabilized by
a fractional-N PLL synthesizer,” IEEE Transactions on Microwave Theory
pump phase-locked loops,” IEEE Transactions on Circuits and Systems I:
[5] I. S. Syllaioz and P. T. Balsara, “Multi-clock domain analysis and mod-
celling of all-digital frequency synthesizers,” in Proceedings of the 2011
IEEE International Symposium on Circuits and Systems (ISCAS 2011),
Rio de Janeiro, Brazil May 2011, pp. 153-156.
impact of phase noise parameters on target signal detection in FMCW-
radar system simulations for automotive applications,” 2011 IEEE CIE
International Conference on Radar (Radar), Chengdu, China, Oct. 2011,
p. 494-497.
10 GHz low-noise phase-locked loop with improved PVT tolerance,”
Analog Integrated Circuits and Signal Processing, vol. 67(3), pp. 319-
modeling and charge-pump operation for fractional-N PLLs,”
IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57,
Rofougaran, and W. J. Kaiser, “A 4GHz fractional-N synthesizer for IEEE
802.11a,” 2004 Symposium on VLSI Circuits Digest of Technical Papers,
Honolulu, USA, June 2004, pp. 46-49.
frequency synthesizers for high-spectral purity,” IEEE Transactions on
Circuits and Systems II: Analog Digit. Signal Processing, vol. 50,
for in-band phase noise reduction in Delta-Sigma synthesizers,”
IEEE Transactions on Circuits and Systems II: Analog Digit. Signal Processing,
attenuation improvement of all-digital frequency synthesizers,” in
Proceedings of 2004 Custom Integrated Circuits Conference (CICC’04),
izer for 802.11a wireless LAN,” IEEE Journal of Solid-State Circuits,
[16] M. Pichler, A. Stelzer, P. Gulden, C. Seisengerber, and M. Vossiek,
“Phase error measurements and compensation in PLL frequency synthe-
sizers for FMCW sensors: context and application,” IEEE Transactions on