A Stochastic Pattern Generation and Optimization Framework for Variation-Tolerant, Power-Safe Scan Test

V.R. Devanathan, C.P. Ravikumar,
Texas Instruments, India
Presented at ITC 2007
Full paper available from IEEE Xplore

V. Kamakoti
Indian Institute of Technology Madras, India

Motivation

• Process Variation
  – Impact on Delay/Timing is well-known
  – Also impacts power (esp. instantaneous peak)
    • 3% clock skew variation => 79% increase in instantaneous peak toggles!!
Purpose

• Debugging and fixing power-related test failures effort-intensive
  – Need correct-by-construct variation-tolerant power-safe pattern generation

• Aim of this work
  – Target 1: Constrained global peak test power
    • Limits may come from package or tester
  – Target 2: Constrained dynamic IR-drop
    • Must reduce localized peak power dissipation
    • Limits may come from power grid
  – Target 3: Reduced pattern count overhead
    • Need to optimize power-safe pattern generation

Outline

• Introduction
• Observations
• Statistical Variation Modeling
• Variation-Tolerant Power Profiling
• Power-safe Pattern Generation & Optimization
• Experiments and Results
• Conclusion
Introduction

• Scan Test Constraints
  – Test power >> Functional mode power
  – Excessive IR-drop => yield-loss

• Low Cost Tester / Package Constraints

• Power supply grid designed for functional worst-case
  – Over-designing for test => Area overhead

ATPG must be Timing-aware

• Need for Timing Awareness
  – Glitches/Hazards need to be considered for correct power estimation
  – Peak power pattern ≠ Instantaneous peak power Pattern
AFTERG must be Layout-aware

• Need for layout-awareness
  – Functional power dissipation is not uniformly distributed across the chip
    • Even within a core, static IR-drop induces a regional power constraint

Proposed Power-Safe Pattern Generation

• Characteristics of Proposed Power-Safe Pattern Generation
  – Timing aware
    • Consider glitches / hazards
  – Layout aware
    • Different regions have different power constraints
    • Static IR-drop plot may be used to derive regional power constraint
  – Variation-tolerant
    • Statistical variation Modeling
Layout Awareness

- Design partitioned into regions based on physical layout
  - Size of region determined by power grid architecture
  - Regional toggle constraints derived from static IR-drop plot
  - Each region $R$ has an Activity Vector $A_R$
    - $A_{R,i}$ = Number of toggles in the region $R$ at the time instant $i$

Max. allowable switching activity varies with region

Layout Aware Toggle Constraints

- **Global Toggle Constraint (GTC)**
  \[
  GTC \geq \sum_{R} \sum_{j} A_{R,j}; \forall j, R
  \]

- **Global Instantaneous Toggle Constraint (GITC)**
  \[
  GITC \geq \text{Max}_{j} \sum_{R} A_{R,j}; \forall j, R
  \]

- **Regional Instantaneous Toggle Constraint (RITC) / Maximum Regional Toggles (mR)**
  \[
  m_R \geq A_{R,j}; \forall j, R
  \]
Statistical Timing Simulation

- Statistical Timing Simulation
  - Discrete probability distribution
  - Let \(<i, \Delta>\) denote \(<\text{inertial delay, transport delay}>\)
  - E.g. rise transition propagation

\[
P_{\text{rc}}(t = \tau + \Delta) = \left[ P'_{\text{a}}(t = \tau) \ast \min (\alpha', \beta') \right] + P_d
\]

where
\[
\alpha' = P'_{\text{b}}(t = \tau) + P_{\text{1b}}(t = \tau)
\]
Transition Propagation Probability

\[
\beta' = P'_{\text{b}}(t = \tau + i) + P_{\text{1b}}(t = \tau + i)
\]
Hazard Cancellation Probability

Need for Statistical Variation Model

- Statistical vs. Uncertainty Interval Schemes
  - Uncertainty Interval Scheme is Pessimistic
Power-Safe ATPG

• Overview
  – PODEM-based ATPG
  – Heuristics to minimize hazards
  – Regional and Global Toggle Constraints to limit switching activity

• Pattern Optimization
  – Maximal re-use of patterns from commercial ATPG tools
  – Regenerate only power-unsafe patterns

Hazard Minimization

• Estimating Glitch Probability
  – Timing Window Size =
    (latest_signal_arrival – earliest_signal_arrival)
  – Timing Window Size = 0 => Balanced Path => Glitch-free

• Minimize glitches => Use least timing window size
**Pattern Optimization Flow**

1. **Initial Pattern Set** → **Statistical Power Profiler**
2. **Violating Patterns** → **Power-safe Patterns**
3. **Fault Simulation** → **Violating Faults** → **Power-safe ATPG** → **Final Power-safe Pattern Set**

**Experimental Results**

- Proposed Pattern Generation and Optimization Flow implemented in Perl
  - Input distribution: standard normal distribution
  - Toggle constraint set to 90% of the original peak value
Experimental Results

• Average pattern count increase compared to Random-fill ~ 8%

![Pattern Count Graph]

Experimental Results

• Run Time
  – Power Profiling dominates ATPG time

![CPU Time Graph]
Experimental Results

• Effect of Process Variation
  – Power-Safe ATPG is more tolerant to specified variation

![Graph showing the comparison of Power-Safe ATPG, Random Fill, Adjacent Fill, 0-fill, and 1-fill among different Standard Deviation of Delay Variation (σ).](image)

Conclusion

• Summary
  – Statistical Power-safe ATPG is proposed
    • Tolerant to process variation
    • Can handle arbitrary delay distribution

• Future Work
  – Run time reduction
Thank You