High performance germanium photodetectors integrated on submicron silicon waveguides by low temperature wafer bonding

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Abstract: We demonstrate germanium photodetectors integrated on submicron silicon waveguides fabricated with a low temperature ($\leq 400^{o}$C) wafer bonding and ion-cut process. The devices shows a low dark current of ~100 nA, a fiber accessed responsivity of > 0.4 A/W and an estimated quantum efficiency of above 90%.

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OCIS codes: (040.5160) Photodetectors; (250.5300) Photonic integrated circuits; (200.4650) Optical interconnects

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Silicon based photonics [1-8], widely pursued for the vision of integrating microphotonics with microelectronics on the same chip, rely on high performance photodetectors for its realization. Germanium (Ge), due to its large absorption coefficient at near-infrared frequencies, and its lower cost and compatibility of parallel processing with silicon compared to III-V semiconductors, is perceived as the best candidate for on-chip photodetectors [9-13]. High performance Ge photodetectors integrated on silicon waveguides have been reported very recently [14,15]. However, they require specified high temperature ($\geq 700^{o}$C) epitaxial growth of Ge, which limits the process compatibility with microelectronics. Polycrystalline Ge photodetectors fabricated from low temperature ($\leq 300^{o}$C) evaporation have also been reported, however, their efficiency is relatively low (~ 15%) due to the poor crystal quality [16]. Here we report low dark current (~100 nA) and high efficiency (>90%) single crystalline Ge photodetectors integrated on submicron silicon waveguides fabricated using a low temperature wafer bonding process, which enable on-chip photonic interconnections.

In order to achieve high sensitivity and high speed photodetectors we use a waveguide integrated metal-semiconductor-metal (MSM) configuration. Figure 1(a) and (b) show the schematic design of our photodetectors. Here a single crystalline Ge film is bonded on a submicron silicon waveguide with a thin SiO_2 layer for electrical isolation. Metal electrodes are placed on top of the Ge pad to confine the light horizontally and collect the photo-generated carriers. The small size of the silicon waveguide allows small electrode spacing and thus ensures high speed operations [12,14]. Another advantage of this scheme is that, since the carrier transport takes place only in the Ge layer and thus imposes no electrical requirement on the waveguide layer, one can fabricate the photonic circuits using materials which can be deposited on top of a CMOS chip such as amorphous or polycrystalline silicon [17-19]. This is in contrast to detectors that require the use of single crystalline silicon for either Ge epitaxy growth or carrier transport [14,15]. Figure 1(c) shows the TE mode profiles of the silicon waveguide alone and the first and second order modes excited in the photodetector region. These modes are calculated using finite difference mode solver with dimension as follows: the silicon waveguide is 500 nm by 230 nm, the Ge slab thickness is 250 nm, the SiO_2 isolation layer is 40 nm thick, and the Au electrodes are 100 nm thick with spacing of 750 nm. The refractive indices of Si, Ge and SiO_2 are 3.48, 4.36 and 1.46 respectively. The multimode excitation does not affect the detector efficiency since the light in each mode will eventually be absorbed by the 30 μm long Ge, though with different absorption length (~5 μm and ~10 μm respectively). For integrated photodetectors, the spurious optical back-reflection at the detector interfaces is a concern. For the parameters we assumed above, the back-reflection level is calculated from FDTD simulations to be about -20 dB, thanks to the strong optical confinement of the input silicon waveguide. Further reduction in reflection might be required for photonic circuits to avoid crosstalk and can be achieved by means such as slightly increasing the waveguide dimensions or the thickness of the isolation oxide. In this work, we use a quadratic

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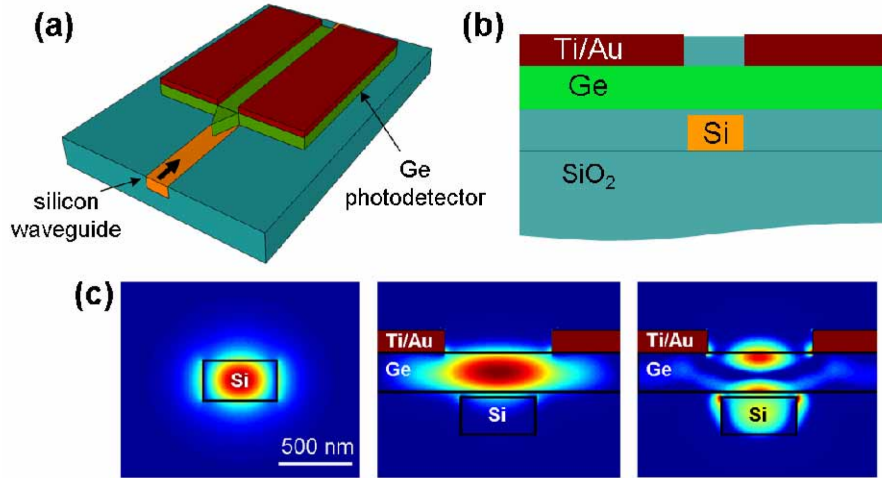

Fig. 1. Schematics of (a) the integrated Ge photodetector on a silicon waveguide, and (b) the device cross section. (c) TE mode profiles of the input silicon waveguide and the two modes excited in the photodetector region.

germanium taper to reduce the reflection (see Fig. 1(a)). With a ~4 µm long taper starting from 50 nm wide, the simulated reflection level is reduced to below -25 dB.

The thin Ge film used here is a high quality single crystalline film transferred from a Ge bulk wafer by a low temperature wafer bonding and ion-cut process. Figure 2 shows our entire fabrication flow, where the processing temperature is maintained $\leq 400^oC$, below the 450^oC limit for CMOS backend processes [19]. This would allow the integration of photonic circuits on top of a CMOS chip following the metallization steps of the microelectronic chip. First a 4-inch unintentially n-doped Ge wafer from Umicore (resistivity $> 40\ \Omega\cdot cm$) was capped with 100 nm SiO_2 by plasma enhanced chemical vapor deposition (PECVD) at 400^oC, and ion implanted with hydrogen ions ($4x10^{16}$ cm^{-2} at 80 KeV). The SiO_2 capping layer protects the Ge surface during the ion implantation and was subsequently removed with diluted hydrofluoric acid. Silicon waveguides were first defined on a 4-inch silicon-on-insulator (SOI) wafer from SOITEC with electron-beam (E-beam) lithography and inductively coupled reactive ion etching (ICP-RIE). Figure 3(a) shows a top view scanning electron microscope (SEM) image of the waveguide, which has a cross section dimension of 500 nm x 230 nm. A PECVD SiO_2 cladding layer was then deposited and planarized with chemical mechanical polishing (CMP) down to a thickness of approximately 40 nm. A thickness variation from ~40 nm to ~70 nm is observed across the 4-inch wafer with an edge exclusion of 15 mm. This oxide layer acts as the bonding interface and the electrical isolation layer between the Ge layer and the underneath silicon. After these processes, we cleaned the implanted Ge wafer and the patterned SOI wafer with NH_4OH based solutions to obtain hydrophilic surfaces. The wafers were bonded together at room temperature with applied downward force of 2000 N (equivalent pressure: $2.5x10^5$ Pa). The bonded wafers were then annealed at 100^oC in an Ar environment under atmospheric pressure to enhance the bonding strength. The temperature was then gradually increased up to 400^oC. At such elevated temperatures, the implanted hydrogen ions form microcavities at the implantation depth, which induces sufficient in-plane stress to split the thin Ge film above the implantation depth off from the bulk wafer. Similar technologies have been used to transfer various semiconductor thin films including Si, Ge, GaAs and InP to silicon [20 and references therein]. The exfoliated thin film, which is approximately 670 nm thick, remains bonded to the patterned SOI wafer. A second CMP process was then performed to reduce the Ge thickness to

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approximately 250 nm. Across the wafer a thickness variation of less than 20 nm is observed resulting from the CMP process. The observed variations in both SiO_2 and Ge thickness should not noticeably affect the detector efficiency based on simulations. Figure 3(b) shows an SEM cross sectional image of the transferred layer. We then define the Ge photodetector pads on top of the silicon waveguides with E-beam lithography and ICP-RIE. Figure 3(c) shows a top view SEM image of one of the devices after this step. Germanium tapers with a tip width of 50 nm and a length of approximately 4 μm are used on each side of the Ge photodetector pad. The relatively low image contrast between the silicon and SiO_2 trenches is caused by the 40 nm SiO_2 cladding layer on top of silicon. Another PECVD SiO_2 cladding layer of 700 nm was deposited to cover the silicon waveguides to ensure efficient coupling with optical fibers. Vias for contact electrodes were then defined and etched, and 15 nm Ti and 200 nm Au were deposited to form the MSM structures. Figure 3(d) shows an optical image of a device after this step, with an electrode spacing of 750 nm. The electrodes were then connected to Au contact pads located next to the photodetectors. Here the metal forming the metal-Ge schottky barrier is Ti. Au is used for the ease of electrical probing, and can be replaced by other metals such as aluminum which is compatible with the CMOS processing. The devices were then diced and polished for optical and electrical testing. The entire fabrication process can be done with temperature $\leq 400^{o}$ C and is compatible with the backend processing of CMOS microelectronics.

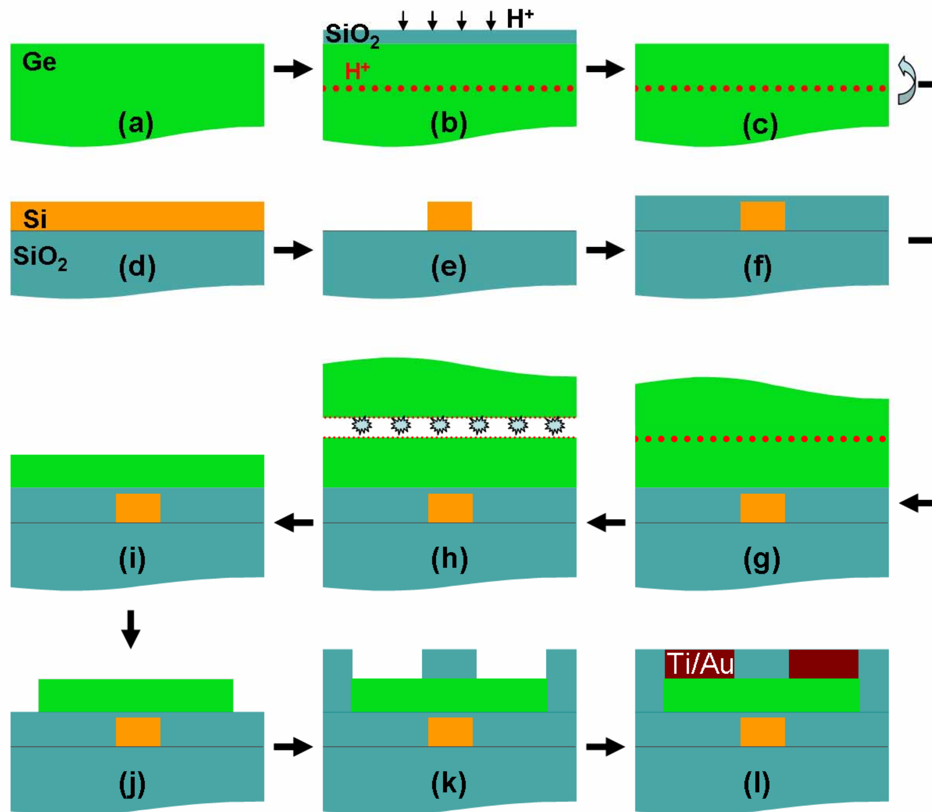

Fig. 2. Fabrication process flow for our Ge photodetectors. (a-c) Prior processing on the Ge wafer, including SiO_2 deposition, hydrogen implantation, and SiO_2 removal with HF. The red dotted line indicates implantation depth. (d-f) Prior processing on the SOI wafer, including patterning of Si waveguides, SiO_2 deposition, and then SiO_2 CMP planarization. (g-i) are wafer bonding, layer splitting, and then Ge CMP. (j-l) include patterning of Ge, SiO_2 deposition, via etch and metal deposition.

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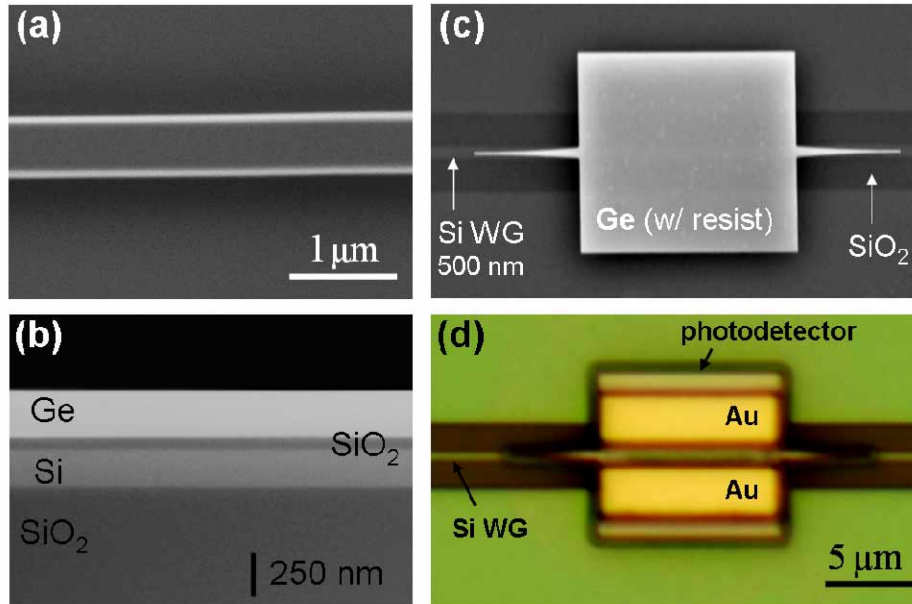

Fig. 3. (a) SEM top view image of the silicon waveguide without cladding. (b) SEM cross sectional image of the ion-cut Ge layer. (c) SEM top view image of the Ge pad with tapers on top of the silicon waveguide. The relatively low contrast between the silicon and SiO_2 trenches is caused by the 40 nm SiO_2 cladding layer on top of silicon. The Ge pad still has E-beam resist left. (d) Optical image of the fabricated Ge photodetector before contact pads.

We measure a low dark current of ~100 nA, a high fiber-accessed responsivity of >0.4 A/W, and an estimated quantum efficiency of above 90% in our fabricated Ge photodetectors. We use a Keithley 2400 sourcemeter to apply a bias voltage across the device and record the dark current. The photocurrent is measured by launching TE polarized light from an optical fiber into the silicon waveguides with nanotapers at the input end of silicon waveguides for efficient coupling [21]. Figure 4(a) shows a typical response for a photodetector length of 30 µm. The dark current is measured to be approximately 100 nA for a bias voltage up to 4 volts. The dark current density (4 nA/μm^2) is considerably lower than the previous reported Ge photodetectors using a similar MSM configuration but epitaxially grown Ge [14]. This is attributed to the higher crystal quality of the ion-cut Ge layer compared to the epitaxial growth where the large lattice mismatch (4.2%) between silicon and Ge induces a large amount of dislocation defects. The observed dark current is higher than that of PIN-based Ge photodetectors [10,11,15]. However, since one important source of dark current in MSM detectors is thermionic emission at the metal-semiconductor interfaces, further reduction can be achieved by employing asymmetric schottky barriers forming the MSM photodetector [22]. Decreasing the contact area (now ~4 µm electrode width) can also reduce the dark current. Figure 4(a) also plots the photocurrent under illumination with a 0.95 mW input (measured at the end of the fiber) for a wavelength near 1550 nm. A large signal to noise ratio (photocurrent to dark current) of ~3000 is observed with this illumination level. The photocurrent saturates with a bias voltage above 2.5 V, which is higher than what is typically required (~1 V) for such electrode spacing [14]. This is due to the structural design we used here rather than material properties. From optical and electrostatic simulation we found that the carriers are generated not only in the gap between the two electrodes, where the collecting electrical field is high, but also in the taper region and slightly underneath the electrodes (due to diffraction), where the collecting electrical field is much weaker. This problem can be resolved by avoiding the low field regions using a slightly modified geometry of the waveguide and detector. Figure 4(b) plots the spectrum of the

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measured fiber-accessed responsivity. A value as high as 0.44 A/W is observed near 1527 nm. If corrected for the coupling loss from the fiber to the silicon waveguide (estimated to be ~3 dB [21]) and the propagation loss of the 0.3 cm long silicon waveguide before the photodetector (estimated to be 4-5 dB/cm [6]), the quantum efficiency is estimated to be above 90%. The roll-off in responsivity after 1540 nm (corresponding to the band edge of Ge) is due to the decreased absorption of Ge and unwanted absorption due to the metal electrodes.

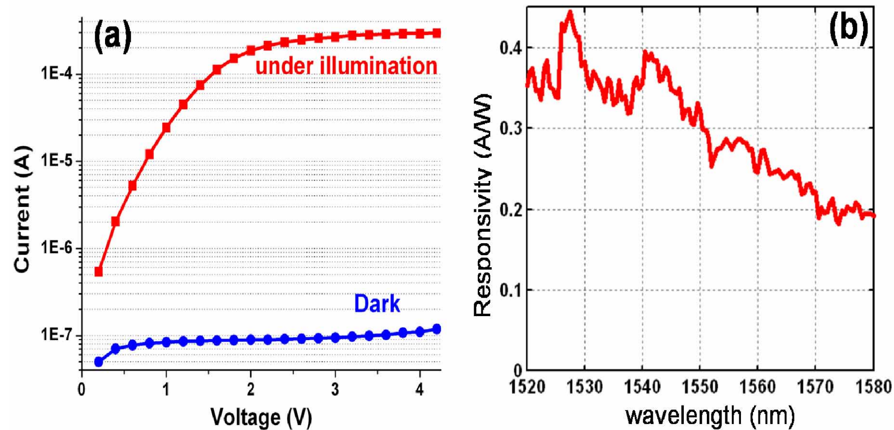

Fig. 4. (a) Measured dark current and photocurrent. (b) Spectrum of the measured fiber-accessed responsivity.

The small-spacing MSM photodetectors should allow very high speed operation. The capacitance of our photodetector is calculated to be approximately 2 fF, and the RC delay is on the order of 100 fs for a 50 Ω impedance [12], therefore not a limiting factor in the speed of the device. The speed is limited mainly by the carrier transit time, which is inversely proportional to the spacing between the electrodes [12,14]. For an spacing of 500 nm and a saturated carrier velocity of 6×10^6 cm/s for both electrons and holes in Ge [23], the carrier transit time is close to 10 ps, corresponding to a 3dB cut-off frequency of ~45 GHz [10,14]. This is consistent with the measured transit time and cut-off frequency for 1 μm electrode spacing of 19 ps and 25 GHz respectively in Ref. 14. We expect that speed above 40 GHz can be achieved in this device with the elimination of the low field regions as discussed above.

In conclusion, we demonstrate Ge photodetectors integrated on submicron silicon waveguides with a low dark current of approximately 100 nA, a fiber-accessed responsivity of >0.4 A/W, and an estimated quantum efficiency above 90%. Theoretical speed above 40 GHz should be reached with revised structural design. These photodetectors with high performances and full compatibility with the CMOS backend processes enable the vision of integrating microphotonics and microelectronics on the same chip.

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