Synthesis of Finite State Machines with Magnetic Domain Wall Logic

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Abstract—As the feasibility of basic logic operators based on magnetic domain wall (MDW) logic has been demonstrated we present here the synthesis of more complex functions using this technology. After the presentation of the specific design constraints associated to MDW logic, we describe the architecture of Finite State Machines and show simulation results for a 3-bit counter.

I. INTRODUCTION

Recently, new nanometric magnetic components based on the propagation of domain wall were discovered [1,2]. The demonstration of the feasibility of the basic logic functions, especially AND and NOT gates, paves the way for an alternative technology for digital circuits featuring intrinsic non volatile storage. Furthermore, the simplicity of this technology, compatible with plastic flexible substrate, could lead to very low production cost and very low power dissipation. As basic gates were demonstrated, the design of complex digital circuits seemed straightforward. Actually, magnetic domain wall logic features particular constraints and requires specific design methodology [3,4]. Finite State Machine (FSM) constitutes one of the most popular design templates for digital circuit. As, the synthesis of FSM gives access to a wide set of sequential logical functions it constitutes an important challenge for the domain wall logic. In this paper, we present the design and simulation of a FSM using magnetic domain wall (MDW) logic. In the first part, we introduce the basic components. In the second part, we focus on the specific behavior of MDW circuits. Finally, we present the architecture of FSM using MDW logic.

II. BASIC COMPONENTS

MDW components are made of a ferromagnetic track with small width, in the range of 100 nm. Such ferromagnetic nanowires feature an anisotropic behavior and, in its stable states, the magnetization can only be oriented along the long axis of the nanowire. The nanowire is then intrinsically binary. In addition, a magnetic domain wall (MDW) exists between domains with opposite magnetization and it can propagate through the nanowire when pushed by a external magnetic field [1,5,6]. More precisely, the domain wall propagation can occur if the magnitude of the external magnetic field is higher than a "standard" threshold. In addition, propagation can occur in bends when the external magnetic field is rotating. Furthermore, crossover of two perpendicular track can be used without interference because the propagation occur at different times. Finally, when the external rotating magnetic field (ERMF) is non-symmetrical but superimposed with a static magnetic field (DC offset), a 'y' shape component can operate either as a logic gate [2], a fan-out element or a memory depending on its orientation relatively to the static magnetic field.

The direction of rotation of the ERMF drives the propagation direction of the MDW. Indeed, in bends, the MDW can propagate only when the ERMF follows the curvature of the track. Obviously, the propagation through a 90°-bend imply a T/4 delay where T is the period of the ERMF. The propagation direction is also used to define the logical state associated to the magnetization direction. Arbitrarily, we choose to associate the HIGH (resp. LOW) logic state to magnetization oriented in the direction of the MDW propagation (resp. in the direction opposite to the MDW propagation). Notice that, thanks to the ERMF, the propagation of the HIGH logic state and the propagation of the LOW logic level never occur simultaneously.

When two bends components are joined to build a cusp-shape component [7], a MDW can enter the inner section with one magnetization state (figure 1-A and 1-B) and, T/2 later, continues its propagation with the magnetization in the...
opposite direction (figure 1-C). Consequently, this component operates like an inverter associated to a T/2 delay.

A 'y' shape component oriented with the fork section as output, relatively to the direction of propagation of MDW, operates like a fan-out element. A MDW entering in the input section forks and continues its propagation through the two outputs.

For a 'y' shape component oriented with the fork section as an input, two cases must be distinguished.

If the magnitude of the ERMF is greater than a "high" threshold, the propagation of a single MDW occurs even if the other input state is different. In this case, the output and the other input switch to follow this new magnetization direction. Note that the switching of the other input must be stopped with an appropriate bend, eventually belonging to a not gate, otherwise it may propagate erroneously through other devices.

If the magnitude of the ERMF is greater than the "standard" threshold but remains lower than the "high" threshold, the propagation occurs only if the two input states are equal.

So, three different behaviors (figure 2) can be obtained with this gate:

1. If the magnitude of the ERMF is lower than the high threshold, then the component can be used as a memory. When the two inputs are different, the component is in its storage state. On the contrary, when the two input level are HIGH (resp. LOW) the output is set (resp. reset). We call this component a magnetic /RS flip-flop.

2. If, thanks to a DC offset, the magnitude of the EMRF is greater than the HIGH threshold for the HIGH level but lower than this HIGH threshold for LOW level, then the HIGH level is the absorbing element of this gate while the LOW level is the neutral element. Consequently, this is an OR gate.

3. Conversely, if, thanks to a DC offset, the magnitude of the EMRF is greater than the HIGH threshold for the LOW level but lower than this HIGH threshold for HIGH level, then the LOW level is the absorbing element of this gate while the HIGH level is the neutral element. Consequently, this is an AND gate.

III. SPECIFIC CONSTRAINTS

We previously shown in [4] that a straightforward CMOS-like design strategy cannot be used for building complex digital circuits with MDW components. This results from two constraints specific to MDW logic.

First, the MDW inverter includes a T/2 delay. Thus, it can not be considered exactly as a combinatorial function. In addition, as long as the ERMF is global to the entire chip, AND gates and OR gates must be oriented in the opposite directions. Consequently, bends must be used to mix AND and OR gates. As the propagation through 180°-bends implies T/2 delay, the design of complex functions never leads to an actual combinatorial behavior. From the designer point of view, this implies a lack of synchronization of the various inputs. So, a resynchronization is required. This can be obtained with a sampling component (figure 3) build from /RS flip flop [4].
Propagation through MDW component is driven by the rotation direction of the ERMF and the curvature in bend components. As we previously noted, the propagation of a MDW through a 'γ'-shape component with a magnitude of the ERMF higher than the "high-threshold" not only switches the output but also the other input. This "back-propagation" of the digital signal must be managed and the insertion of a bend after all the fan-out elements constitutes an efficient conservative workaround.

IV. FSM ARCHITECTURE

A typical architecture of FSM is shown on figure 4. The state register and the first combinatorial function dedicated to transition calculation constitute the core of this architecture.

The state register can be built with d-latch flip-flop. As we already shown in [4], this d-latch flip-flop can be built from the previously presented /RS flip-flop. The ERMF magnitude and DC offset is then constrained by the d-latch orientation. Any combinatorial function can be expressed in a canonical form using a product of maxterms or a sum of minterms. Physical implementation of one of this canonical form necessitates to mix AND, OR and inverters. As we previously noted, this requires to reverse the propagation direction with bends between AND gates and OR gates, leading to a 'U'-shape architecture. Alternatively, thanks to the De Morgan's theorem, a straight-shape architecture can be obtained at the expense of adding inverters. The resulting FSM architecture is presented on figure 5.

V. CONCLUSION

New nanometric devices require new design methodologies. In this paper, we presented the specific behaviors that affect the MDW circuits: mainly signal back-propagation and parasitic quantified delays. Despite these constraints, we described the architecture of FSM using this technology. This is illustrated with the design and simulation of a 3-bit counter. As FSM is a very general model, this open the door for the synthesis of a wide range of logic functions.

REFERENCES

Figure 6. Schematic of a modulo-8 Magnetic counter

Figure 7. Simulation result for a modulo 8 magnetic counter