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A New Multilevel Inverter with Reduced Number of Switches

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ABSTRACT

In recent day's Multilevel inverter (MLI) technologies become a incredibly main choice in the area of high power medium voltage energy control. Though multilevel inverter has a number of advantages it has drawbacks in the vein of higher levels because of using more number of semiconductor switches. This may leads to vast size and price of the inverter is very high. So in order to overcome this problem the new multilevel inverter is proposed with reduced number of switches. The proposed method is well suited for a high power application and it built with three Dc sources and six Switches. Multi carrier pwm technique is used for sine wave generation. The results are validated through the harmonic spectrum of the FFT window by using Matlab/simulink. The result of the proposed MLI is compared with the conventional MLI and other seven level existing topologies.

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1. INTRODUCTION

In recent days MLI has drawn large interest in high power industry. They present a latest set of aspects to facilitate and utilized in reactive power compensation [3]. The unique arrangement of multilevel voltage source inverters allow them to achieve high voltages with the low harmonics not including the utilization of transformers or series connected synchronized switching devices [9].

The Diode clamped, Flying capacitor, Cascaded H-bridge inverter are the three main different multilevel inverter structures which are used in industrial applications with separate dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor voltage balancing and this problem is overcome in cascaded H-bridge inverter [4]-[7].

Conventional cascaded seven level multilevel inverter require twelve switches and three dc sources separately [8]. The main drawback in Conventional cascaded is that when levels are increasing it requires more number of semiconductor switches. As a result some alternations are to be made inorder to reduce the size and switch of the inverter. The next topology is made with three sources and nine switches and it yields the stair case waveform with the reduced total harmonic distortion compared to conventional multilevel inverter [1].

Then the next topology is further reduced for two switches then it consists of three dc sources and seven switches where the harmonics are reduced [2]. Again the seven level inverter is reduced with one switch but it also leads to increase in one of the dc sourcesso the topology is made of four dc sources and six switches [6]. But increase in one dc sourceis consideres as one of the drawback of this circuit. By analysing the advantages and drawbacks of the existing topologies. The new topology is proposed and discussed in this paper which overcomes the drawbacks of the existing topologies.

The proposed topology is designed with three dc sources and six switches and also it consists of some additional features like minimum number of switches conducting at a specific interval of time, Further the multicarrier pwm method [5].

2. EXISTING TOPOLOGIES

2.1. Seven Level Nine Switch MLI Topology

This topology is designed with five switches and three dc sources along with one H-bridge consists of four switches which is used for polarity reversal to produce three positive and three negative and one zero voltage level which is shown in Figure 1. The switching pattern of the seven level nine switch topology is shown in Table 1.

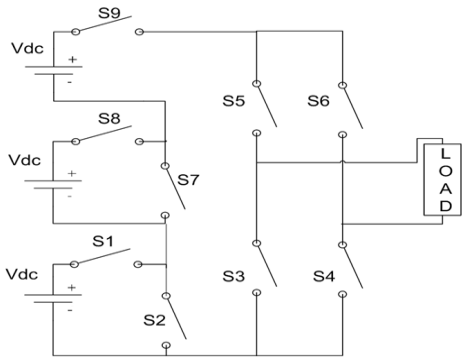

Figure 1. Configuration of seven level nine switch Topology

Table 1. Switching Pattern for seven levels nine switch topology

S.No	Switches state					Output voltage
	S1	S2	S7	S8	S9	
1	Off	On	On	Off	On	Vdc
2	Off	On	Off	On	On	2Vdc
3	On	Off	Off	On	On	3Vdc

2.2. Seven Level Seven Switch MLI Topology

Seven Level Seven Switch is designed with one H-bridge inverter along with three switches and three dc sources has shown in Figure 2. Switches S1, S2, S3, S4 are used for polarity reversal for generating the waveforms in positive and negative cycles. Switches S5, S6, S7 are used for generating the voltage levels upto 3Vdc. The switching configuration of this topology is shown in Table 2.

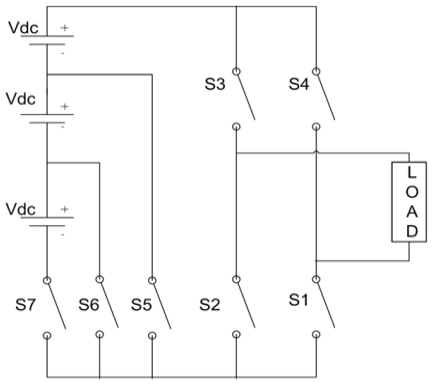

Figure 2. Configuration of seven level seven switch Topology

Table 2. Switching Pattern for seven levels nine switch topology

S.No	Switches state			Output voltage
	S5	S6	S7	
1	Off	On	On	Vdc
2	Off	On	Off	2Vdc
3	On	Off	Off	3Vdc

2.3. Seven level six switch with four dc sources MLI Topology

This structure is designed with six switches without H-bridge and four dc sources is used. Switches S6. S7 are used for generating the pulses in positive and negative sequences and the switch S1 is connected to the load it is used only when all the switches are open to produce zero voltage level. Switch S2, S3, S4 are used to generate the levels Vdc, 2Vdc and 3Vdc in both the positive and the negative levels. The circuit arrangement is shown in Figure 3. The switching topology of seven level six switches is shown in Table 3.

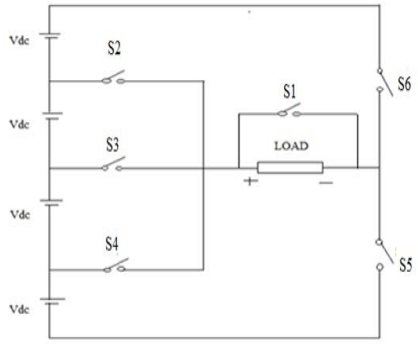

Figure 3. Configuration of 7 level 6 switch Topology

Table 3. Switching Pattern for seven level six switch topology

S.No	Switches state						Output voltage
	S1	S2	S3	S4	S5	S6	
1	Off	Off	Off	On	On	Off	Vdc
2	Off	Off	On	Off	On	Off	2Vdc
3	Off	On	Off	Off	On	Off	3Vdc
4	On	Off	Off	Off	Off	Off	0
5	Off	On	Off	Off	Off	On	-Vdc
6	Off	Off	On	Off	Off	On	-2Vdc
7	Off	Off	Off	On	Off	On	-3Vdc

3. PROPOSED TOPOLOGY

The proposed topology is simple in design and compared to the existing topologies, it consists of three dc sources and six switches. It also have additional features like only two switches conducting at an interval of time. Two switches used for polarity reversal and the remaining four switches used for waveform generation.

The generalized expression for the number of switches and the number of dc sources for the proposed topology is given by:

$$N= (2*V– 5)$$

Where N= number of levels and V= number of switches.

$$N = (2*S + 1)$$

Where S=number of dc voltage sources.

Figure 4 shows the circuit arrangement of proposed topology which consists of six switches and the resistive load is used. Switches S4&S6 are used for reversal polarity and the remaining switches are used to generate the levels in both positive and negative sides to produce the desired seven level waveforms. The switching sequence is displayed in Table 4.

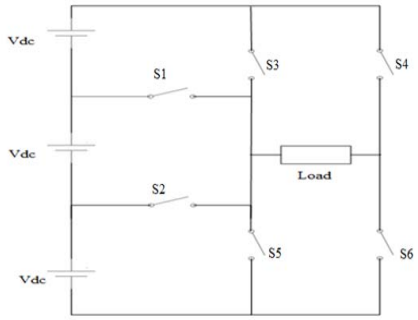

Figure 4. Configuration of seven level six switch Proposed Topology

Table 4. Switching Pattern for seven level six switch topology

S.No	Switches state						
	S1	S2	S3	S4	S5	S6	Output voltage
1	Off	On	Off	Off	Off	On	Vdc
2	On	Off	Off	Off	Off	On	2Vdc
3	Off	Off	On	Off	Off	On	3Vdc
4	Off	Off	Off	Off	Off	Off	0
5	On	Off	Off	On	Off	Off	-Vdc
6	Off	On	Off	On	Off	Off	-2Vdc
7	Off	Off	Off	On	On	Off	-3Vdc

4. PWM TECHNIQUES

The modulation technique used in this paper is level shifted modulation. Phase shifted modulation is not used because it generates more harmonics. In level shifted modulation there are four techniques phase disposition, phase opposition disposition, alternative phase opposition disposition, inverted phase disposition. Out of these four two techniques are discussed here.

4.1. Alternative Phase opposition Disposition (APOD)

Every carrier (triangular) waveforms is inverted with the next triangular waveform and it is intersected with the sinusoidal waveform. The above explanation is diagrammatically shown in figure5.

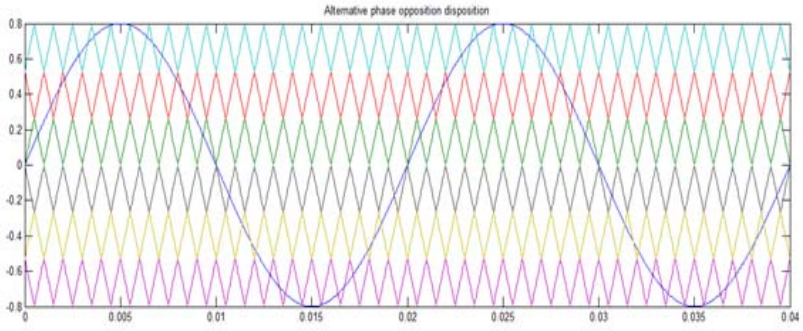

Figure 5. Alternative Phase opposition disposition PWM

4.2. Inverted Phase Disposition (IPD)

All the six triangular wave forms are inverted and it is intersected with the sinusoidal wave form it is shown in Figure 6.

When the sinusoidal wave is higher than all the 6 carrier waveforms pulses are generated in upper sequence and the sinusoidal signal is lower than all the 6 carrier waveforms pulses are generated in the lower sequence. Zero level is produced when the sinusoidal signal is lesser than lower carrier waves and it is bigger than higher carrier waveforms.

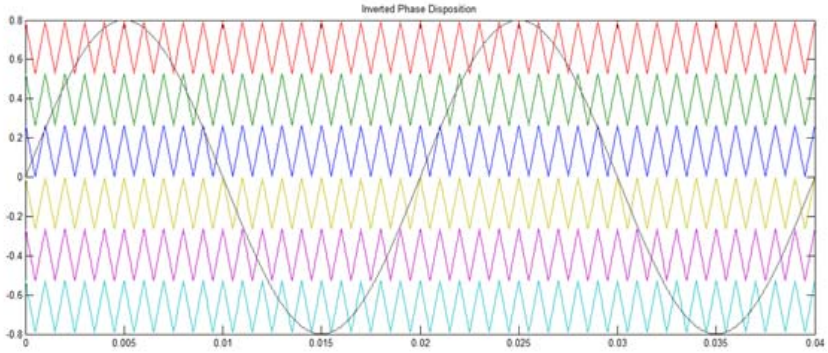

Figure 6. Inverted Phase Opposition disposition PWM

5. SIMULATION RESULTS

The simulation diagram of the proposed inverter is shown in Figure 7. All the switches used in this circuit are MOSFET. The switches S4 and S6 are bidirectional and the remaining switches are unidirectional and the resistive load is taken as 10ohms.The dc source voltage is taken as 10V. The circuit used for generating the pulses is shown in Figure 7.

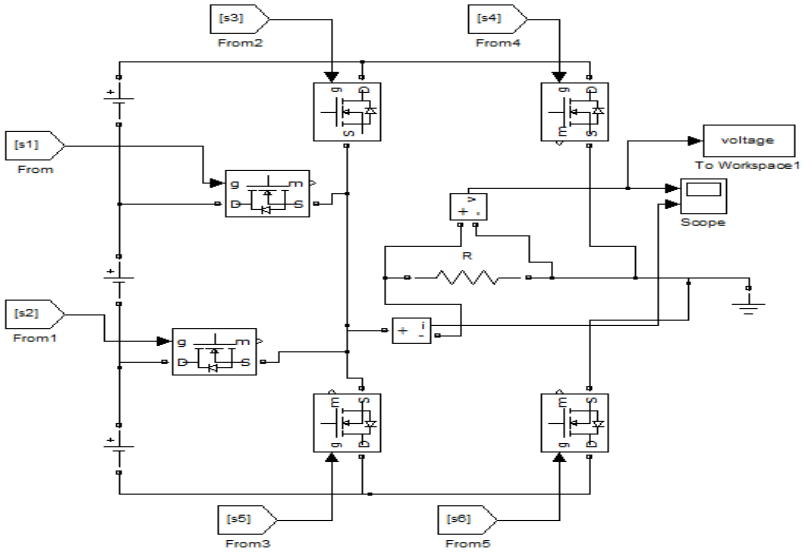

Figure 7. Simulation diagram for Proposed 7 Level MLI

The circuit is designed in Matlab/simulink and the generation of pulses has been made by comparing every carrier wave with the sine wave and the resultant pulses has been given to the appropriate switches to produce the seven level staircase waveform. The waveforms of the voltage and the current is shown in Figure 9. Figure 8 shows how the pulses are generated and the appropriate pulses is given to the respective switches.Here the switch S2 has been given with the pulses of +Vdc and -2Vdc and the switch S1 requires 2Vdc and –Vdc and the switch S3 needs 3Vdc and the switch S5 needs -3Vdc. Switches S6 requires positive polarity and the switch s4 needs negative polarity and the basic logic gates like AND, OR, NOT are used for comparing the carrier signals to produce the desired levels for the switches.

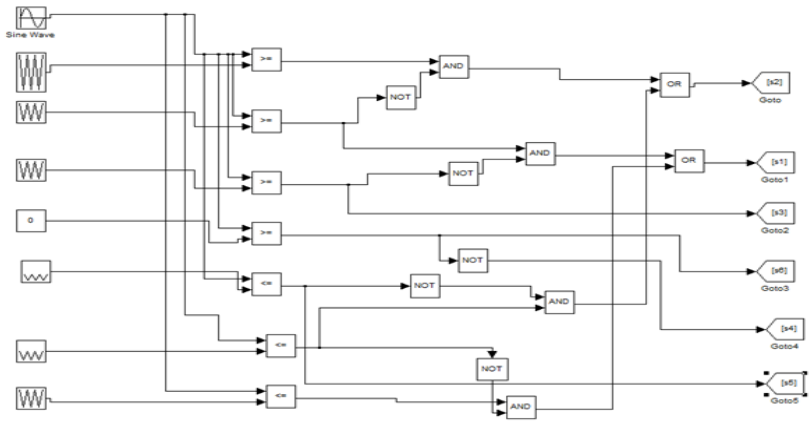

Figure 8. Pulse generation circuit for Proposed Seven level MLI

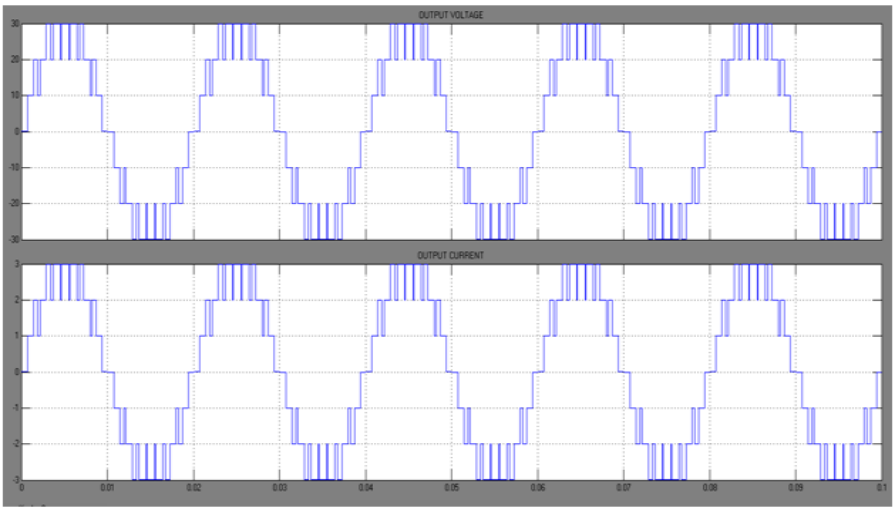

Figure 9. Ouput Voltage and Current Waveform of proposed MLI

The total harmonic distortion of APOD, IPD PWM scheme is view through the FFT window and it shown below. The comparison table has been created for total harmonic distortion and the voltage stress to show that the proposed topology is better when compared to the existing topologies.

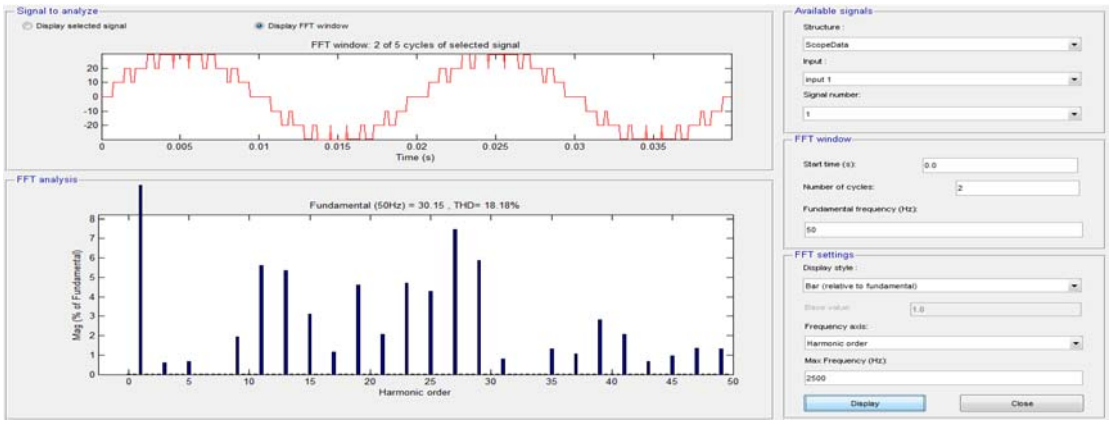

Figure 10. FFT Analysis of proposed topology using APOD

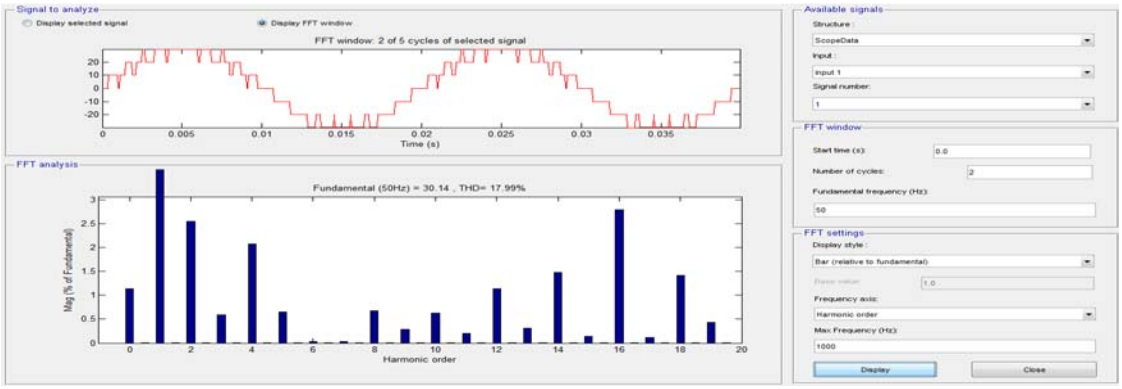

Figure 11. FFT Analysis of proposed topology using IPD

Table 5. Comparison of THD Content

PWM Technique	Symmetric conventional cascaded 7level MLI (%)	Asymmetric conventional cascaded 7level MLI (%)	7level 9 switch (%) MLI	7level, 7switch (%) MLI	7level, 6switch (%) MLI	7level, 5switch (%)MLI	Proposed 6 switch 7level (%) MLI
APOD	22.46	19.42	-	-	18.52	18.4	18.18
IPD	-	-	-	-	-	-	17.99

Table 6. Comparison of Voltage Stress across Switches

Parameter	Conventional CMLI	9switches 7level MLI	7switches7level MLI	6switches 7level MLI	5switches 7level MLI	Proposed Topology 6switches 7level MLI
Voltage Stress	5V (all switches)	11V(S5)	6V(S3)	3.33V(S3)	3.33V(S3)	2V(S3&S1)
		10V(S6)	6V(S2)	13.3V(S2)	13.3V(S2)	19V(S5)
		2V(S7) 10V(S8&S9)	18V(S1)	23.3V(S1)	23.3V(S1)	9V(S6)

Table 7. Comparison of the components of proposed multilevel inverter with the existing topologies

In-built structure	Flying capacitor	Diode clamped	Cascaded 7level	7level, 9switch	7level, 7switch	7level, 6switch	7level, 5switch	Proposed 7level, 6switch
Number of capacitor	14	6	-	-	-	-	-	-
Number of diodes	-	>=8	-	-	-	-	-	-
Number of switches	10	10	12	9	7	6	5	6
Number of dc sources	-	-	3	3	3	4	4	3

6. CONCLUSION

A new topology for seven level multilevel inverter is proposed in this paper and the simulations are done in Matlab/simulink. The simulation results are matched with the conventional seven level inverter with the reduction in THD. And the inverted phase opposition disposition method produce reduction in the harmonic distortion compared to the conventional topologies.

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