A 90nm Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor with 380MHz ARM9 and Mixed-Signal Extensions

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Outline

- Introduction to target application
- BB chip overview and performance
- Circuit level power optimization
- System level power optimization
- Power measurement results
- Conclusion

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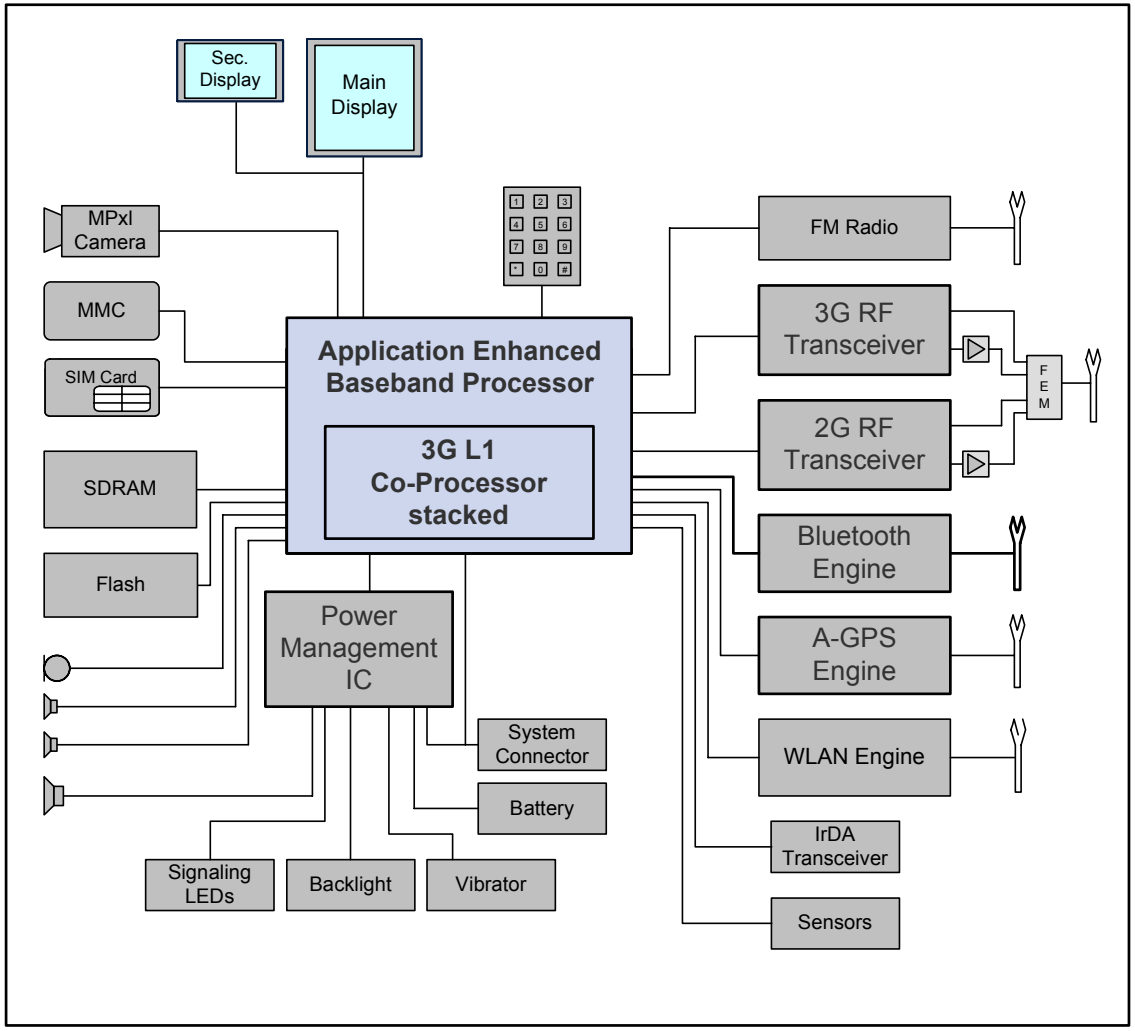
Target Application: Mid-Range Feature Phones



- Baseband processor is core component of platform
- Main use cases:
  - Phone in standby
  - Voice call
  - Music replay
  - Video record/replay
  - Video telephony
  - Data transfer
  - Gaming

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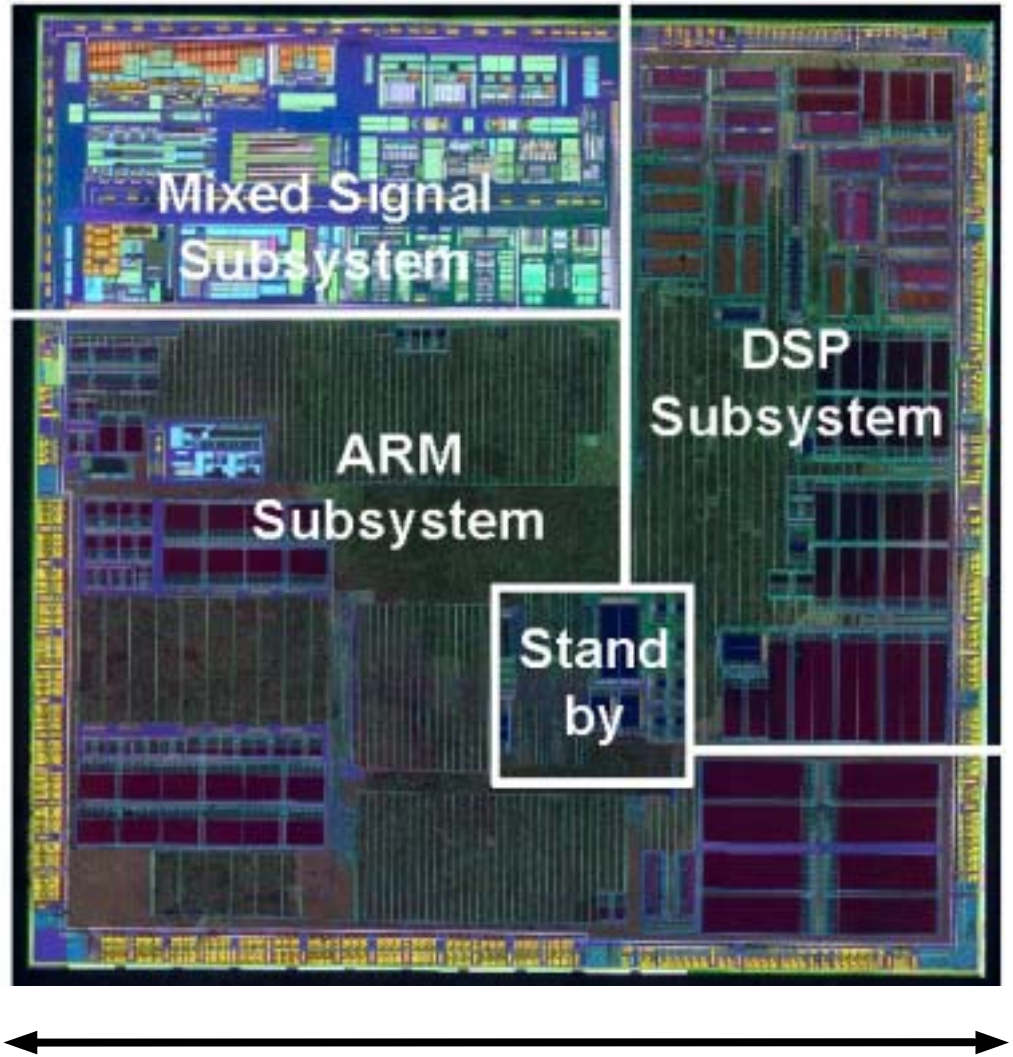
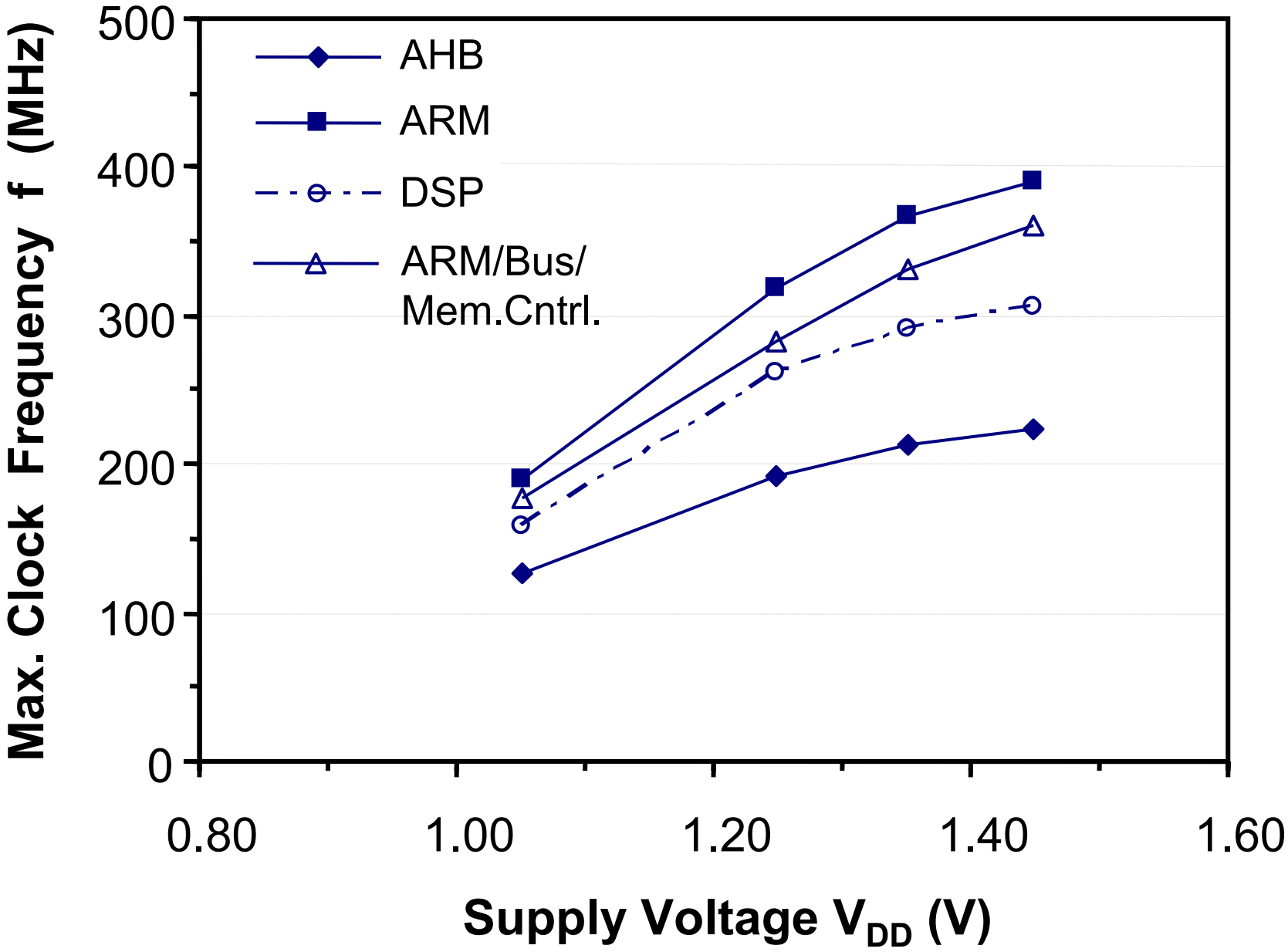
BB Processor Overview

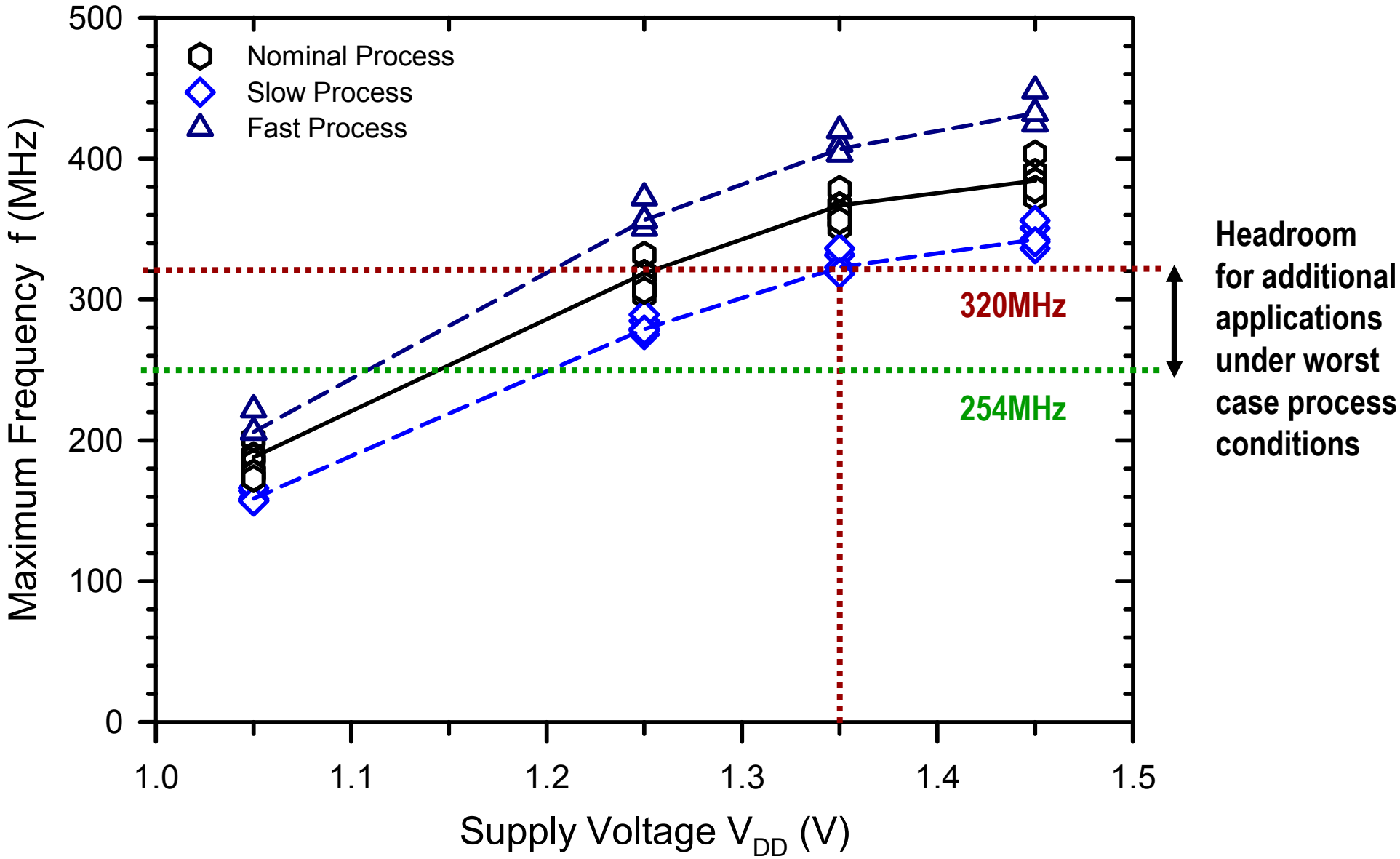


- CMOS technology
  - 90nm mixed-signal low-power
  - Dual gate-oxide for core devices
  - Triple well concept
- ARM926 for protocol stack and applications
- TEAKlite DSP subsystem for GSM/EDGE Layer 1
- Mixed signal subsystem
  - High quality audio front-end
  - I/Q RF interface

Core Performance Measurements



ARM Performance for Intended Process Splits



Performance Requirements

Application	Settings	ARM f (MHz)	DSP f (MHz)
GSM idle	sleep mode paging	0 26	0 26
GSM Voice call	6.60-AMR	26	52
Music replay	MP3	26	26
Data download	E-GPRS	52	104
Video telephony	UMTS CS, MPEG-4 (15 fps, QCIF)	104	78
Camcorder	MPEG-4 encode (20 fps, QVGA)	254	52

- ARM (380MHz) and DSP (300MHz) provide enough processing performance to fulfill requirements
- Still headroom for
  - use case combinations and
  - currently unknown use cases

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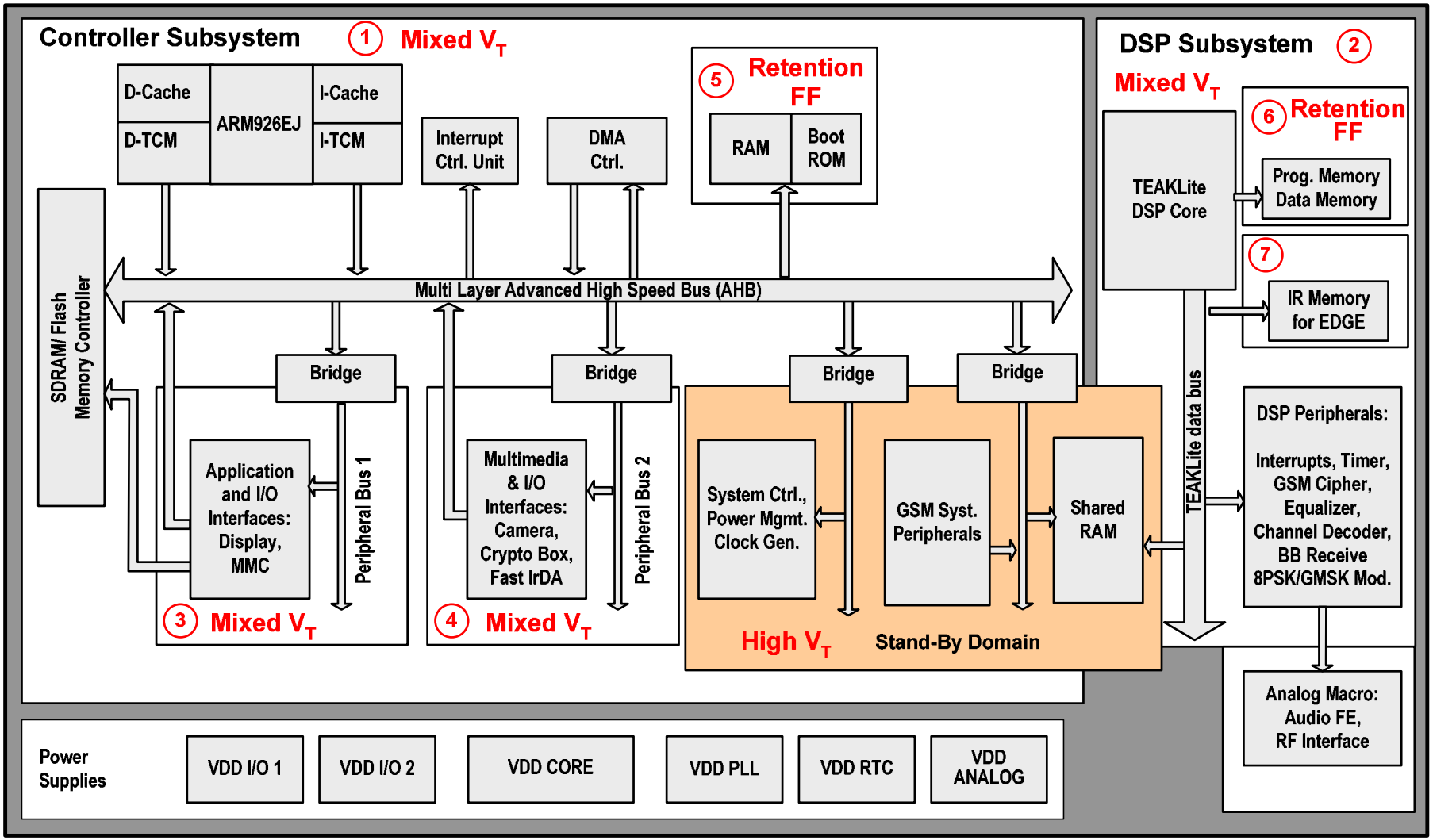
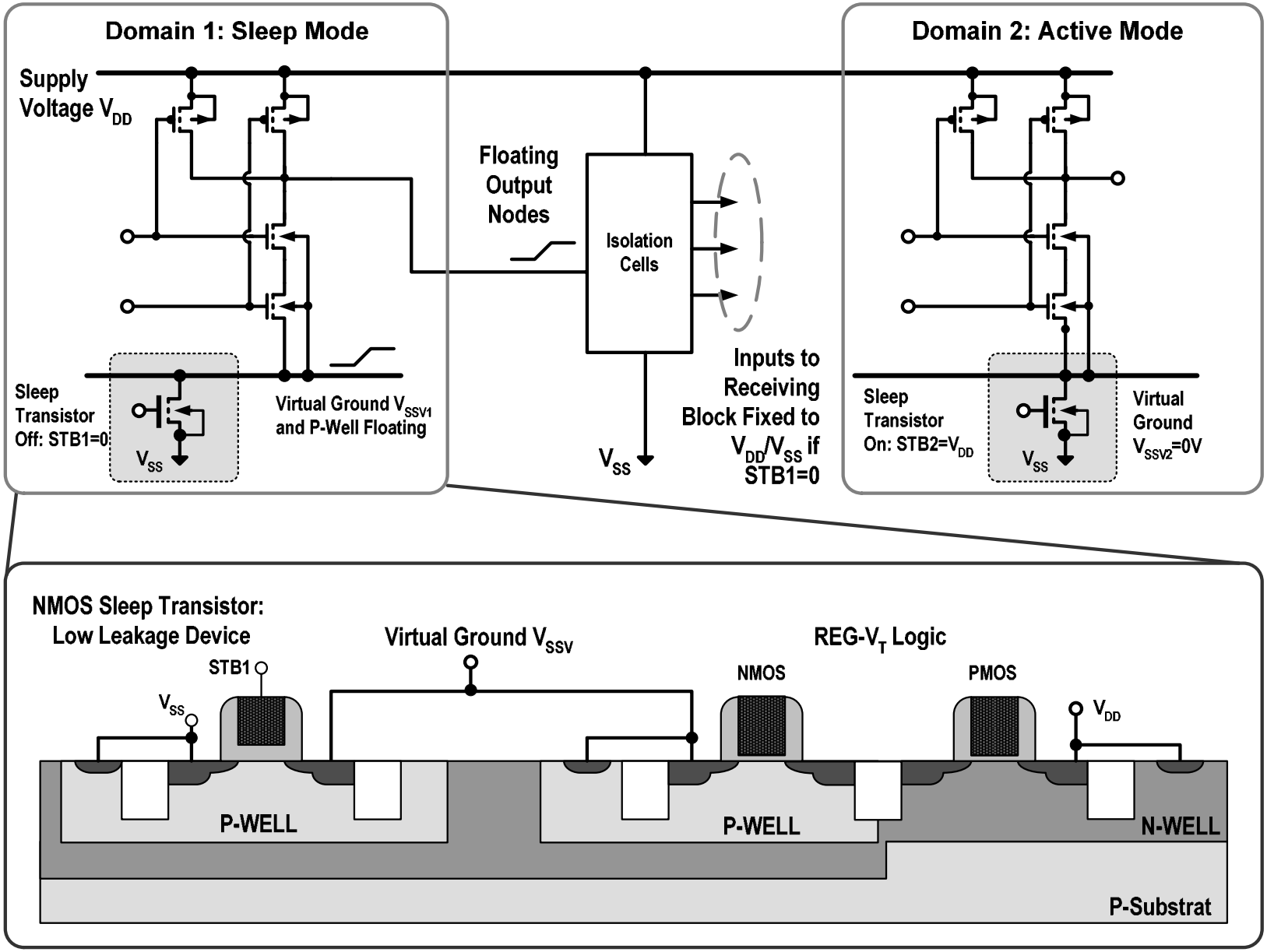
Circuit Level Power Saving Measures

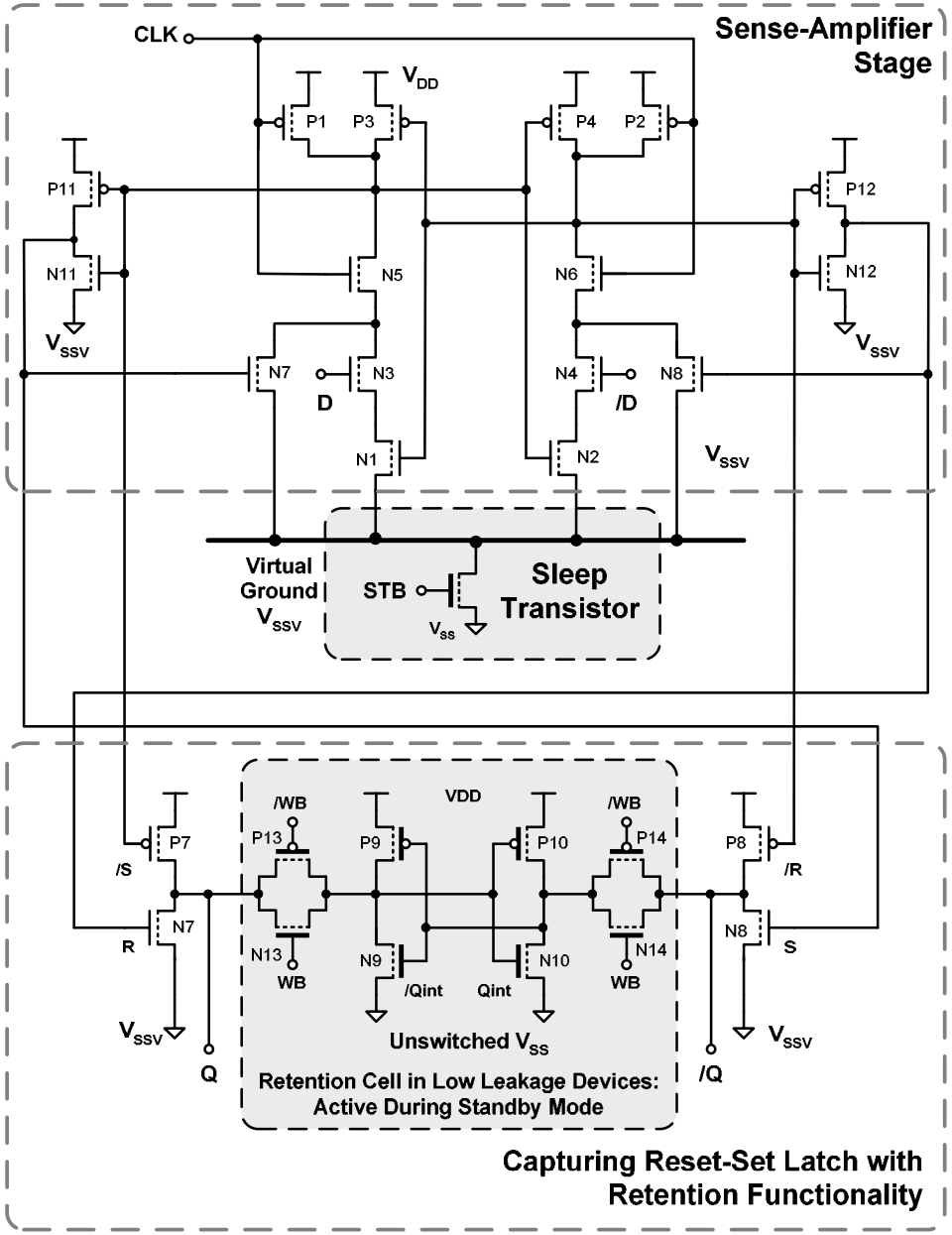


(n) … can be switched off by sleep transistors

Implementation of Sleep-Transistor Concept

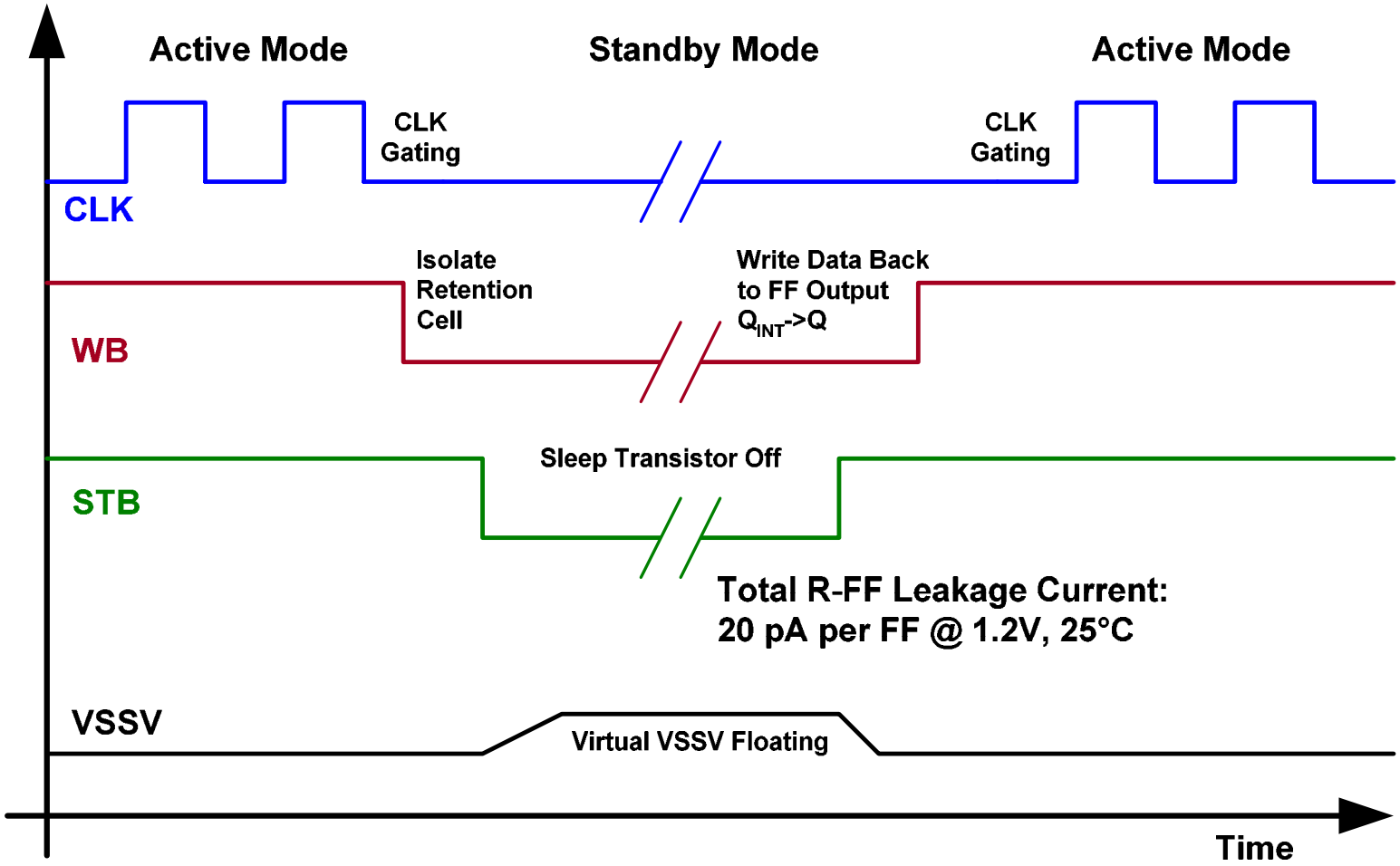


Retention Flip Flop



- **Motivation:** Store data locally for fast processor restart
- **Idea:** isolate retention cell from flip flop input stage
- **This work:**
  - Sense-amplifier based flip flop
  - Retention cell implemented in low leakage devices to eliminate gate leakage current
  - Isolation of the retention cell by transmission gates
  - Negligible delay increase due to fast switching transistors implemented in Reg-V_T devices

Retention Flip Flop: Operation



FF Performance: CLK-Q delay: $t_{CLK\text{-}Q}$=150ps @ 10ps setup time, V_{DD}=1.2V, T=110°C, slow process

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System Level Power Optimization

- **Scaling of clock frequency (f):** clocks of main building blocks are adjusted to the use case

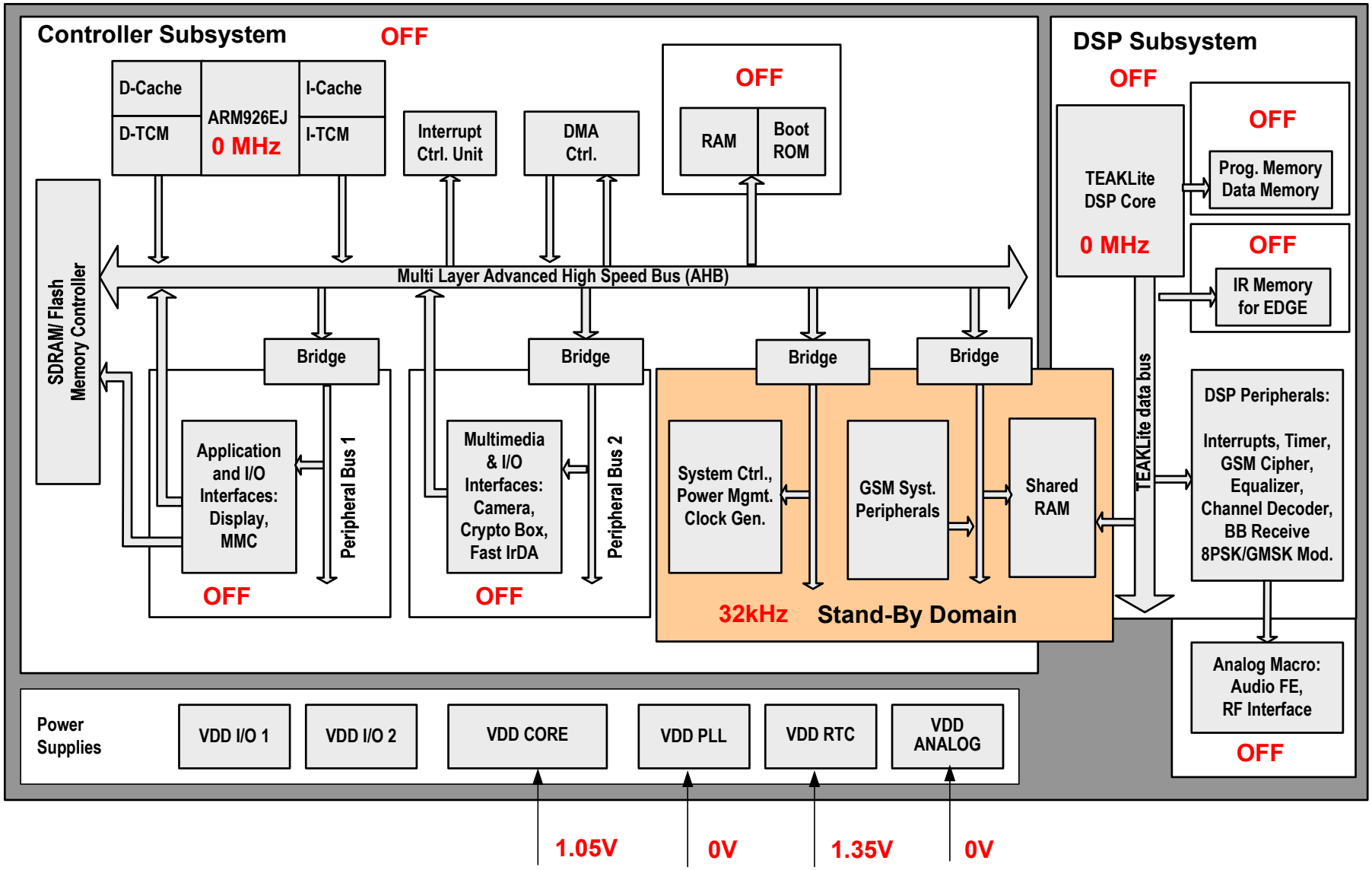
  → Reduction of dynamic power dissipation

- **Scaling of core voltage ($V_{DD\ CORE}$):** core supply voltage is adjusted to the use case

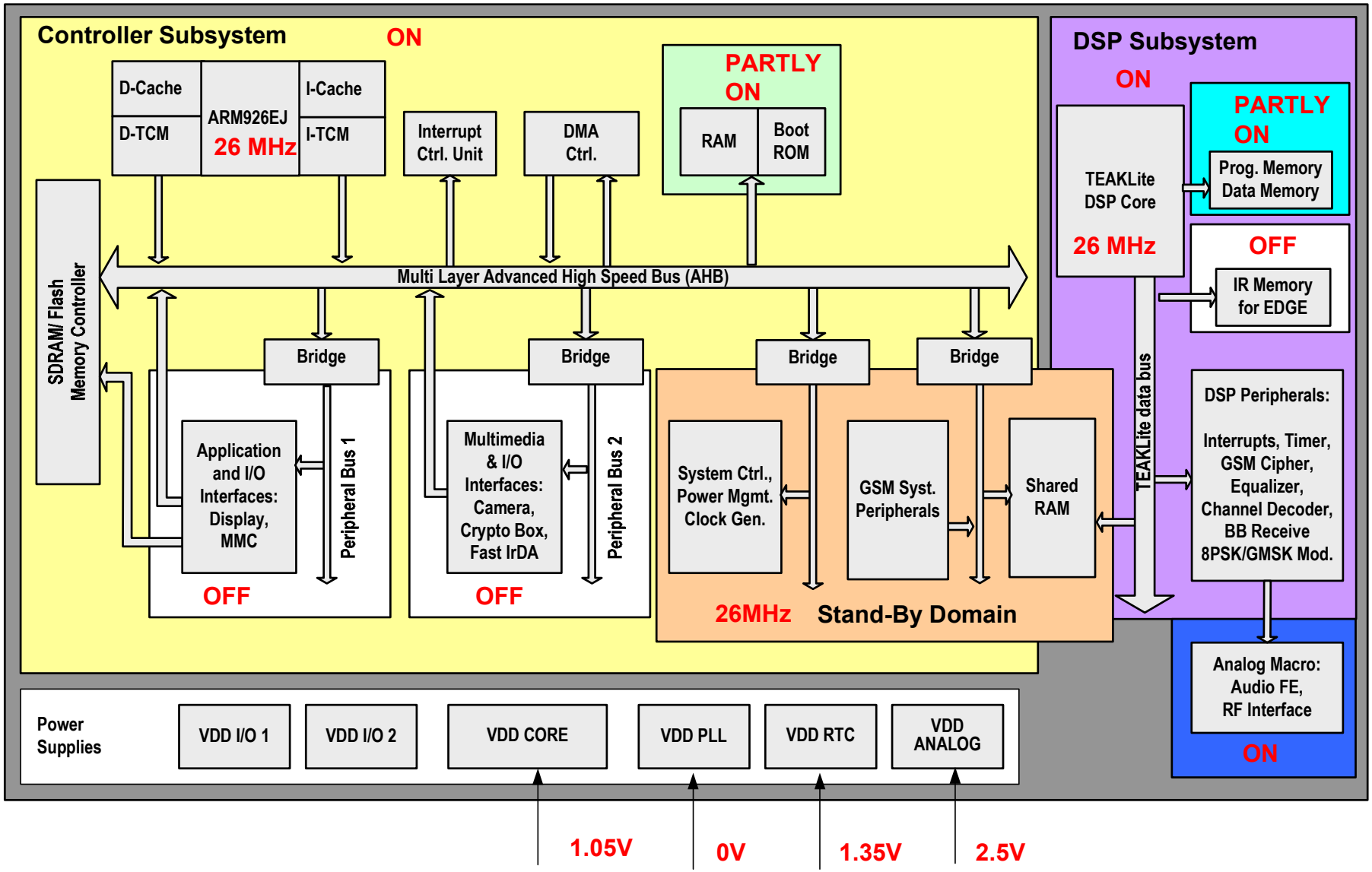
  → Reduction of both dynamic and static power dissipation

$$\text{Power dissipation} = \alpha * f * C * V_{DD}^2 + I_{leak}(V_{DD}) * V_{DD}$$

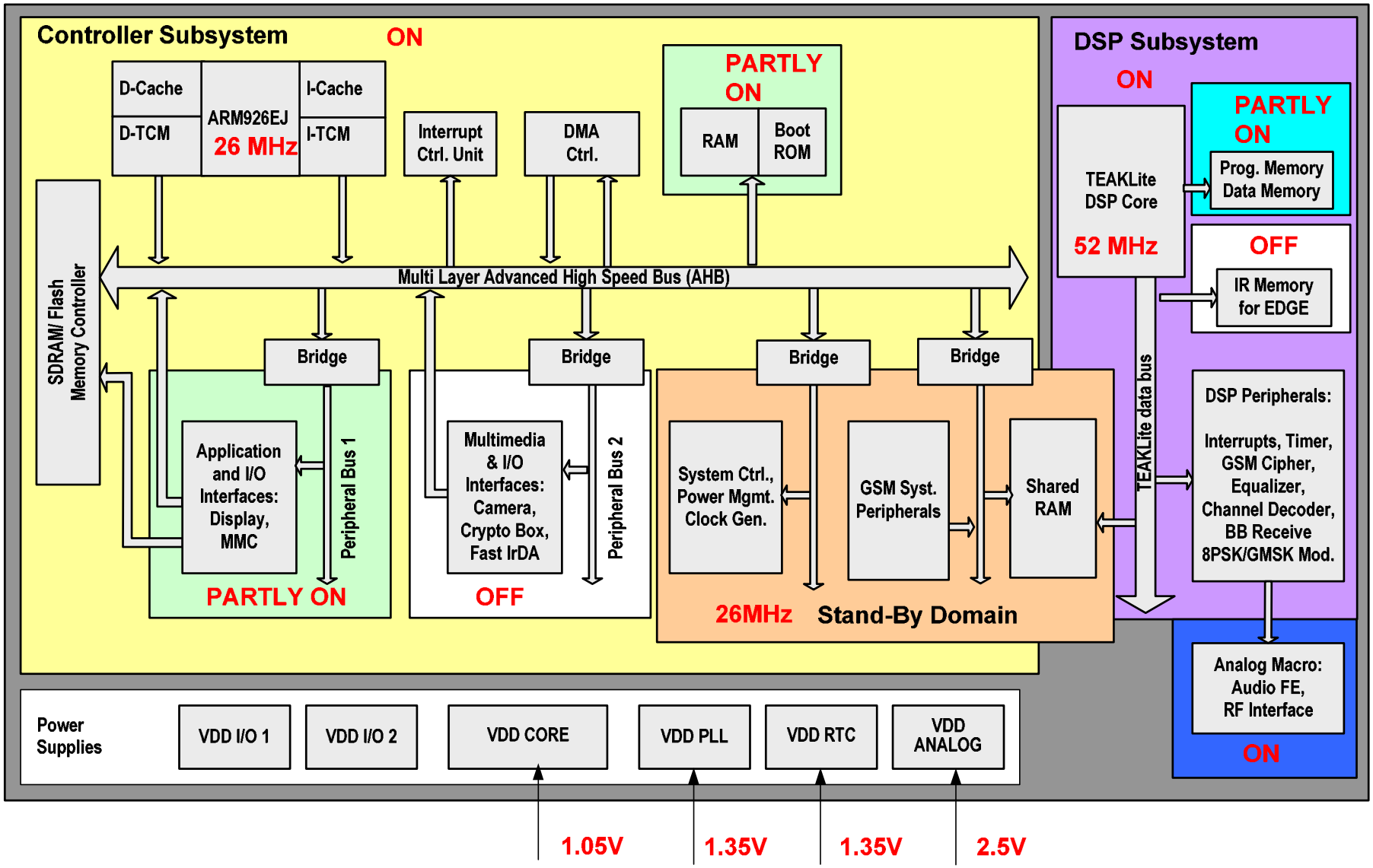
‘GSM Sleep’ Configuration



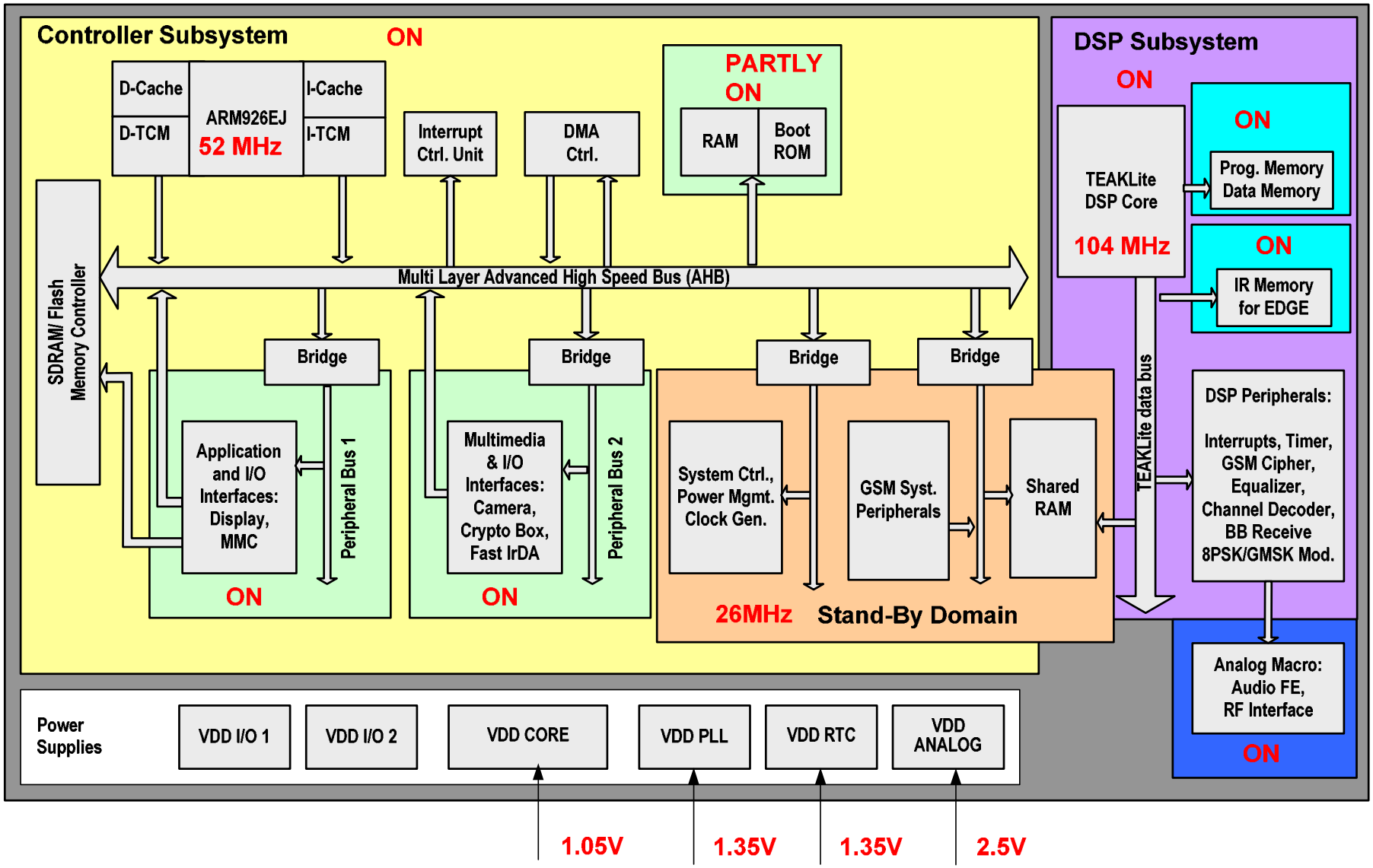
‘GSM Paging’ Configuration



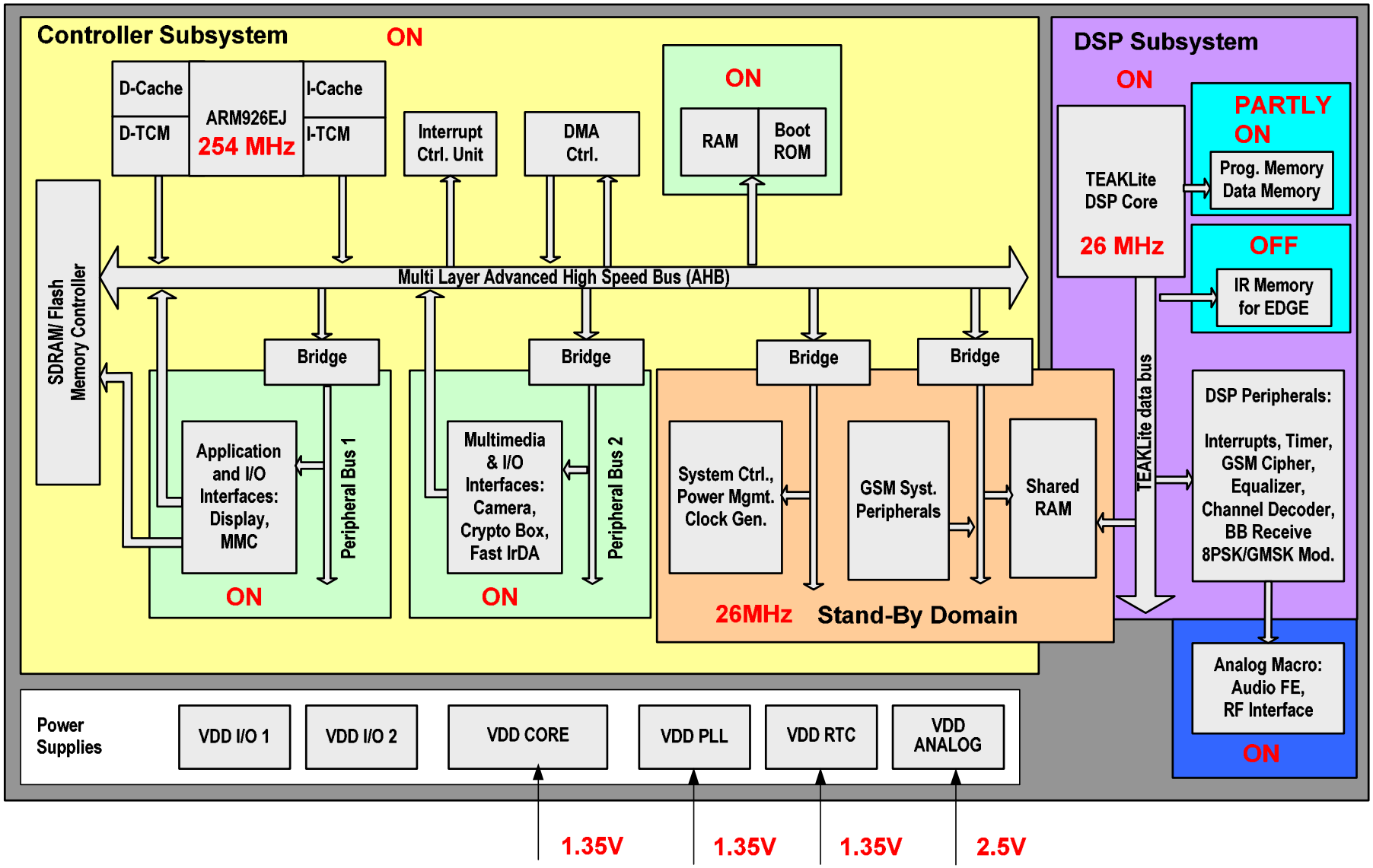
‘GSM Voice Call’ Configuration



‘E-GPRS Data Download’ Configuration



‘Camcorder’ Configuration



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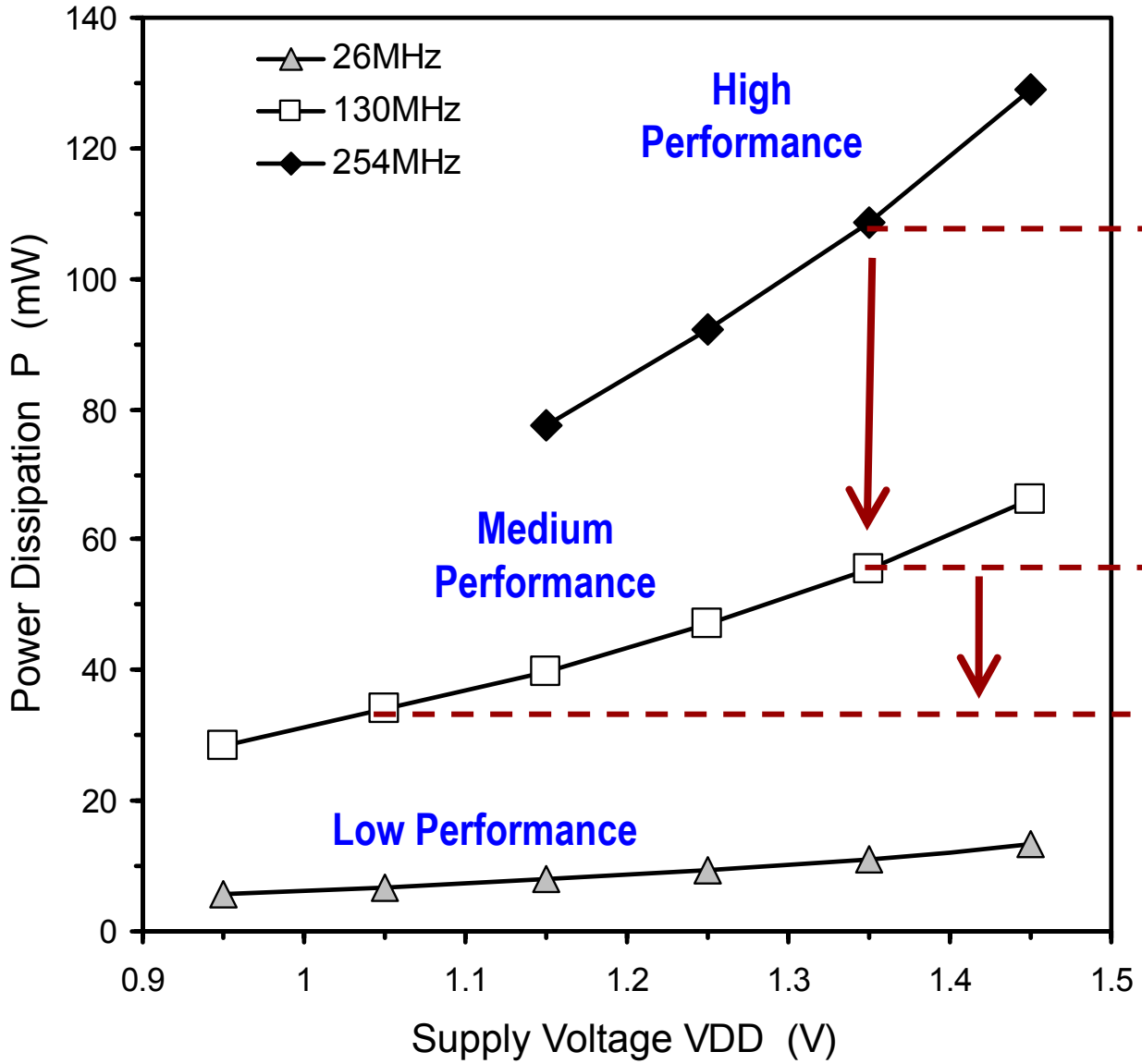
Measured ARM9 Power Dissipation

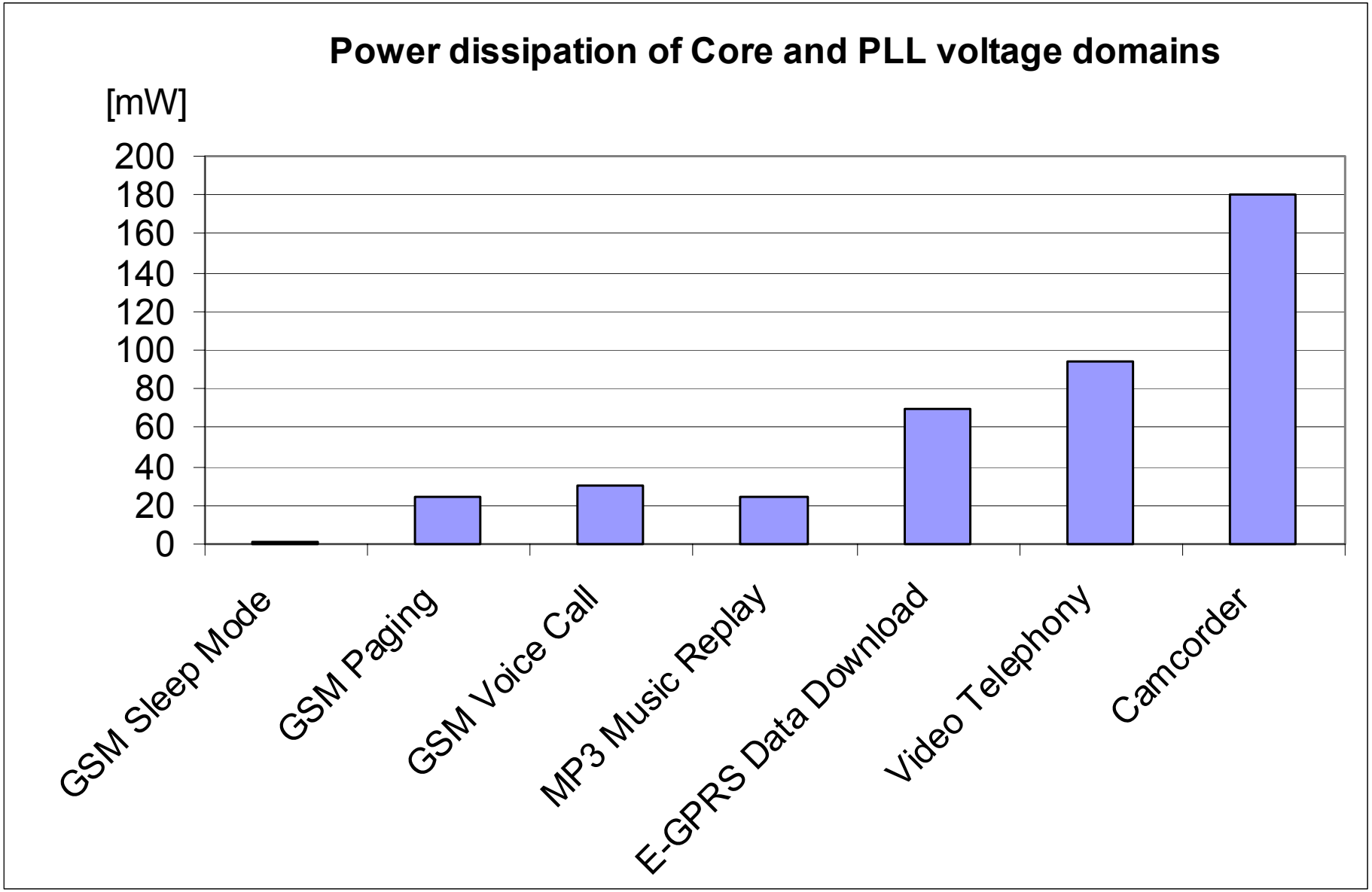


Example:

-49% reduction by **frequency scaling** from 254MHz to 130MHz

-38% reduction by **voltage scaling** from 1.35V to 1.05V

Measured Power Versus Applications



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Presented GSM/EDGE BB Chip in 90nm demonstrates

- High performance ARM9: 380MHz @ 1.35V
  - Enabling next generation mobile phone applications
- Use case driven implementation of power saving features in a novel combination
  - Standby domains and SRAMs in low leakage devices
  - Sleep transistors to switch off mixed-V_T domains
  - Retention flip-flops
  - Frequency scaling
  - Voltage scaling

Backups

90nm CMOS Core Devices at V_{DD}=1.2V

	Regular-V_t Device nFET/pFET	Low Leakage Device nFET/pFET
Poly Gate Length (nm)	70	90
$V_{t,sat}$ (mV)	370/290	550/513
Oxide Thickness t_{ox} (nm)	1.6	2.2
On-Current (μA/μm)	680/290	350/155
Off-Current (pA/μm)	300	5
6 Level Metallization, 4 Thin Metal Levels, Triple Well on Non-Epi Substrate		

References

Baseband and Wireless IC's:

[1] Y. Neuvo, "Cellular Phones as Embedded Systems", ISSCC Dig. of Techn. Papers , Feb. 2004.

[2] J. Kissing et al., "A Fully Integrated SoC for GSM/GPRS in 130nm CMOS", ISSCC Dig. of Techn. Papers , Feb. 2006.

[3] P. Royannez et al., "90nm Low Leakage SoC Design Techniques for Wireless Applications", ISSCC Digest of Technical Papers , Feb. 2005.

[4] T. Kamei et al, "A Resume-Standby Application Processor for 3G Cellular Phones", ISSCC Digest of Technical Papers,, Feb. 2004.

[5] A. Coller et al.,, Reprogr. EDGE Baseband and Multimedia Handset SoC with 64Mb embedded DRAM", ISSCC Dig. of Tech. Papers, Feb. 2005.

Low Power Circuit Techniques and CMOS Technology:

[6] T. Schafbauer et al., "Integration of High-performance, Low-leakage and Mixed Signal Features into a 100nm CMOS Technology", Symp. on VLSI Technology, 2002.

[7] S.V. Kosonocky et al., "Low-power circuits and technology for wireless digital systems", IBM J. Research and Development, Vol. 47, No. 23, March 2003, pp. 283-298.

[8] J.T. Kao et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits, , IEEE J. of Solid-State Circuits, Vol. 35, No. 7, July 2000, pp. 1009-1018.

[9] K.J. Nowka et al., "A 32-Bit Power PC System-on-a Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling", IEEE J. of Solid-State Circuits, Vol. 37, No. 11, Nov. 2002, pp. 1441-1447.

[10] L.T. Clark, F. Rici, and M. Biyani, "Low Standby Power State Storage for Sub-130-nm Technologies, IEEE J. of Solid-State Circ., Vol. 40, No. 2, Febr. 2005, pp. 498-506.

[11] S. Henzler et al, "Sleep Transistor Circuits for Fine-Grained Power Switch-Off with Short Power-Down Times", ISSCC Dig. of Techn. Papers, Feb. 2005.

[12] K. von Arnim et al., „A Low-Leakage 2.5GHz Skewed CMOS 32b Adder for Nanometer CMOS Technologies", ISSCC Dig. of Techn. Papers, Feb. 2005.

[13] M. Miyazaki et al., "A 1.2GIPS/W Microprocessor Using Speed-Adaptive Threshold-Voltage CMOS With Forward Bias, IEEE J. of Solid-State Circuits, Vol. 37, No. 2, Febr. 2002, pp. 201-217., 2005.

[14] K. von Arnim et al, "Efficiency of Body Biasing in 90nm CMOS for Low Power Digital Circuits", IEEE J. of Soli-State Circuits, Vol. 40, Mo.7, July 2005, pp. 1549-1553.

[15] B. Nikolic, V. Oklobdzija, "Sense Amplifier-Based Flip Flop", ISSCC Digest of Technical Papers, pp. 282-283, Feb. 1999.