Abstract — This work presents a micromachined RF-CMOS transformer fabricated in a commercially available 0.18μm CMOS process. Maskless micromachining post-processing is used to remove oxide and substrate material from around the transformer, reducing parasitic effects and improving the performance of the transformer.

Index Terms — baluns, CMOS integrated circuits; MEMS, maskless micromachining, Q enhancement, radio frequency integrated circuits, RF-CMOS transformers.

I. INTRODUCTION

Use of an integrated transformer proves beneficial in a wide variety of RF-CMOS circuits, including voltage controlled oscillators, mixers, and power and low-noise amplifiers [1]. The growth of the wireless communications market in recent years has increased the demand for high-performance transformers for these applications.

However, performance of RF-CMOS transformers, like single inductors, is severely limited by the presence of parasitic effects. In addition to the desired inductances and mutual inductance, the designer must consider the effects of parasitic resistances which increase noise and energy loss, and capacitances which create a resonance frequency above which the device cannot usefully function. These in turn are caused by series resistance in the transformer coils, capacitances between the coils and between them and the substrate, and loss due to induced currents in the substrate.

These effects are described by the parameters quality factor (Q) and self-resonance frequency (fsr). Since fsr and Q dictate the maximum frequency at which inductive devices may be used, as well as their usefulness due to considerations of power usage and noise, the designer must search for a device whose parameters meet the needs of the given application. Often, the performance of inductive elements is a limiting factor in the effectiveness of a RF-CMOS design [2].

Several methods have been proposed to address these deficiencies in CMOS inductors and transformers. Losses in the substrate can be decreased by using a high-resitivity substrate, made of sapphire [3], glass [4], or high-resitivity silicon [5]. Alternatively, a conductive “ground shield” can be used beneath the inductive device to prevent electromagnetic fields from entering the substrate [6]. The device can also be designed as a solenoid [7] or be vertically oriented [8], so that most fields do not enter the substrate at all, with the additional advantage that the parasitic capacitances are significantly reduced.

Series resistance can be reduced by thickening the metal coils in the vertical or horizontal direction, or by dividing the inductor into several parallel current paths [9] or varying the trace width to reduce current crowding. In addition to all these techniques, a number of others are discussed in [10].

However, the above techniques tend to have significant disadvantages. Introduction of a ground shield raises Q, but lowers fsr due to the proximity and higher capacitance between the inductor and the shield. Use of a special substrate, or special inductive structures such as the solenoid, introduces often unacceptably high additional costs. Some other techniques produce only minimal improvement in fsr and Q.

In this study we propose a novel MEMS post processing approach to improve the performance of RF-CMOS transformers. By combining MEMS with RF-CMOS, we may provide the best strategy in terms of cost, convenience, and effectiveness. This is achieved by applying micromachining as post processing to suspend a conventionally manufactured transformer above the substrate, as has been performed for spiral inductors in [11],[12]. By removing the oxide and substrate in the vicinity of the device, many parasitic elements are significantly reduced, and significant increases in both Q and fsr are expected.

II. CONCEPTS

A transformer consists of two or more inductors whose magnetic fields are coupled, so this analysis of RF-CMOS transformers begins with an analysis of RF-CMOS spiral inductors. Such an inductor is typically modeled using the pi-type equivalent circuit of Fig. 1. In this model [13]:

Rs is the nominal inductance.

Rs is the parasitic series resistance in the coil, modified to account for the skin effect and proximity effect. This term also includes the effects of eddy currents induced in the substrate by the inductor’s magnetic field.

Cp is the parasitic parallel capacitance. It represents the capacitance between the inductor coils – at the underpasses where one part of the coil passes below the other, and due to the horizontal proximity of loops in the inductor spiral.

Cox1 and Cox2 represent capacitance between the inductor and the substrate, or between the inductor and the patterned ground shield if one exists.

Csub1, Csub2, Rsub1, and Rsub2 represent parasitic effects in the substrate, and their quantities are chosen to match experimental data.
Equivalent circuit models for RF-CMOS transformers typically [13]-[15] begin with a pi-type equivalent circuit for each inductive coil, add a magnetic coupling term between the coils, and subtract parasitic elements as is necessary to match the design (i.e. the top coil of a stacked transformer has little coupling to the substrate) and to make the equivalent circuit manageable.

An appropriate equivalent circuit (following [15]) for the transformer designed in this work is shown in Fig. 2. In addition to coupling capacitances, appropriate grounds have been inserted for the transformer’s differential and single-ended coils. The circuit has three non-ground terminals, two for the differential coil and one for the single-ended coil of the transformer.

The etching process is expected to reduce most or all of the parasitic elements in this model. Cox1, Cox2, and Cox3 should be reduced in proportion to the change in dielectric constant (SiO2 to air). The mutual capacitances Cm1 and Cm2 should also be reduced but not as drastically, since in our micromachining process (see below) the horizontal dielectric layers between the top metal and underpass levels are etched away only partially.

In general, the contribution of substrate eddy currents to Rs1 and Rs2 is much diminished by a process like ours. However, our transformer includes a patterned ground shield (PGS) which serves to eliminate much of the eddy current effect even before post-processing (at the expense of lower fSR). Removing the PGS by etching will allow more fields to enter the substrate, but since the substrate will be further etched and distanced from the transformer the quantity of these fields will be lessened. It is not obvious which effect will dominate, and therefore whether Q will rise or fall when the PGS and substrate are etched. However, fSR will certainly rise since the presence of the PGS served to decrease it.

### III. Fabrication

#### A. Transformer Fabrication

A RF-CMOS transformer was fabricated in a commercially available 0.18μm CMOS process provided by Tower Semiconductor Ltd.

As shown in Fig. 3, the transformer consists of three loops on the top metal layer, forming two transformer coils which will here be referred to as L1 and L2. L1 is a single-ended coil consisting of the middle of the three metal loops. It has a diameter of 174μm. Two underpasses connect it to GSG measurement pads at the left side of Fig. 3. L2, consisting of the innermost and outermost metal loops, is a tapped differential mode inductor. Its two metal loops are joined in parallel by underpasses on the right side of the picture, and by a ground tap at the left side of the figure, which is connected to a ground pad in common with L1. Due to electromagnetic effects which modify the current distribution, the overall inductance of L2 is higher than would be expected by taking the inductances of each coil in parallel. Each of the three loops is 15μm wide (except at corners), and the spacing between them is 2μm.

Two sets of square GSG measurement pads are visible on the right and left sides of Fig. 3, colored grey. On top of these are white polygons, which represent patches of metal deposited on top of the original measurement pads. Deposition of these patches became necessary when it was decided to use a different-sized measurement probe than had originally been planned.
B. Micromachining Process

A four-step front-side post-processing micromachining process, previously presented in [11], has been developed in order to release the transformer. This high-yield process is compatible with commercially available CMOS processes to ensure low overall cost of the micromachined transformers.

The process steps are as follows:

1. An anisotropic dry etch using CHF$_3$ plasma removes the oxide material above the transformer and horizontally adjacent to its coils. Upon reaching the transformer, this etch forms a thin passivation layer on the aluminum, protecting it from the HF etching stage.

2. An isotropic wet etch using HF removes further oxide from around the transformer. The main purpose of this etch is to remove oxide in the thin (2µm wide) vertical gaps between the transformer coils, a task not always effectively done by the dry CHF$_3$ etch. However, this etch must run for only a short time lest it reach the thin metal underpasses and impair the transformer’s overall stability. Our growing expertise at performing the first CHF$_3$ etch means that the HF step can now generally be skipped, but it is included here for completion’s sake.

3. A second anisotropic CHF$_3$ dry etch removes all the remaining oxide underneath the transformer, until the substrate is reached. This step can be stopped slightly early, so as not to damage a polysilicon or metal patterned ground shield if present, in which case the fourth etching step is not performed. (In our transformer there is a ground shield, but it consists of a patterned ion implantation in the substrate and is not affected by the CHF$_3$ oxide etch.)

4. An isotropic high pressure SF$_6$ front-side dry etch forms a cavity in the silicon substrate. The depth is limited by the rate of etching of aluminum by SF$_6$. Trials have shown that the substrate can be etched at least 25µm deep without the aluminum inductor being significantly weakened. It is suspected that somewhat greater depths can be etched safely, but this awaits experimental confirmation.

Fig. 4 shows an inductor fabricated in the same technology as our transformer, successfully released using the described micromachining process. Fig. 5 shows a closer view of a different successfully released inductor.

IV. MEASUREMENTS AND RESULTS

An Agilent E8361 vector network analyzer is used to acquire two-port scattering parameters of the transformer before and after post-processing. The S-parameters are de-embedded with the help of a standard GSG calibration kit. Z-parameters are then derived from the S-parameters and used to obtain inductance and quality factor values for the transformers, according to the following equations:

\[ L = \frac{\text{Im}(Z_{11})}{2\pi f} \]
\[ M = \frac{\text{Im}(Z_{21})}{2\pi f} \]
\[ Q = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} \]

Delays in the transformer’s commercial fabrication process have prevented the application of the micromachining process and the performance of measurements by the time of writing (though it is hoped that results will be available in time for the COMCAS conference). Instead, HFSS electromagnetic simulation results are presented here as a prediction of measurements that we hope to perform in the near future.
Simulations were run for three models: the unetched transformer; the transformer with oxide removed through the first three steps of our micromachining process ("Etched oxide"); and the transformer with the substrate etched to a depth of 25µm in addition to the oxide etching ("Etched substrate"). Results are shown in Fig. 6.

For the simulated “Etched oxide” process, which leaves the substrate unetched to preserve the patterned ground shield, the micromachined transformer’s $f_{SR}$ was increased from 20.6 to 25.1GHz (22%), and its peak quality factor increased from 16.4 at 9GHz to 17.3 (5%) at 11GHz, compared to the unprocessed transformer. These values are for the transformer differential coil; similar improvement was obtained for the single-ended coil. Q improvement is visible only at high frequencies, since at low frequencies most loss is caused by series resistance rather than substrate currents, and our process does not affect series resistance.

The “Etched substrate” process was expected to show higher $f_{SR}$ than when only the oxide was etched. In fact, slightly lower $f_{SR}$ (24.8GHz) was observed with the substrate etched than without. The discrepancy is attributed to the simulation environment: since no patterned ground shield was present in the “Etched substrate” simulation, its model contained far fewer elements and the generated mesh was substantially different. Physical measurements are expected to resolve this discrepancy. Q is improved relative to the unprocessed transformer, but it cannot be determined whether Q will be improved relative to the “Etched oxide” transformer, since the simulated Q values are nearly identical and some simulation error is assumed to be present.

The magnetic coupling coefficient

$$k = \frac{M}{\sqrt{L_1L_2}}$$

rose with frequency for all simulations from about 0.35 to over 0.8 near $f_{SR}$. A rise in $k$ with frequency has also been observed in other works, such as [1]. $k$ did not appear to be affected by the post-processing except as a result of the increase in $f_{SR}$.

It is expected that S-parameter characterization of the fabricated device, to be finished in the near future, will confirm these simulation results.

Fig. 6a,b. Simulated L, Q, $k$ for the post-processed and unprocessed transformer.
V. CONCLUSION

This work presents a micromachined RF-CMOS transformer fabricated in a commercially available 0.18\( \mu \)m CMOS process. Maskless micromachining post-processing is used to remove oxide and substrate material from around the transformer. Electromagnetic simulations predict an increase of 5% in peak Q (at a 22% higher frequency) and of at least 22% in \( f_{SR} \). The micromachined transformer’s higher quality factor and increased \( f_{SR} \) will enable its use in more designs and at higher frequencies than is possible without micromachining. A single transformer was examined here, but the improvements obtained should be applicable to a wide variety of RF-CMOS transformer designs for different applications.

REFERENCES