IMPLEMENTATION OF A LOW-KICKBACK-NOISE LATCHED COMPARATOR FOR HIGH-SPEED ANALOG-TO-DIGITAL DESIGNS IN 0.18

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ABSTRACT

In traditional comparators especially for ADCs, one serious problem is the kick back noise, which disturbs the input signal voltages and consequently might cause errors at the outputs of the ADCs. In this paper, we will work on a novel ultra low-power rail-to-rail CMOS latched comparator with very low kickback noise for low to medium speed ADCs. This comparator adopts a preamplifier followed by a dynamic latch structure to achieve fast-decision, high resolution as well as reduced kick-back noise. A new adaptive power control (APC) technique is used to reduce the power consumption of the preamplifier.

Simulation results would be based on a mixed signal CMOS 0.18µm technology, at a supply voltage of 1.8V.

KEYWORDS: Kickback Noise, Latched Comparator, APC

INTRODUCTION

Recent growing interest in acquiring biomedical signals with low-voltage, low-power, miniaturized CMOS electronic devices has fostered a new era for ADC designs. For ADCs in biomedical systems, the sampling speed can be relaxed and is usually less than 200KS/s. The resolution is moderate, generally 6-10 bits. However, the power consumption and area of these systems have to be as small as possible.

As a major building block, the analog-to-digital converter (ADC) is widely used in mixed-signal circuits and systems. Basic implementation of the ADC requires the design of analog circuits such as operational amplifier (opamp), sample-and-hold (S/H), band gap reference (BGR) voltage, and comparator circuits along with the development of capacitors. Being an interface between the analog world and the digital circuit, the ADC is implemented in the same technology as the digital circuit.

As the scaling of CMOS technology continues, the supply voltage gets lower and in a low-voltage design, the low supply voltage inherently limits the maximum input voltage swing. This can eventually lead to poor signal-to-noise ratio (SNR). In order to maximize the SNR, rail-to-rail input range is expected in the ADC design. Thus, a rail-to-rail comparator is necessary to achieve the required rail-to-rail input swing.

BASIC CONCEPT OF COMPARATORS

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison.

If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.
PREAMPLIFIER BASED COMPARATOR

Now analog-to digital converter requires lesser power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The power consumption, speed takes major roll on performance measurement of ADCs.

Dynamic comparators are being used in today’s A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. However, an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor $\beta(=\mu\text{CoxW/L})$ and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators.

This offset voltage can be minimized by introducing preamplifier based comparators as shown in below:

![Fig 2: Basic Comparator Block](image)

It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise.

**Static Characteristics**

Static characteristics comprises of gain, output high (VOH) and low states (VOL), Input Resolution, Offset and Noise.

Gain of comparator can be written as:

$$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH}-V_{OL}}{\Delta V}$$  \hspace{1cm} (1)

Where $\Delta V$ is the voltage input change.

First-Order Model for a Comparator:

![Fig 3: Input Output characteristic](image)

$VI_H =$ Smallest input voltage for which the output voltage is VOH  
$VI_L =$ Largest input voltage for which the output voltage is VOL
First Order Model With Input Offset Voltage and Noise:

\[
A_V = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \tag{2}
\]

Fig 4: Input Offset Voltage and Noise

Dynamic Characteristics:

Dynamic characteristics of the comparator comprises of Propagation delay and Gain.

\[
\text{SR} = \frac{\text{d}V_{\text{out}}}{\text{d}t} \tag{3}
\]

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate. Slew rate comes from the relationship, \( I = C \frac{\text{d}V}{\text{d}t} \tag{4} \)

Where \( I \) is the current through a capacitor and \( V \) is the voltage across it.

If the current becomes limited, then the voltage rate becomes limited. Therefore for a comparator that is slew rate limited we have,

\[
\Delta T = \frac{\Delta V}{\text{SR}} = \frac{(V_{OH} - V_{OL})}{2 \cdot \text{SR}} \tag{5}
\]

where \( \text{SR} \) = slew rate of the comparator.

Basic Preamplifier

For the design of preamplifier main consideration of gain and bandwidth to increase the gain bandwidth product biasing current we can increase.

\[
A_v = \frac{g_{m0}}{g_{m2}} = \sqrt{1 + \frac{I_0}{I_2}} \tag{6}
\]

\[
f_{-3dB} = \frac{f_{\text{GBW}}}{|A_v|} \tag{7}
\]
\[ g_m = \sqrt{\frac{(2k_p \cdot w I_d)}{L}} \] (8)

\( g_m \) is Transconductance and \( k_p \) is process Transconductance.

**Fig 6: Basic Preamplifier Circuit**

Preamplifier amplified a minimum signal to a value much higher than the offset voltage of the latch. The amplified signal (output of preamplifier) is applied to the latch through transistors M5 and M6. Rapid changes in the output of the latch can propagate through the drain gate capacitances of M1 and M2 that leads the kickback noise. Smaller the latch time constant faster the response.

**Fig.7 Basic Latch Circuit**

**BASIC OUTPUT BUFFER**

The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (0 or 1.8v). The output buffer should accept a differential input signal. The overall comparator gain is product of the gain of the preamplifier and the gain of the latch. Gain of inverters inserted after the latch does not contribute to the overall gain anymore.
KICKBACK NOISE [1]

In a common structure of a latched comparator given in the figure below. In the reset phase the switch is closed and the currents in the transistors of the differential pair depend on the input voltage. There will be a small differential output voltage because the switch has nonzero resistance—the circuit is operating as an amplifier.

When the regeneration phase starts, the switch opens and the two cross-coupled inverters implement a positive feedback; this makes the output voltages go towards 0 and vdd, according to the small output voltage found at the end of the reset phase. The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the next comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called kickback noise.

Minimization Techniques of Kickback Noise:

- Insert sampling switches before the input differential pair, which are opened during the regeneration phase.
- Reducing the voltage swing at the drain of the input transistor can reduce the kick-back noise.

1.8.2 What we used to minimize the kickback noise:

Rearranged reset switch NS2 to release the kickback noise through the diode-connected transistor.
TYPES OF COMPARATORS

A latched dynamic comparator is an ideal candidate for low-voltage low-power designs as it has benefited from the elimination of static current flowing.

Modern high-speed comparators typically have one or two stages of pre amplification followed by a track-and-latch stage. The preamplifiers are used to obtain higher resolution and to minimize the effects of kickback. The output of the preamplifier, although larger than the comparator input still much smaller than the voltage levels needed to drive digital circuitry. The track-and latch stage then amplifies it again during the latch-phase, when positive feedback is enabled. The positive feedback regenerates the analog signal into a full-scale digital signal. The track-and latch stage minimizes the total number of gain stages required, even when good resolution is needed.

Kickback denotes the charge transfer either into or out of the inputs when the track-and-hold stage goes from track mode to latch mode. This charge transfer is caused by the charge needed to turn the transistor in the positive feedback circuitry on and by the charge that must be removed to turn transistors in the tracking circuitry off. Without preamplifiers kickback enter the driving circuitry and cause very large glitches. The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called kickback noise.

CONTINUOUS-TIME COMPARATOR[6]

A continuous-time comparator does not suffer the kick-back noise problem due to the smaller variation of the input drain, which is limited from VSAT to VDD – VTH in operation, as compared to the dynamic comparator; however, the power consumption is much larger due to static current flowing, as shown in figure:

![Fig 10: Conventional Continous-Time Comparator](image)

DOUBLE CLOCK DYNAMIC LATCH COMPARATOR[5]

Trade offs for the switch sizing two transistors surrounding nclk making large them pulling down the active branch quickly, but increases the glitch size when switching on. The size of the transistors has to be kept small enough to prevent the glitches from feeding through the self biased differential amplifier to the comparator output .The size of nclk switch can be kept small, reducing parasitic capacitance on the regeneration nodes, and increasing the gain during the sensing phase(end of nclk).

There are several ways to reduce the kick-back noise in the circuit. Commonly, reducing the voltage swing at the drain of the input transistor can reduce the kick-back noise. Fig. 2 uses this technique to reduce the kick-back noise.
The circuit is in the reset mode when the CLK is low. In this mode, the latch is totally disconnected from VDD and GND by the transistors M10 and M11. In this phase, there is no PMOS pre-charging circuit and NMOS pass-transistor M7 for output charge sharing is used to equalise both the outputs to VDD/2. This helps in achieving a significant half power reduction as compared to the case when there is a pre-charging circuit. The comparing speed is also faster. The comparing speed can be further increased by increasing the widths of M4 and M6. This reduces the charge lost. The power consumption is also reduced. The circuit uses a $V_{ref}$ of $V$ and $V_{in}$ of $V$.

If the input of the comparator is greater than the reference voltage, then the circuit has to give an output of ‘1’ and if the comparator input is less than reference voltage then the output of the comparators should be ‘0’.

**IMPLEMENTED DESIGN**

Adaptive power control technique [3]
In the operation of conventional dynamic comparator, it consumes static power at the regeneration time which is usually a whole half cycle of system clock. If it can be turned off as soon as the comparator output is valid instead of whole half cycle, the power efficiency will be maximized with lowest power consumption.

We used an adaptive power control (APC) technique to implement this function. It’s a very neat concept as shown in The APC block will detect the validity of comparator’s output and generate a pulse to disable the dc path adaptively and save power.

The schematic of APC is shown in Fig.5. The output of APC is an adaptive pulse to control the comparator adequately. With careful design and optimization, the APC can be implemented by only two exor gates. It results in the minimized power dissipation, because the power of APC is extremely smaller than comparator. Since the APC will turn off comparator automatically depending on the output validity, it is irrelative to the process and bias variation.

The schematic of the new comparator is shown in fig.N1-4 and P1-4 formed the preamplifier stage while the P5, 6 and N7, 8 formed the output latch stage. The N1, N2 and PI, P2 are the merged nMOS and PMOS transistor. As a result, the comparator has rail-to-rail input range.

During the reset phase when clock is low, NS1, NS2, N5 and N6 are switched off while the reset transistors P7, P8 are turned on. This is to ensure that there is no static current in reset session. When the clock is high NS1, NS2, N5 and N6 are turned on while P8 and P7 are switched off. The input differential pairs and the latch are in conduction at the beginning of this phase. The differential input voltage is converted to a differential current and mirrored to the regenerative latch. Positive feedback at the latch enables the regeneration of a small differential voltage at yin to a full swing differential output.

To reduce the power consumption we are using here automatic power control technique consists of two exor gates.
DETAILED PROBLEM DEFINITION

1. As the scaling of cmos technology continues the supply voltage gets lower and it limits the maximum input voltage swing which leads to poor ADC signal to noise ratio(SNR).
2. We are using here dynamic latched comparator which is the ideal candidate for low voltage, low power as it eliminates the static current flowing.
3. This latched comparator suffers from intolerable kick back noise because of the large voltage swing at the drain of the differential pair. This voltage variation introduces current flow due to the source impedance the current flow generates kick back noise which can lead to erroneous comparator output.

SOLUTION METHODOLOGY

1. We can reduce the kick back noise by reducing the voltage swing at the drain of the input transistor.
2. The differential input voltage is converted to a differential current and mirrored to the regenerative latch. Which makes the circuit very immune to the kickback noise.
3. To reduce power consumption adaptive power control technique is used, which consists of two E-Xor gates. APC will turn off comparator automatically depending on the output validity, it is irrelative to the process and bias variation.

ANALYSIS

Continuous Time Conventional Comparator

Dc analysis: Gain: 22.33dB
Figure 15: Dc Waveform Between Input and Output Voltages

Fig. 16: Transient waveform

Analysis of double clock preamplifier comparator:

Dc analysis: Derivative of dc graph: Gain: 23.11dB

Figure 17: Dc Waveform Between Input and Output Voltages

Fig. 18 Transient Waveform

Charge sharing preamplifier based latch comparator
Dc analysis: Gain: 25.61dB

Figure 19: Dc Waveform Between Input and Output Voltages

Analysis of Implemented preamplifier based comparator using apc circuit

Dc analysis: Gain: 28.76dB

Figure 21: Dc Waveform Between Input and Output Voltages
RESULTS

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<td>Equivalent input noise</td>
<td>1.943µV/sq(Hz)</td>
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<td>9.97µV/sq(Hz)</td>
<td>0.00218fV/sq(Hz)</td>
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CONCLUSIONS

This paper reports a novel ultra low-voltage low-power rail to-rail comparator to be used in analog-to-digital converter designs. A simple adaptive power control circuit is also implemented. With the help of Adaptive Power Control circuit, the power consumption of the implemented comparator is reduced. The comparator consumes only 111.6µW at 50MHz clock frequency and 1.8 V power supply.

REFERENCES


