A High-Frequency Fully Differential BiCMOS Operational Amplifier

Andrew N. Karanicolas, *Student Member, IEEE*, Kenneth K. O, John Y. A. Wang, Hae-Seung Lee, *Member, IEEE*, and Rafael L. Reif, *Senior Member, IEEE*

***Abstract*—This paper presents a high-frequency fully differential BiCMOS operational amplifier designed for use in switched-capacitor circuits. The op amp is integrated in a 3.0-GHz, 2-μm BiCMOS process with an active die area of 1.0 mm$\times$1.2 mm. This BiCMOS op amp offers an infinite input resistance, a dc gain of 100 dB, a unity-gain frequency of 90 MHz with 45° phase margin, and a slew rate of 150 V/μs. The differential output range is 12 V. The circuit is operated from a $\pm$5-V power supply and dissipates 125 mW. The op amp is unity-gain stable with 7 pF of capacitive loading at each output. The op amp is a two-stage, pole-split frequency compensated design that employs a PMOS input stage for infinite input resistance and an n-p-n bipolar second stage for high gain and high bandwidth. The frequency compensation network serves both the differential- and common-mode amplifiers so the differential- and common-mode amplifier dynamics are similar. A dynamic switched-capacitor common-mode feedback scheme is used to set the output common-mode level of the first and second stages.**

I. Introduction

THE increasing interest in high-performance integrated analog and digital mixed processing systems drives the need for high-performance switched-capacitor analog circuits such as switched-capacitor filters [1] and analog-to-digital converters [2]. Such analog circuits often require high-performance operational amplifiers with a high-frequency capability and large dc gain [3]. The key advantage of implementing mixed signal systems in BiCMOS process technology is that for analog circuits, bipolar devices offer a transconductance that is generally higher compared to MOS devices, leading to, for a given area, higher speed and higher gain. The CMOS devices offer high-density logic in addition to capability for switched-capacitor analog circuit architectures. A fully differential pipeline A/D architecture is desirable for implementation in a mixed signal environment. This paper describes a fully differential BiCMOS operational amplifier that is designed for use in switched-capacitor analog circuits.

This paper is organized as follows. A brief description of the BiCMOS process will be presented in Section II. This section will give an overview of the process along with a summary of key BiCMOS device parameters. A more complete description of the process is given in [4]–[6]. The op-amp circuit will be presented in Section III. This section will describe the design of the first and second stages, the common-mode feedback network, and the biasing circuit. In Section IV, measurements of the op-amp unity-gain frequency, gain–bandwidth product, and step response will be shown.

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A. N. Karanicolas, J. Y. A. Wang, H.-S. Lee, and R. L. Reif are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139.

K. K. O was with the Massachusetts Institute of Technology, Cambridge, MA 02139. He is now with Analog Devices, Inc., Wilmington, MA 01887.

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II. BiCMOS Process Description

A. Process Overview

The focus of the BiCMOS process is on building high-precision and high-speed analog/digital mixed systems for 10-V operation [5]. The process design reflects an emphasis on high-performance analog circuit capability in addition to high-density CMOS digital circuit capability. The devices available in the process are: NMOS, PMOS, vertical n-p-n, vertical p-n-p, and poly-n^+ capacitor. A cross section of the devices in this process is shown in Fig. 1.

The process development approach is to integrate the bipolar devices into an existing twin-well CMOS process. The vertical n-p-n devices are fabricated in a selective epitaxial layer deposited after the LOCOS field oxidation step of the CMOS process [4]. This epitaxial layer is deposited on n^+ buried islands, located in p-wells. The nonoptimized vertical p-n-p bipolar structures are formed by depositing the selective epitaxial layer on CMOS p-wells, without the n^+ buried islands, thus using the wells as the collectors. Since there is no buried layer for the p-n-p, its collector resistance is much higher than its n-p-n counterpart. The interconnect system for this BiCMOS process uses a single level of metal and polysilicon. The op amp is fabricated in twin-well BiCMOS built on p/p^+ epitaxial wafers permitting independent connection of the PMOS n-well substrate.

B. Key BiCMOS Device Parameter Summary

Table I summarizes the key CMOS device parameters in the BiCMOS process [5]. The CMOS devices feature a 2-μm drawn channel length and a gate-oxide thickness of 23 nm. For the NMOS and PMOS devices, the respective values for the zero-bias threshold voltage are 0.7 and -0.75 V. The subthreshold slopes are 90.7 and 86.5 mV/decade while the back-body coefficients are 0.66 and 0.26 $V^{1/2}$ for the NMOS and PMOS devices, respectively. The drain–source breakdown voltages of the NMOS and PMOS devices were 7.0 and -20 V, respectively. The threshold voltages of NMOS and PMOS field transistors are 12.9 and -16.7 V, respectively.

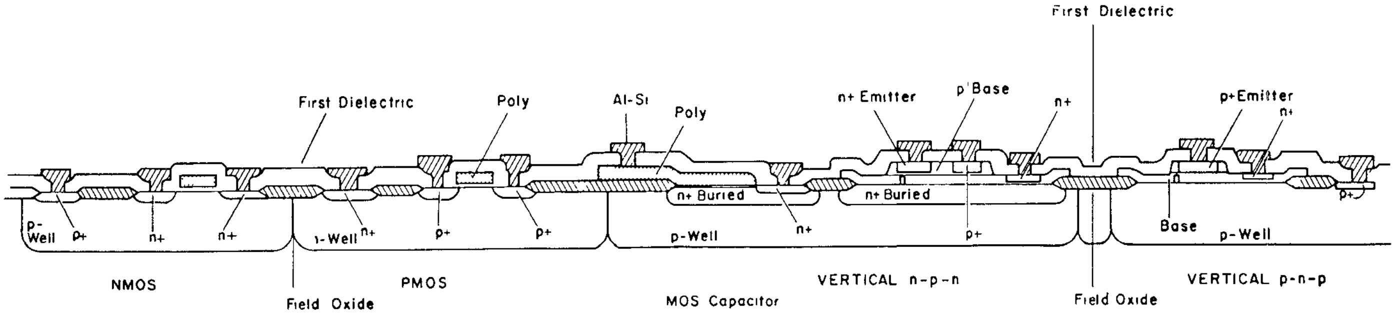

Fig. 1. Cross section of devices available in the BiCMOS process.

TABLE I
SUMMARY OF KEY CMOS DEVICE PARAMETERS IN THE BiCMOS PROCESS

Parameter	NMOS	PMOS
$L_{(DRAWN)}$	2 μm	2 μm
t_{OX}	23 nm	23 nm
V_{T0}	0.70 V	−0.75 V
Substrate Slope	90.7 mV/decade	86.5 mV/decade
Back-Body Coefficient	0.66 $V^{1/2}$	0.26 $V^{1/2}$
V_{DS} Breakdown Voltage	7.0 V	−20 V
V_T (Field)	12.9 V	−16.7 V

TABLE II
SUMMARY OF KEY BIPOLAR DEVICE PARAMETERS IN THE BiCMOS PROCESS

Parameter	n-p-n	p-n-p
Emitter Area (Min)	$(4.5\ \mu m)^2$	$(9.5\ \mu m)^2$
h_{FE} (Max)	70	70
Early Voltage	44 V	125 V
R_C	165 Ω	7.5 kΩ
R_E	11.5 Ω	11.2 Ω
R_B	250 Ω (est.)	n.a.
BV_{CBO}	33 V	> 30 V
LV_{CEO}	9.2 V	> 30 V
BV_{EBO}	4.0 V	33 V
C_{jeo}	77 fF	33 fF
C_{jco}	55.8 fF	51 fF
C_{jso}	320 fF	288 fF
f_T (Max)	3.0 GHz	200 MHz

Table II shows a summary of the key bipolar device parameters in the BiCMOS process [5]. Although the p-n-p device is not optimized, the f_T and R_C for this device can be improved by optimizing the epitaxial thickness and the p-well collector doping. The minimum-size n-p-n bipolar transistor has an emitter area of 4.5 μm×4.5 μm, a maximum h_{FE} of 70, and an Early voltage of 44 V. The series collector resistance R_C is 165 Ω and the series emitter resistance R_E is 11.5 Ω. The series base resistance R_B is estimated as 250 Ω based on op-amp performance. The collector–base breakdown voltage BV_{CBO} and the sustaining collector–emitter breakdown voltage LV_{CEO} are 33 and 9.2 V, respectively. The emitter–base breakdown voltage BV_{EBO} is 4 V. The maximum f_T is 3.0 GHz for a 4.5-μm×18-μm device with $I_C = 5$ mA and $V_{BC} = -4$ V.

III. Op-Amp Circuit Description

The BiCMOS op-amp performance objectives are derived from the requirements of high-performance switched-capacitor analog circuits. The key design goals are a high unity-gain frequency, high dc gain, and an infinite input resistance. The op amp is a fully differential, two-stage design. The fully differential architecture enables good high-frequency power supply rejection ratio in addition to increased dynamic range.

In Figs. 2, 3, and 4, the substrates for NMOS and PMOS devices are implicitly connected to V_{SS} and V_{DD}, respectively, unless otherwise indicated. The p-well substrates for all n-p-n devices and poly-n$^+$ capacitors are connected to V_{SS}.

A. First- and Second-Stage Design

Fig. 2 shows the basic op-amp circuit with the main analog signal path emphasized in bold. The op amp employs a PMOS differential pair in the first stage composed of devices M_1 and M_1'. The PMOS devices provide infinite input resistance as well as lower threshold voltage hysteresis [7] and lower $1/f$ noise power spectrum density (PSD) compared to NMOS devices. The source and substrate of the first-stage PMOS differential pair devices are connected together. This prevents the body effect from coupling source–substrate noise voltage to drain noise current, and thus, to an equivalent gate–source noise voltage.

Observing the right-half portion of Fig. 2, the input stage is actively loaded with transistor Q_2. The emitter resistance R_N is used to reduce the input-referred thermal noise due to Q_2 by reducing the effective transconductance of Q_2. However, the value of R_N cannot be increased arbitrarily as an excessively large value would lead to saturation of Q_2 for the bias currents of interest. As a result, R_N is chosen to reduce the effective transconductance of Q_2 while satisfying bias constraints.

The second stage is a bipolar design consisting of common-emitter amplifier Q_5 and cascode device Q_6. It can be shown that for a frequency-compensated two-stage amplifier, the nondominant pole frequency is $p_2 \approx -G_{m2}/C_L$ [8], where G_{m2} and C_L are the transconductance and load capacitance, respectively, of the second stage. The high transconductance of bipolar devices is used in the second stage to permit a high bandwidth by pushing the nondominant pole out to a high frequency. In addition, this high transconductance permits a high dc gain. The second stage employs a cascode structure to provide a large output resistance for high dc gain. The input impedance to the second state is relatively low compared to the output impedance of the first stage. As a result, transistor Q_3 is used as an emitter follower interposed between the first and second stages to minimize loading effects. The op amp uses a pole-splitting frequency compensation capacitor C_c and nulling resistor

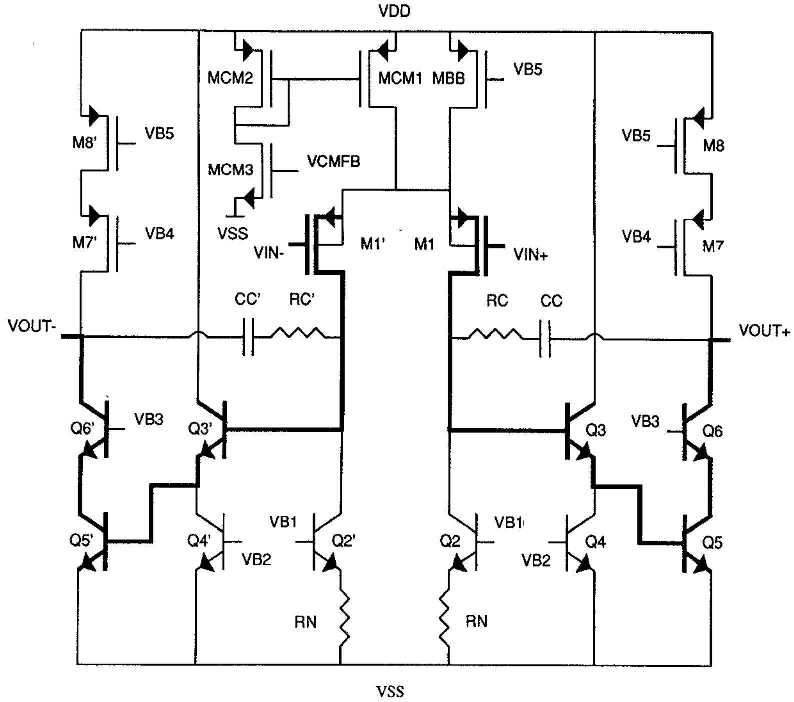

Fig. 2. Main signal path of the BiCMOS op-amp circuit.

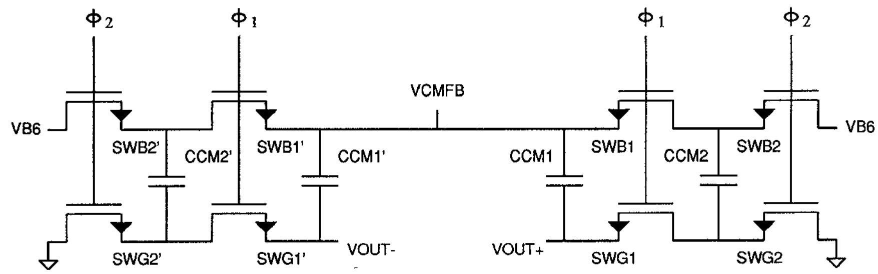

Fig. 3. Switched-capacitor common-mode feedback circuit.

R_c. A low-impedance output buffer is not needed for this op amp for the intended switched-capacitor applications.

The value of R_B for devices Q_5 and Q_5' in the second stage is important because of the pole contributed by R_B and C_π, respectively, for Q_5 and Q_5'. An excessive value of R_B for these devices can lead to peaking in the op-amp frequency response magnitude in two-stage op-amp designs because of a failure in pole splitting [9]. This peaking, of sufficient magnitude, can compromise the stability of the op amp. In the BiCMOS op-amp circuit, the bipolar devices in the second stage use a p^+ base surround around the emitter in order to minimize R_B and thus minimize the peaking.

B. Common-Mode Feedback Scheme

The fully differential op amp requires a common-mode feedback loop to set the output common-mode level. This op amp uses a dynamic common-mode feedback scheme for this purpose [1], [10]. As the op amp is a two-stage design, the common-mode feedback circuit controls the first-stage bias current to set the common-mode levels of both the first- and second-stage outputs [11].

The input of the common-mode amplifier is shown in Fig. 2 as node V_{CMFB} at the gate of transistor M_{CM3}. An increase in this voltage causes each of the op-amp output voltages to decrease. If a disturbance causes the output common-mode level to increase, the common-mode sense circuit will correspondingly increase voltage V_{CMFB}. This causes the op-amp output common-mode level to respond opposite to the disturbance, thus stabilizing the output common-mode level. It can be seen from Fig. 2 that the common-mode signal path is composed of the first and second stages of the differential amplifier in addition to devices M_{CM1}, M_{CM2}, and M_{CM3}. The frequency compensation network serves both the differential-mode and common-mode amplifiers. As a result, the common-mode and differential-mode amplifier dynamics are comparable. The unity-gain frequency of the common-mode amplifier is made slightly lower than that of the differential-mode amplifier. This is to ensure proper phase margin for the common-mode amplifier as the common-mode loop transmission has more high-frequency poles than the differential-mode loop transmission.

The dynamic common-mode output level sense circuit is shown in Fig. 3. Capacitors C_{CM1} and $C_{CM1'}$ are used to derive voltage V_{CMFB} from $V_{\text{OUT}+}$ and $V_{\text{OUT}-}$. Voltage V_{CMFB} represents the output common-mode level. By using capacitors to sense the output common-mode level, the differential- and common-mode dc gains of the op amp are not affected. In addition, the use of a capacitor sense network does not degrade the differential output range. In order to

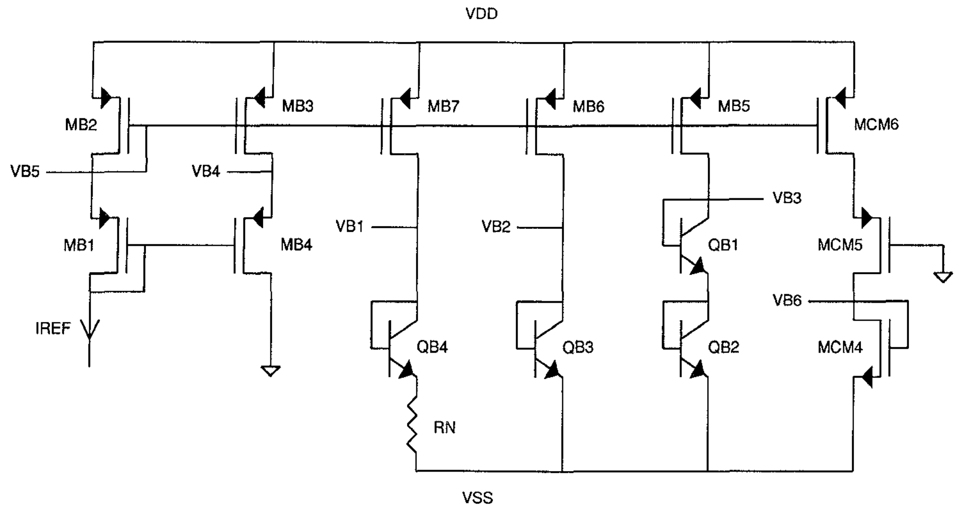

Fig. 4. Bias circuit.

provide a frequency-independent common-mode sense function with the capacitor network, the input to the common-mode amplifier must also be capacitive. As a result, a MOS device is used for this input, namely M_{CM3}. The capacitive sense network is periodically refreshed by capacitors C_{CM2} and $C_{CM2'}$ using a MOS switch network and nonoverlapping clock phases ϕ_1 and ϕ_2. The MOS switch network is composed of NMOS devices $SW_{B1}, SW_{G1}, SW_{B2}, SW_{G2}$ and $SW'_{B1}, SW'_{G1}, SW'_{B2}, SW'_{G2}$. The periodic refresh is necessary for two reasons. First, since V_{CMFB} is a capacitive node, the initial charge at this node is not determined. The refresh provides a means to establish the charge at this node such that the common-mode output voltage is at the desired level. Second, the refresh compensates for leakage currents at node V_{CMFB}. Between refresh cycles, the leakage currents are integrated by the common-mode amplifier and capacitors C_{CM1} and $C_{CM1'}$. Without refresh at sufficient rate, the deviation in the output common-mode level, with respect to a desired level, becomes excessively large between refresh cycles. Thus, the refresh rate must be high enough so that this deviation is at an acceptable level. Bias voltage V_{B6} adjusts the set point for the common-mode feedback loop. This set point is determined such that the output common-mode level is at ground potential, as split power supplies are used.

C. Bias Circuit

Fig. 4 shows the bias circuit for the op amp. Current sources with an "improved cascode" [8] structure are used to provide larger output compliance along with higher effective output resistance for the PMOS active loads in the second stage. As shown in Fig. 2, devices M_7, M_8 and M'_7, M'_8 compose these active loads. The bias reference portion for these devices, and the remainder of the bias circuit, is composed of devices M_{B1}, M_{B2}, M_{B3}, and M_{B4}. Emitter resistance R_N is included between the emitter of Q_{B4} and V_{SS} in order to maintain a 1:1 current mirror ratio between Q_{B4} and Q_2, Q'_2. Devices Q_{B3} and Q_4, Q'_4 compose a current mirror used to bias the emitter followers Q_3, Q'_3. Diode-connected devices Q_{B1} and Q_{B2} are used to derive a bias voltage for cascode devices Q_6, Q'_6. A single external current source is used to bias the op amp.

TABLE III
SUMMARY OF BiCMOS OP-AMP MEASUREMENTS

Parameter	Measured Value
dc gain	100 dB
unity-gain frequency	90 MHz
phase margin	45°
slew rate	150 V/μs
capacitive loading per output	7 pF
differential output range	12 V
power supply	± 5 V
power dissipation	125 mW
active die area	1.0 mm$\times$1.2 mm

IV. Op-Amp Measurements

Experimental results are summarized in Table III. The measured parameters are as follows: dc gain of 100 dB, unity-gain frequency of 90 MHz, phase margin of 45°, slew rate of 150 V/μs, capacitive loading of 7 pF per output, differential output range of 12 V, $\pm$5-V power supply, and 125-mW power dissipation. A 100-μA external current source was used to bias the op amp. The op amp is unity-gain stable with the above capacitive loading. The dynamic switched-capacitor common-mode feedback was engaged for all op-amp measurements. The associated clock period was 6 μs for ϕ_1 and ϕ_2, respectively. For linear operation, each op-amp output can swing to within 2 V of a $\pm$5-V power supply for zero output common-mode level. Thus, each output can swing 6 V so the differential output range is 12 V. For $\pm$3.5-V power supply, the differential output range is 6 V. Although the differential input-referred thermal noise PSD was not measured, the simulated value was 1.21×10^{-16} V^2/Hz or 11 nV/$\sqrt{\mathrm{Hz}}$. A photograph of the op-amp die is shown in Fig. 5. The active die area is 1.0 mm$\times$1.2 mm.

In Fig. 6, the results of the unity-gain frequency measurement are shown. For this measurement, the op amp is operated in an open-loop configuration. The top waveform is the differential input at 500 mV/div and the bottom waveform is the differential output at 500 mV/div. The time scale is 5 ns/div. With an input frequency of 90 MHz, it is seen that the input and output magnitudes are equal. The output waveform is 135° phase shifted with respect to the input

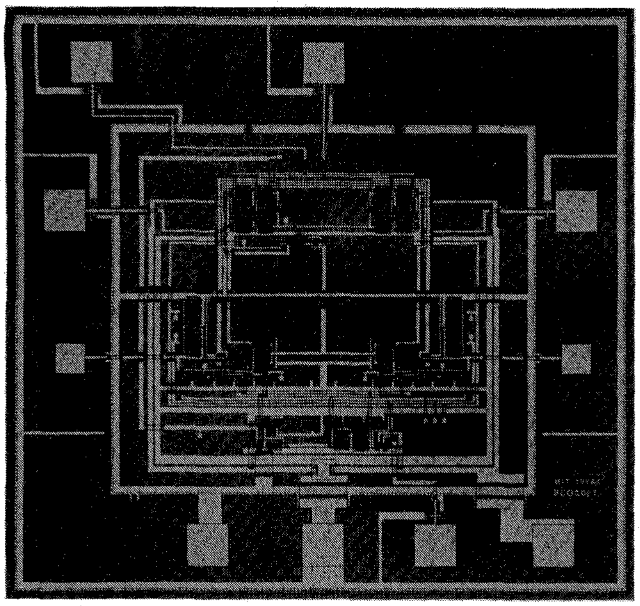

Fig. 5. Die photograph of the BiCMOS op amp.

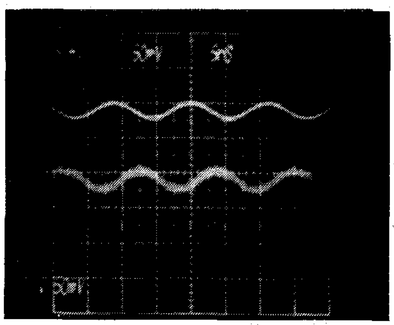

Fig. 6. Unity-gain frequency measurement. Top: differential input, 500 mV/div. Bottom: differential output, 500 mV/div. Time scale: 5 ns/div. Unity-gain frequency is 90 MHz with 45° phase margin.

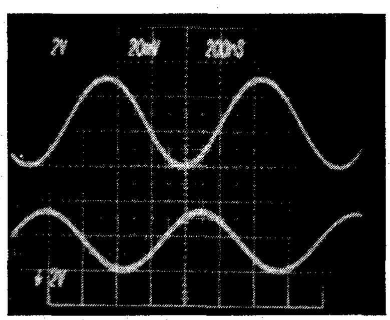

Fig. 7. Gain–bandwidth product measurement. Top: differential input, 20 mV/div. Bottom: differential output, 2 V/div. Time scale: 200 ns/div. Gain–bandwidth product is 110 MHz.

waveform. Thus, the unity-gain frequency is 90 MHz with a 45° phase margin.

In Fig. 7, the op-amp is configured for a closed-loop gain of -100. The top waveform is the differential input at 20 mV/div and the bottom waveform is the differential output at 2 V/div. The time scale is 200 ns/div. With an input frequency of 1.1 MHz, the output magnitude is reduced 3 dB compared to a lower frequency case, for constant input magnitude. In addition, the output waveform is about 45° phase shifted with respect to the input waveform, compared to a lower frequency case. Thus, the -3-dB frequency of the closed loop is 1.1 MHz. This indicates a gain–bandwidth product of 110 MHz for the op amp.

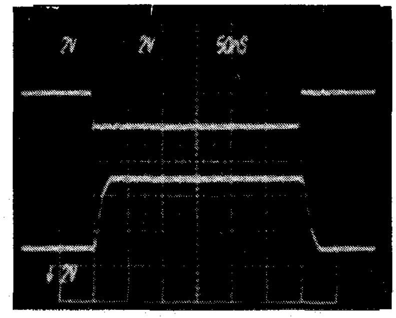

Fig. 8. Slew-rate measurement. Top: differential input, 2 V/div. Bottom: differential output, 2 V/div. Time scale: 50 ns/div. Slew rate is 150 V/μs for positive and negative output changes.

In Fig. 8, the op amp is configured for a closed-loop gain of -2. The top waveform is the differential input at 2 V/div and the bottom waveform is the differential output at 2 V/div. The time scale is 50 ns/div. Upon application of a step at the input, it is seen that the output exhibits slew-rate limiting. The step response shows a slew-rate limit of 150 V/μs for positive and negative output changes. In this closed-loop gain of -2 configuration, the loop transmission is about 1/5 to 1/6 of the op-amp loop transmission because of attenuation from the feedback network, op-amp input capacitance, and parasitic capacitance from the input pins on the chip carrier. As a result of the reduced loop transmission, the closed loop exhibits nearly a single-pole response after the slew-rate limit portion is complete for this configuration.

The op amp was configured in a closed-loop unity-gain connection in order to measure the differential-mode power supply rejection ratio (PSRR). A PSRR of greater than 45 dB was measured for frequencies up to 1 MHz for the positive and negative power supply rails.

Op-amp circuits were operated from ± 3.5-V up to ± 5.5-V power supply, using the same common-mode feedback clock period and bias current, without significant change in the performance parameters above. At ± 5-V power supply operation, it is expected that NMOS device M_{CM3} will be operating near the NMOS drain–source voltage breakdown limit of 7 V. The drain–source voltage of M_{CM3} could be reduced by placing an NMOS, or n-p-n, cascode device in series with the drain of M_{CM3}.

V. Conclusion

A fully differential BiCMOS op amp for use in high-performance switched-capacitor analog circuits has been presented. The op amp is integrated in a 3.0-GHz, 2-μm BiCMOS process. A dc gain of 100 dB, unity-gain frequency of 90 MHz, and slew rate of 150 V/μs have been demonstrated. A dynamic common-mode feedback scheme has been used to set the output common-mode level of the first and second stages.

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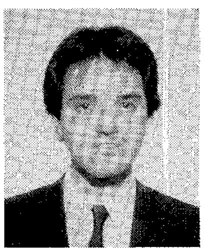


Andrew N. Karanicolas (S'85) was born in Philadelphia, PA, on July 28, 1965. He received the S.B. and S.M. degrees in electrical engineering from the Massachusetts Institute of Technology (M.I.T.), Cambridge, in 1987 and 1990, respectively. He is currently a candidate for the Ph.D. degree in electrical engineering at M.I.T.

From 1987 to 1988 he was a Teaching Assistant in the Department of Electrical Engineering and Computer Science at M.I.T. Since June 1988 he has been a Research Assistant at the M.I.T. Microsystems Technology Laboratory. His research interests include high-performance BiCMOS and CMOS analog integrated circuits.

Kenneth K. O was born in Seoul, South Korea. He received the B.S. and M.S. degrees in January of 1984, and the Ph.D. degree in September of 1989 from the Massachusetts Institute of Technology (M.I.T.), Cambridge, in electrical engineering. His M.S. thesis, "The Mobility of Carriers in the Si/SiO_2 Interface," was based on his work done at International Business Machines Corporation while he was a Co-op student. His Ph.D. dissertation was entitled "BiCMOS Technologies for Analog/Digital Applications Utilizing Silicon Epitaxial Growth."

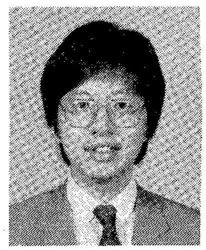
After his M.S. program, he worked as a process engineer in VHSIC Operation at Harris Corporation until he returned to M.I.T. for his Ph.D work in 1985. He is currently working on a submicrometer CMOS process at Analog Devices in Wilmington, MA. His current interests include novel process technologies and their applications to devices, VLSI circuits, and systems.

Dr. O received a Materials Processing Center Fellowship in 1985. He is a member of Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.

John Y. A. Wang received the S.B. and S.M. degrees in electrical engineering from the Massachusetts Institute of Technology (M.I.T.), Cambridge, in 1987.

His research experience includes work on analog-to-digital converters as a Research Assistant at M.I.T., and as a Member of the Technical Staff at Texas Instruments and Hughes Aircraft. Currently he is a Research Assistant at the M.I.T. Media Laboratory Vision and Modeling Group working on a doctorate degree in electrical engineering. His current research involves human and machine vision with special interest in motion and stereoscopic vision.

Mr. Wang is member of Sigma Xi, Tau Beta Pi, and Eta Kappa Nu.



Hae-Seung Lee (M'85) was born in Seoul, South Korea, in 1955. He received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1978 and 1980, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1984, where he worked on the self-calibration techniques for A/D converters.

In 1980 he was Member of the Technical Staff in the Department of Mechanical Engineering at the Korean Institute of Science and Technology, Seoul, Korea, where he was involved in the development of alternative energy sources. Since 1984 he has been with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology (M.I.T.), Cambridge, where he is now Associate Professor. Since 1985 he has acted as Consultant to Analog Devices, Inc., Wilmington, MA, and M.I.T. Lincoln Laboratories, Lexington, MA. His research interests are in the areas of integrated circuits, devices, fabrication technologies, and solid-state sensors.

Prof. Lee was a recipient of the 1988 Presidential Young Investigators' Award.

Rafael L. Reif (M'79–SM'90) was born in Maracaibo, Venezuela, on August 21, 1950. He received the degree of Ingeniero Electrico in 1973 from Universidad de Carabobo, Valencia, Venezuela, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1975 and 1979, respectively.

From 1973 to 1974 he was an Assistant Professor at Universidad Simon Bolivar, Caracas, Venezuela. In 1978 he became a Visiting Assistant Professor in the Department of Electrical Engineering, Stanford University. In 1980 he joined the Massachusetts Institute of Technology (M.I.T.), Cambridge, where he is currently a Professor in the Department of Electrical Engineering and Computer Science. He is presently working on the plasma-enhanced chemical vapor deposition of epitaxial silicon, Si–Ge alloys, and gallium arsenide, polycrystalline silicon, and titanium silicide, and on novel fabrication technologies for high-speed bipolar transistors and thin-film transistors.

Dr. Reif held the Analog Devices Career Development Professorship of M.I.T.'s Department of Electrical Engineering and Computer Science, and was awarded the IBM Faculty Fellowship of M.I.T.'s Center for Material Science and Engineering from 1980 to 1982. He also received a Presidential Young Investigator Award in 1984. He is a member of Tau Beta Pi, the Electrochemical Society, and the American Physical Society.