A Two-phase Switching Hybrid Supply Modulator for Polar Transmitters with 9% Efficiency Improvement

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Emerging polar transmitters for highly efficient and linear power amplifiers (PAs) demand for high-efficiency, high-bandwidth and low-ripple supply modulators. In [1], a linear regulator is used; however, its efficiency is low at low power levels. A switched-mode power supply (SMPS) is used in [2]; but the high switching loss due to high switching frequency (necessary for high bandwidth) limits the maximum efficiency to ~76%. A hybrid amplifier (HA) topology combining both linear amplifier (LA) and switching amplifier (SA) is used in some recent work [3,4]. In this topology, a high-bandwidth LA replicates the input envelope voltage $V_{in}$ at its output $V_{o}$, while the high-efficiency SA supplies most of the load current within its bandwidth. Yet, the switching bandwidth is finite in [3] and the LA in [4] needs to supply most of the high-frequency load current due to the exceptionally large inductor (200µH) used for realizing small output ripple; and therefore, limiting the dynamic efficiency. Figure 10.1.1 shows the proposed wideband HA featuring two-phase switching (2PHSW) for reducing ripple and improving static efficiency, and a feedforward bandpass filter (FF-BPF) for enhancing dynamic efficiency.

2PHSW has been used in a SMPS for polar transmitters [5] but it brings additional advantages when being used with HA. To match an equivalent design using 1PHSW, halved phase frequency and twice the size of inductance can be used in 2PHSW. Despite the same phase inductor current ripple in two cases, the ripple cancellation in 2PHSW has two merits. First, the output ripple is reduced. Second, the reduced ripple current working into the output stage of LA results in less loss ($\text{ripple}_{LA}$ loss) since the ripple current overlaps the drain-source voltage of the output device of the LA. 2PHSW is very useful in this regard as in the PWM control, the largest current ripple is at 0.5 duty ratio (middle power level) and this is where ripple cancellation is most complete in 2PHSW. With 2PHSW, ripple-$\text{ripple}_{LA}$ loss is reduced by ~50% for an evenly distributed voltage span across the output. Finally, if the same silicon area is allocated for power switches, the switching loss is halved in 2PHSW as compared to 1PHSW since switching frequency is halved. The lower switching loss is especially important at low output power levels where the switching loss dominates. The drawback of 2PHSW is the need for two inductors. Yet, noting that two inductors are used in some prior designs [3,5], and small inductors (500nH) are used in the design to improve large-signal tracking of SA, the cost is acceptable.

The LA is an OTA buffered by a Class-AB super-source-follower output stage to provide low output impedance for attenuating the output ripple due to SA [3]. Miller compensation with a pullup resistor compensates the local super-source-follower loop. The resistor is implemented as a switch, which is open at high load condition to lower the mid-band output impedance, and closed at low load condition to ensure the loop stability. With only 15mA of bias current, the LA achieves a UGF of 40MHz (including resistive feedback), output impedance of 0.25Ω at 20MHz, and output swing of 0.4-to-2.8V from a 3.3V $V_{dd}$.

Figure 10.1.4 shows the measured efficiency of the HA with a 3.82µA resistive load. At DC input, three curves (2PHSW_HA at 10MHz phase frequency, 1PHSW_HA at 20MHz by using a common ramp for both PWM comparators, and the mode with only LA enabled) are plotted. Similar to previous work [4], HA shows more than 10% efficiency gain than using LA only. The efficiency of LA-only mode at full-power region is not taken since the metal width of interconnects in the LA was not designed to support full-load current. Compared to 1PHSW, 2PHSW achieves up to 9% efficiency gain at low- to middle-power levels, where the PA operates most often in typical conditions. The maximum efficiency is 89% at maximum output of 33dBm; and efficiency still reaches 60% at 10dB back-off. Dynamic efficiency when HA is tracking full-wave (0.4 to 2.8V) rectified sine waves (RSWs) of different frequencies is also shown. Without FF-BPF, the efficiency drops to ~72% as early as 1MHz due to the finite bandwidth of the generic current loop. When FF-BPF is enabled, the efficiency is raised by 8 to 12% and the efficiency curve levels off at higher frequency of 4MHz due to FF-BPF's bandwidth extension.

Figure 10.1.5 shows waveforms when HA tracks full-wave RSWs. $V_{o}$ tracks $V_{in}$ well at both 500kHz and 4MHz. At 500kHz, ripple cancellation is clearly seen in total inductor current. There is an imbalance (~150mA) between $i_{L1}$ and $i_{L2}$ due to the offset in OTAs for $i_{L}$-sharing, causing some efficiency penalty but not affecting the tracking performance much. At 4MHz (beyond $i_{L}$-sharing loop bandwidth of 1MHz), current sharing is still in effect although it is on the basis of 2 RSW cycles. Figure 10.1.6 shows the HA tracking a WCDMA envelope (which is extracted from the figure in [2]). $V_{o}$ tracks $V_{in}$ very well, and $i_{L}$ resembles $i_{L1}$ so well that LA does not need to drive much AC-current. Such fast tracking performance is comparable to the previous work in [2] and [4], while both static and dynamic efficiencies are greatly improved. The measured peak-to-peak output ripple is below 40mV. These measurement results suggest that the proposed 2PHSW HA can be a good candidate as the supply modulator of PA in wideband polar transmitters. Figure 10.1.7 shows the micrograph of the chip, which is fabricated in a 0.35µm CMOS process. The die dimension is $1.78 \times 1.74\text{mm}^2$.

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References
Figure 10.1.1: Block diagram of the proposed two-phase switching hybrid amplifier as an RF PA supply modulator.

Figure 10.1.2: Schematic of control block including current-loop compensator, FF-BPF and inductor current sharing control.

Figure 10.1.3: Schematic of the proposed two-phase ramp generator. The design is much simpler than the commonly used DLL approach.

Figure 10.1.4: Measured efficiency of the chip. 9% (~8 to 12%) static (dynamic) efficiency gain is achieved as compared to 1-phase switching without FF.

Figure 10.1.5: Measured tracking response of full-wave RSWs of 500kHz and 4MHz. Current sharing and ripple cancellation are verified.

Figure 10.1.6: Measured tracking response to WCDMA signal. Most of the load current is supplied by high-efficiency switching amplifier.
Figure 10.1.7: Micrograph of the chip fabricated in a 0.35µm CMOS process.