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Heteroepitaxial growth of $In_{0.30}Ga_{0.70}As$ high-electron mobility transistor on 200 mm silicon substrate using metamorphic graded buffer

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We report on the growth of an $In_{0.30}Ga_{0.70}As$ channel high-electron mobility transistor (HEMT) on a 200 mm silicon wafer by metal organic vapor phase epitaxy. By using a 3 μm thick buffer comprising a Ge layer, a GaAs layer and an InAlAs compositionally graded strain relaxing buffer, we achieve threading dislocation density of $(1.0 \pm 0.3) \times 10^7$ cm^{-2} with a surface roughness of 10 nm RMS. No phase separation was observed during the InAlAs compositionally graded buffer layer growth. 1.4 μm long channel length transistors are fabricated from the wafer with I_{DS} of 70 μA/μm and g_m of above 60 μS/μm, demonstrating the high quality of the grown materials. [http://dx.doi.org/10.1063/1.4961025]

I. INTRODUCTION

InGaAs high-electron mobility transistors (HEMT) are routinely used for the fabrication of high-frequency, low power amplifiers.[1] There are typically two substrate options for commercial fabrication of InGaAs HEMTs. First, the lattice-matched InP substrate, with devices fabricated on them commonly referred to as lattice-matched or pseudomorphic HEMTs (pHEMT). Second, a GaAs substrate, with devices on them commonly referred to as metamorphic HEMTs (mHEMT).[2] For mHEMT, a buffer is employed to gradually change the lattice constant from the GaAs substrate to the desired device lattice constant, typically the $In_{0.53}Ga_{0.47}As$ lattice constant.

A new kind of circuit can be enabled by integrating of InGaAs analog devices with Si CMOS, which draws benefits from both technologies. First, it will benefit from the computing power of the Si CMOS logic. Second, it will benefit from the radio frequency capabilities of the III-V HEMTs.

The first barrier for this integration is incompatibility in wafer sizes Most Si CMOS manufacturing uses 200 mm diameter size wafers and above. Commercial InGaAs HEMTs fabricated on InP and GaAs substrates are not available in such sizes, precluding wafer-level integration with Si CMOS.

We address this integration challenge by growing InGaAs HEMTs directly on 200 mm silicon substrates, which makes them amenable to being integrated with a Si CMOS device layer directly at the wafer level. Such integration includes wafer bonding steps, and the complete flow has been described in our previous work[3,4] with the final goal of stacked CMOS and III-V as depicted in Figure 1.

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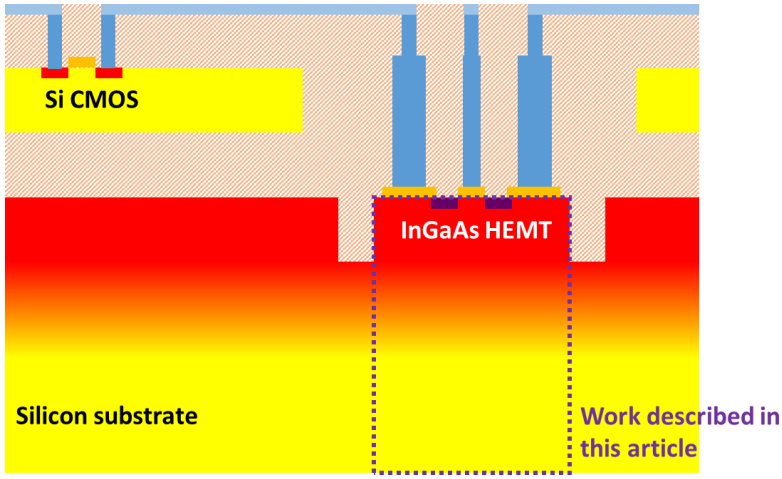

FIG. 1. Schematic of a Si CMOS device and an InGaAs HEMT device that are monolithically integrated on the same silicon substrate. This work will decribe the part highlighted by the purple square: the fabrication of an InGaAs HEMT on a 200 mm silicon substrate.

The first step to create our hybrid circuit is to grow an InGaAs HEMT layer stack on a 200 mm silicon substrate. Different techniques have been successfully developed to integrate InGaAs on silicon: blanket growth,[5,6] layer transfer by wafer bonding[7–10] (which involves a blanket growth initially), and growth in trenches on a patterned Si wafers.[11]

Blanket heteroepitaxy of InGaAs on silicon — using various buffers — typically produces threading dislocation density (TDD) in excess of 10^8 cm^{-2}.[5,7,9] TDD in the range of 10^9 cm^{-2} has been reported by GaAs growth followed by InP directly on silicon substrate,[5] while using an InAlAs compositionally graded buffer by MBE resulted in material with a TDD of 3×10^8 cm^{-2}.[9]

The compositionally graded buffer approach, when optimized, should allow the HEMT layer to reach a lower TDD. For instance, reaching InP lattice constant on a GaAs substrate with a compositionally graded InGaAs buffer has been shown to produce TDD in the 10^6 cm^{-2} range.[12] Similarly, SiGe graded buffer allows pure Ge to be grown on a silicon substrate with a TDD below 10^6 cm^{-2}.[13] During the graded buffer growth, the threading dislocations are recycled into misfit segments that relax the strain built in the growing buffer layer[14] These graded buffers are typically several micrometers thick to accommodate the misfit without generating more dislocations.

However, the graded buffer method has a drawback. In general, slower grading rates that moderate the rate of strain and misfit introduction lead to lower ultimate TDDs which are desirable. However, slower grading rates also mean that thicker buffer layers are needed to modify the lattice constant by a given amount, which would result in high wafer bow in the InGaAs grown on large Si substrate due to coefficient of thermal expansion mismatch between the III-V materials and Si. Therefore, the total buffer thickness was selected to about 3 μm. This thickness allows the InGaAs layer to reach a TDD below 10^8 cm^{-2} and wafer bow of lower than 50 μm. Controlling the wafer bow is critical because high wafer bow will hamper subsequent wafer processing (especially the wafer bonding step).

InAlAs was selected as the graded buffer layer due to its relative high band-gap, 1.6 eV for $In_{0.30}Al_{0.70}As$, which is necessary to keep current leakage low in $In_{0.30}Ga_{0.70}As$ HEMTs. Among $In_xGa_{1-x}As$ HEMTs, the $In_{0.30}Ga_{0.70}As$ HEMT is a compromise between electron mobility and the break-down voltage for reliable performance,[15] especially for InGaAs HEMTs grown on Si substrates.

In this article, we report on heteroepitaxial growth of an InGaAs HEMT on a 200 mm Si substrate. It comprises a pure Ge layer, GaAs and an InAlAs compositionally graded buffer followed by the HEMT device layers. These layers were grown in the same MOCVD reactor. Phase separation is not observed in the InAlAs buffer layer and a TDD of $(1.0 \pm 0.3) \times 10^7$ cm^{-2} is obtained. An $In_{0.30}Ga_{0.70}As$ HEMT was fabricated to demonstrate the high quality of the layers. We speculate that the low TDD in the HEMT layers will improve the reliability of the III-V HEMT devices.

II. EXPERIMENTAL DETAILS

The starting substrates were 200 mm <100> orientated Si wafer with a 6° offcut towards the nearest (111) plane. Prior to the loading to the AIXTRON Crius MOCVD reactor, they were chemically cleaned by SC1 and SC2 solutions followed by an HF dip. The Si wafers were baked at 1050°C under 400 mbar of H_2 for 10 minutes to desorb any contaminants before growth. The Ge buffer layer was grown in a two-step sequence; 100 nm of Ge grown at 400°C and 800 nm Ge grown at 650°C. In order to decrease the dislocation density to 1×10^7 cm^{-2}, the wafer was subsequently annealed in-situ at 850°C and 680°C for 10 minutes each.[16]

For the III-V growth, the Ge-on-Si wafers were subjected to megasonic-cleaning in deionized water prior to their reintroduction into the growth chamber. The wafers were baked for 5 minutes at 630°C under H_2 to remove the Ge native oxide. A two-step process was used to grow the GaAs layer at 630°C to ensure an anti-phase boundary (APB) free layer[17] First, a 100 nm-thick nucleation layer was initiated with an arsine partial pressure of 5 mbar. Then the GaAs layer was grown at our regular epilayer growth conditions, namely V/III = 46, arsine partial pressure of 0.3 mbar and a TMGa flow of 96 µmol/min.

The InAlAs graded buffer was grown by keeping the V/III ratio constant at 50, maintaining a constant group-III flow of 44.8 µmol/min, and varying both the TMIn and TMAl flows linearly. The composition of the graded buffer was varied linearly from AlAs to $In_{0.30}Al_{0.70}As$ with a grading rate (20.1% In)/µm (corresponding to a strain gradient of 1.4% strain/µm). After the desired composition was reached, a 500 nm thick $In_{0.30}Al_{0.70}As$ capping layer was grown. This capping layer separates the devices layers from the misfit dislocation arrays present in the graded buffer.

The HEMT stack was grown at 630°C and was targeted to be lattice-matched to the graded buffer capping layer, and is depicted in Fig. 2. A Si δ-doping layer was deposited ~ 5 nm below the InGaAs channel. For that, the growth was stopped by switching off the group-III flow and SiH_4 was flown for 60 s into the reactor. A 15 nm thick $In_{0.30}Ga_{0.70}As$ channel was then grown, followed by an 25 nm thick $In_{0.30}Al_{0.70}As$ barrier. Lastly, an n-type doped InGaAs contact layer was grown using SiH_4 and DETe as doping sources.

The transistor structure and processing steps for long channel devices are shown in Fig. 2. Long channel devices were fabricated on a sample consisting of a 5 nm thick InAlAs barrier layer and 60 nm thick n^+ InGaAs contact layer. Adipic Acid:H_2O_2 (25:3) solution was used to etch InGaAs contact layer selectively over InAlAs in the channel region. For the gate fabrication, a high-k oxide was deposited via ALD followed by a metal gate.

III. RESULTS

A 20 µm × 20 µm AFM scan of the sample surface is shown in Fig. 3(a). The RMS roughness is 10.6 nm with a peak to valley depth of 81 nm. The micrometer scale wavelength oscillations are due to the misfit dislocation array in the graded buffer. This long range roughness is not detrimental to the performance of devices in which the active region is smaller than the roughness

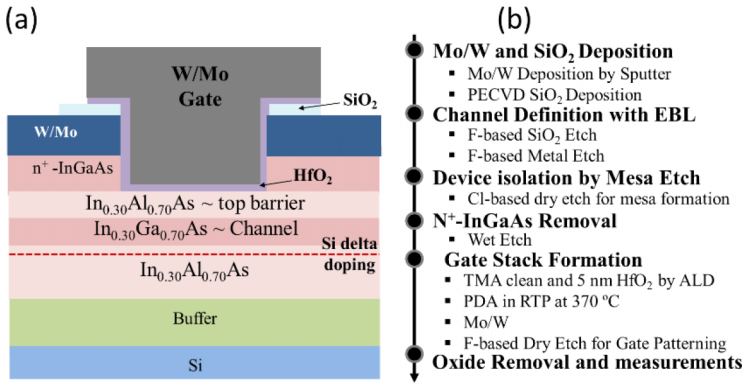

FIG. 2. (a) Simple structure and (b) process flow of the long channel $In_{0.30}Ga_{0.70}As$ HEMTgrown on 200mm Si substrate.

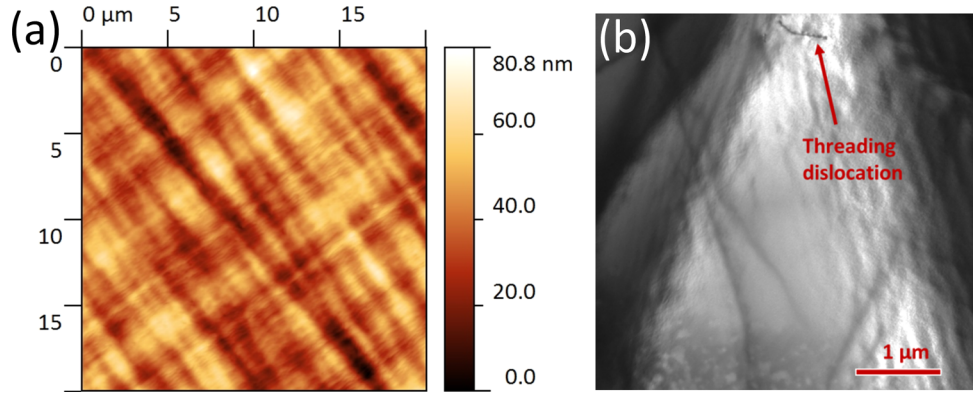

FIG. 3. (a) Surface morphology of a graded buffer sample with a final InAlAs composition of 30%. The cross-hatch pattern is visible along the <110> directions. The peak to valley depth is around 80 nm and the RMS roughness of this scan is 10.6 nm. (b) Plan-view TEM image of an InGaAs HEMT on 200 mm silicon substrate. The sample is observed under the <220> two-beam diffraction condition to 130 enhance dislocation contrast. One threading dislocation can be seen in this image. Multiple images have been analyzed to extract a threading dislocation density of $(1.0 \pm 0.3) \times 107$ cm^{-2}.

oscillation period. The sample was analyzed by plan-view TEM in order to determine the TDD. A representative image revealing a threading dislocation can be seen in Fig. 3(b), and a TDD of $(1.0 \pm 0.3) \times 10^7$ cm^2 was obtained by counting the threading dislocations present over multiple images. The error represents a 95% confidence interval assuming a Poisson distribution.

XRD reciprocal space map analysis of the sample was performed to calculate the InAlAs capping composition and strain value. The InAlAs cap layer composition was measured to be 28.9% with a 0.22% strain (in the [110] in-plane direction), corresponding to a slightly-compressively strained film that is 97% relaxed. Such high relaxation is expected when using compositionally graded buffers.

Fig. 4 shows a cross-section TEM image of the HEMT structure grown on Si. The structure can be divided into the buffer stack and the HEMT layer stack. The composite buffer with total thickness of 3 µm comprises a 0.8 µm thick Ge layer, a 200 nm thick GaAs layer, an InAlAs compositionally-graded buffer that is 1.5 µm thick and a 500 nm thick InAlAs cap layer. The HEMT layer stack – grown on top of the buffer – consists of a 15 nm InGaAs channel, a 25 nm thick InAlAs barrier layer, and a 60 nm thick n-type doped InGaAs contact layer. To supply carriers in the InGaAs channel, Si delta-doping was inserted in the InAlAs layer 3 nm below the channel. Misfit dislocations are clearly visible at the Ge/Si interface, as well as in the InAlAs graded buffer. No dislocations are visible in the InAlAs cap and in the HEMT stack, which confirms the high material quality of the HEMT device stack.

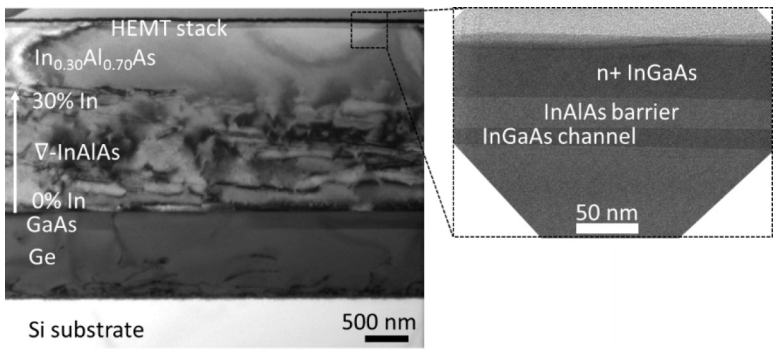

FIG. 4. Cross section TEM image of an InGaAs HEMT grown on a 200 mm silicon substrate. The 3 µm composite buffer is composed of a Ge layer, a GaAs layer and a composition graded InAlAs buffer, capped with a 500 nm thick InAlAs cap. Misfit dislocations are visible in the graded buffer and at the Ge/Si interface. In the HEMT stack, no threading dislocations are observed, indicative of good device material quality. The right inset shows the cross-section TEM image of the HEMT device layers.

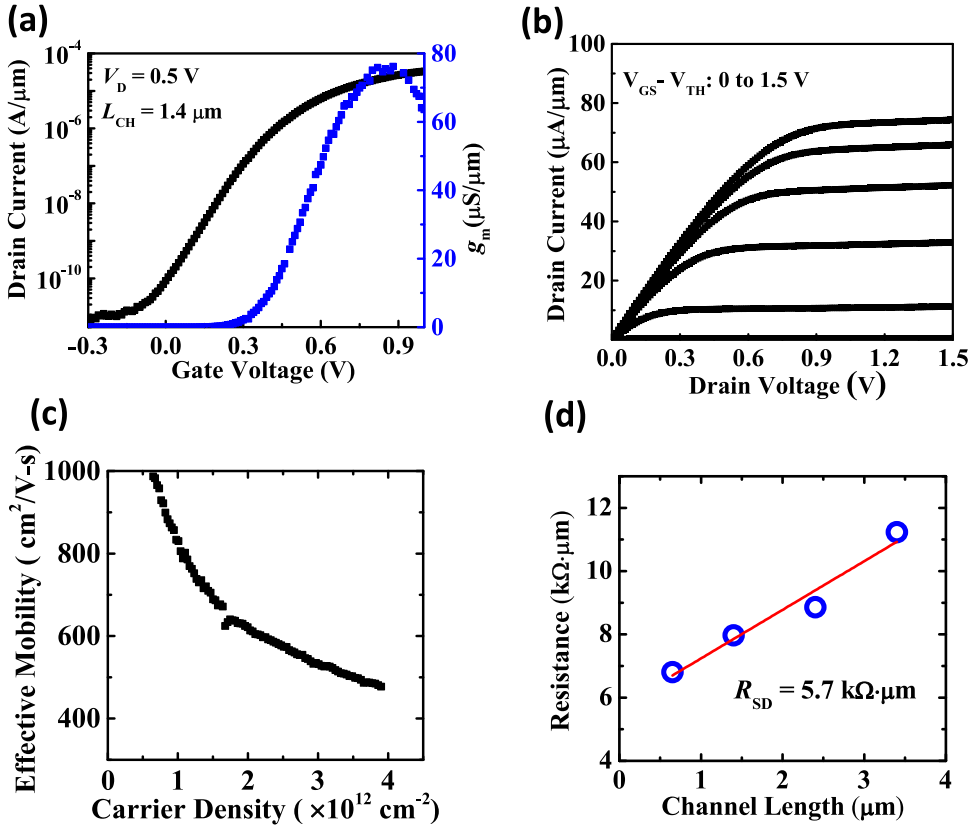

FIG. 5. (a) I_d-V_{gs} and g_m-V_{gs} of a 1.4 μm long channel $In_{0.30}Ga_{0.70}As$ MOS-HEMT. (b) I_d-V_{ds} curves of the same device show on-current exceeding 70 uA/um at V_{gs}-V_{th} = V_{ds}= 1.5 V. (c) Field-effective mobility as a function of the carrier density in the channel. A peak device mobility of ~ 1000 cm^2/V.s was extracted. (d) External device resistance as a function of the channel length. A total source-drain resistance of 5.7 kΩ·μm was extracted.

Hall Effect measurements were conducted in various areas of the 200 mm wafer to characterize the HEMT uniformity. The electron mobility in the 2-dimentional electron gas (2 DEG) varied from 4900 to 5440 cm^2/Vs with a sheet carrier density in the range of (1-2) × 10^{12} cm^{-2}. This non-uniformity can be improved by a proper temperature tuning over the wafer during the growth. The wafer bow is 35 μm which is sufficiently low for subsequent wafer bonding processes.

The electrical characteristics of a 1.4 μm long channel MOS-HEMT fabricated from a similar wafer with a 5 nm thick InAlAs top barrier is shown in Fig. 5. I_D-V_{gs} curve of Fig. 5(a) shows high I_{ON}/I_{OFF} ratio of larger than 5 orders with low off-state leakage current. Minimum subthreshold swing for the same device is ~ 85 mV/decade indicating good electrostatic control and gate stack quality. The peak g_m is above 70 μS/μm at V_{ds} of 0.5 V [Fig. 5(a)]. The drain current exceeds 70 μA/μm at the V_{ds} of 1.0 V and V_{gs} of 1.5 V. A peak device mobility of ~1000 cm^2/V.s was extracted from the split CV and I_D-V_{gs} measurement data. The effective mobility is lower than that of previously reported $In_{0.53}Ga_{0.47}As$ channel devices.[18,19] The relatively low drive current is also due to the larger source-drain series resistance (R_{SD} ~ 5.7 kΩ · μm) in our devices. This large series resistance is mainly due to the large energy barrier of ~ 0.7 eV between InAlAs/InGaAs in the contact region. The reported performance demonstrates the high quality of the HEMT stack material grown on Si, and further optimization of device structure and processing is expected to yield better performance.

IV. CONCLUSION

We have reported on the heteroepitaxial growth of an $In_{0.30}Ga_{0.70}As$ HEMT on 200 mm silicon substrate. Long-channel HEMTs were fabricated from the material using CMOS-compatible

processing. By using a buffer layer stack comprising Ge, GaAs and InAlAs graded buffer, a TDD of $(1.0 \pm 0.3) \times 10^7$ cm^2 was achieved. Long-channel HEMT devices with good electrical properties were demonstrated, suggesting that the graded buffer approach is promising for low power and high-frequency analog devices grown on silicon.

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