Advances in RNMC Technique with Dual-Active Current and Voltage Buffer for High-Load Three-Stage Amplifiers

J. Sobhi                                   ZD.Koozehkanani                 A.Ghardashkhani
University of Tabriz. ECE faculty, IC design research lab.
Tabriz-Iran
sobhi@tabriz.ac.ir                       Zdaie@tabriz.ac.ir              aghardashkhani@gmail.com

Abstract

— This paper presents a novel compensation technique for low voltage low power three-stage amplifier driving large capacitive loads. The frequency bandwidth of this amplifier is improved due to usage of dual-active buffers in the efficient compensation network while a feed forward transconductance helps to enhance output large signal response. The paper provides a design procedure by developing the mathematical and analytical insight for the compensation network elements using phase margin as the main design parameter. The circuit level simulation for the proposed amplifier with a 0.35μm standard CMOS process resulted 6.7MHz unity gain bandwidth and 67 degree phase margin while driving 1-nF load from a single 2V power supply.

Introduction

Operational amplifier is the building block of analog and mixed signal circuits. These circuits increasingly demand low voltage power supply, high dc gain, wide frequency band-width amplifiers which are able to drive large capacitive loads. increasing demand in low-power portable electronic devices and the downscaling in technology, the conventional single-stage cascode amplifiers are not capable to deliver both high dc gain and large output signal swing. In order to avoid cascoding stages, dc gain in excess of 100db is achieved by cascading three or more, simple transconductance gain stages. However multi-stage amplifiers suffer from closed-loop stability problem due to the presence of multiple frequency poles and zeroes which require additional compensation capacitors to provide adequate closed loop stability.

Nested miller compensation (NMC) is a well known compensation technique for the multi stage amplifier. It employs miller capacitor to split the poles so that the non-dominant poles can be located higher than unity-gain frequency .although such nested miller amplifiers provide good stability they lead to enormous power consumption and reduced gain-bandwidth product. To overcome the limitations of NMC, especially when driving heavy capacitive loads, the reversed nested miller compensation (RNMC) is proposed [1]. The RNMC amplifier usually has higher bandwidths than the nested miller one since in the RNM amplifier the inner compensation capacitor does not load the amplifier's output.

The RNMC scheme has the stability problem because of appearing a right half plane (RHP) zero in its frequency response, to alleviate this problem several RNMC variants have been reported [7][13]

In this paper a novel frequency compensation technique witch uses active buffers to move RHP-zero to the left half plane and an analytical insight and mathematical analysis is presented. This paper is organized as follows ,the operating principle and the small signal analysis and mathematical analysis of the proposed amplifier are discussed in section II, section III and section IV show the detailed circuit implementation and measurement results respectively, finally a conclusion is given in section V.

Proposed Compensation Technique

A. Small signal and mathematical analysis

The block diagram of the proposed topology is shown in fig.1.A conventional three stage amplifier consist of three transconductance stages $g_{m1} - g_{m3}$. Parameter $r_{oi}$ and $c_i (i =1−3)$ represent the output resistance and the lumped parasitic capacitance of $i_{th}$ stage. The compensation network includes the two miller capacitors.
The current buffer $A_c$ with its input resistance $r_c$, and the voltage buffer $A_v$, with its output resistance $r_v$. The feed forward stage $g_{nf}$ along with $g_m$ forms the output push pull stage to improve large signal performance without extra power dissipation. Fig. 2 shows the small signal equivalent circuit of Fig.1 [5], where $c_1, c_2, c_3$ and $r_1, r_2, r_3$ are the total capacitance and resistances seen at node 1, 2, and output respectively. By solving open loop small signal equations and performing some routine analysis, the small signal transfer function can be driven and simplified [5].

Assuming $c_1, c_2, c_3, g_1, g_2, g_3$ are the total capacitance and resistances seen at node 1, 2, and output respectively, the open loop transfer function is expressed by

$$A(s) = \frac{V_{out}}{V_{in}} = -A_{dc} \left( \frac{b_2 s^2 + b_1 s + b_0}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} \right)$$  \hspace{1cm} (1)

$$a_0 = (g_{mc} r_{oc} + 1) = g_{mc} r_{oc}$$

$$a_1 = c_1 g_m g_2 g_m g_3 g_{mc} r_{12} r_{23} r_{2} r_{oc}$$

$$a_2 = g_{mc} g_m^2 g_{mc} r_{oc} r_{12} c_{c1} (c_0 + c_1 (r_1 g_m + g_{mc}/g_m))$$

$$a_3 = c_{c1} c_{c2} c_{oc} r_{oc} (c_0 + c_1 (r_1 g_m + g_{mc}/g_m))$$

$$b_0 = -g_{mc} r_{oc} r_v$$

$$b_1 = -c_1 g_{mc} r_{oc} r_v$$

$$b_2 = c_1 c_2 g_{mc} r_{oc} r_v (r_1 + r_{oc})$$

With assumption that $p_1 \gg p_2, p_3$ the dominant pole [2]

$$p_1 = \frac{-a_0}{a_1} = -\frac{1}{c_{c1} g_m g_2 g_m g_3 r_{23} r_{2} r_{oc}}$$  \hspace{1cm} (2)

As a result

$$\omega_{GBW} = 2\pi f_{GBW} = \left| A(s) \right|_{s=0} = \left| A_{dc} \right| = \frac{g_{mc}}{c_{c1}}$$  \hspace{1cm} (3)

And for $s \gg p_1$, the denominator of transfer function $D(s)$, can be approximated as

$$D_s = \left( 1 - \frac{s}{p_1} \right) \left( 1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2 \right)$$  \hspace{1cm} (4)

Therefore, approximate values of the poles $p_2$ and $p_3$ are the roots of (4), these poles can be real or complex; they will be real and widely spaced if

$$\left( \frac{a_2}{a_1} \right)^2 \gg \left( \frac{a_3}{a_1} \right)$$  \hspace{1cm} [1].

This condition can be satisfied when

$$g_{mc} \gg \frac{c_{c1}^2 c_{c2}}{c_0 c_1 g_m^2 g_m g_3 r_{23} r_{oc}}$$  \hspace{1cm} (5)

As a result the proposed compensation technique does not lead to any specific design constraint or matching condition on the $g_m$ and $g_{mc}$, which can be kept reasonably small, thus saving on power and area consumption. The non dominant poles are given by:

$$p_2 = -\frac{a_1}{a_2} = -\frac{c_{c1} g_m}{c_{c2} (c_0 + c_{c1} (1 + g_{mc} r_v))}$$  \hspace{1cm} (6)

$$p_3 = -\frac{a_3}{a_2} = -\frac{g_m^2 g_{mc} r_{oc}}{c_{c1} r_v}$$  \hspace{1cm} (7)

And high frequency zeros are given by

$$Z_{LHP,RHP} =$$

$$d (5b_{12} b_{24} c_{c1} c_{c2} g_{mc} r_{oc} r_v)$$

$$\pm \sqrt{\frac{12 c_{c1} c_{c2} r_v}{d}}$$  \hspace{1cm} (8)

With $b = c_{c2} g_{mc} r_{oc} r_v$

$$d = 5 g_2 g_m^2 g_m^3 r_2$$

The RHP zero locates at very high frequency and the LHP zero locates at

$$Z_{LHP} = -\frac{1}{c_{c2} r_v} = -\frac{g_{mc}}{c_{c2}}$$  \hspace{1cm} (9)

The phase margin is given by
\[ PM = 180 - \tan^{-1}\left(\frac{\alpha_{GBW}}{p}\right) - \tan^{-1}\left(\frac{\alpha_{GBW}}{p^2}\right) + \tan^{-1}\left(\frac{\alpha_{GBW}}{Z_{LHP}}\right) \tag{10} \]

As a result
\[ PM = \tan^{-1}\left(\frac{|p|}{\alpha_{GBW}}\right) \]
\[ \tan^{-1}\left(\frac{c_{rl}^2 g_{m3}}{g_{m1} c_{c2} (c_a + c_{c1} [1 + g_{m3} r])}\right) \tag{11} \]

And for large capacitive loads
\[ PM = \tan^{-1}\left(\frac{c_{rl}^2 g_{m3}}{c_{c2}^2 g_{m1}}\right) \tag{12} \]

As a result using (3), (12) for a given load capacitance, closed loop bandwidth and phase margin values, parameters \( c_{rl}, c_{rl} \) can be estimated.

B. Estimation with Matlab

To estimate the system parameters efficiently the output to input symbolic transfer function has been solved with the assistance of Matlab symbolic analysis tool. As shown in Fig. 3, by substituting real values of symbolic parameters the frequency response, settling behavior, pole/zero locations and root locus of proposed amplifier is plotted by Matlab.

Circuit Implementation

To prove the effectiveness of the proposed compensation technique and show its advantages over other previously reported solutions especially with [8], HSPICE simulations are carried out using standard 0.35\( \mu \)m CMOS technology. The amplifier was designed to achieve a dc gain of about 110db and phase margin of 70° with capacitive load of 1nF and 2-V power supply.

The schematic of three stage amplifier with proposed compensation technique is shown in Figure. 4. First stage composed of M1-M8 is a classical folded cascade OTA. A common source amplifier M9-M10 is adopted as a second stage. The last non inverting stage is implemented by the transistors M11-M14, providing a sign conversion through the current mirror M12-M13. To attain fast time domain response transistor M14 acts as the feed forward stage \( g_{mf} \) [3].

The load capacitance \( c_l \) is taken to be 1nF and the unity gain frequency is set at about 6MHz and the phase margin about 70°. The value of designed circuit parameters of proposed amplifier is shown in Table I. To achieve the target gain-bandwidth product of 6 MHz, we set
\[ g_{m1} = g_{m2} = 95 \ \mu A/V, \ g_{m3} = 150 \ \mu A/V, \ g_{mf} = 280 \ \mu A/V, \ g_{mc} = 180 \ \mu A/V, \ g_{mv} = 105 \ \mu A/V, c_{c1} = 6pF, c_{c2} = 0.02pF. \]

The drain current of M1-M2 is set to 5 \( \mu A \), the drain current of second stage is set to 5.5 \( \mu A \), while the current of last stage is set to 20 \( \mu A \). The current of common drain voltage buffer is set to 3 \( \mu A \). As a result the total DC current consumption is 73 \( \mu A \), and the static power consumption is 146 \( \mu W \). Transistor dimensions are reported in Table I.

\[ \text{Figure 3. Estimation with Matlab} \]

\[ \text{Figure 4. Schematic of three stage open-loop amplifier employing the proposed compensation technique} \]
5 shows the simulated open-loop frequency response of the proposed amplifier. The large signal transient response of the amplifier in unity gain negative feedback configuration is shown in figure 6. The dc gain was 110dB, the gain-bandwidth product was 6.7MHz with phase margin of 67°. Positive and negative slew rates are found to be 0.88 V/μs and 1.08V/μs respectively. Positive and negative settling times, within 1% of the final output are 0.80 μs and 0.69 μs respectively. Table II summarizes the simulation results of the proposed amplifier. Two more precise FOMs were proposed in [4]

\[ IFOM_s = \frac{\omega_{GBW} C_L}{I_{dd}} \]  \hspace{1cm} (13) 

\[ IFOM_L = \frac{SR C_L}{I_{dd}} \]  \hspace{1cm} (14)

using these formulas, a performance comparison with other multistage amplifier topologies is reported in Table- III. It is clear that proposed compensation technique shows an improvement in small signal performance. For better comparison the transistors dimensions are set to be the same as transistor dimensions in [8], and only compensation network is modified with no extra power consumption, as result the better performance of proposed amplifier is clearly shown.

**Conclusion**

In this paper, a new compensation technique for three stage amplifier with large capacitive load is presented. The solution exploits active voltage and current buffers in an efficient topology along with a feed forward stage enhancing large signal performance. The mathematical symbolic analysis is presented to precisely analyzing the system. The proposed compensation technique achieves the largest IFOMs compared to the other previously reported compensation topologies.

**References**


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<th>Compensation Technique</th>
<th>$C_L$ (pF)</th>
<th>$C_{C1}$ (pF)</th>
<th>$C_{C2}$ (pF)</th>
<th>$V_{DD}$ (V)</th>
<th>$I_{DD}$ (mA)</th>
<th>Power (mW)</th>
<th>$f_{GBW}$ (MHz)</th>
<th>SR (V/μs)</th>
<th>IFOM $^S$ (MHz pF/mA)</th>
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