13th IEEE Latin American Test Workshop
PRELIMINARY TECHNICAL PROGRAM

Wednesday, April 11th 2012

08:30 – 09:00  TTEP Tutorials and LATW Registration

9:00 – 09:20  LATW Opening Session

9:20 – 10:10  Invited Talk
Title: On-Chip Structures for Parametric Test
Presenter: Jacob Abraham

10:10 – 10:40  Coffee break

10:40 – 11:40  SESSION 1: Fault Analysis, Simulation and Diagnosis

Built-in Self-Diagnosis Targeting Arbitrary Defects with Partial Pseudo-Exhaustive Test, Alejandro Cook, Sybille Hellebrand, Michael Imhof, Abdullah Mumtaz, Hans-Joachim Wunderlich

Simulation of SET Faults in a Voltage Controlled Oscillator
Walter Calienesbartra, Fernanda Kastensmidt, Ricardo Reis

Low Voltage Testing for Interconnect Opens under Process Variations
Jesus Moreno, Victor Champac, Michel Renovell

11:40 – 12:40  SESSION 2: Design and Synthesis for Testability

IEEE STD 1149.1 basics and advance topics,
Francisco Russi

PSL Assertion Checkers Synthesis with ASM Based HLS tool ABELITE
Maksim Jenihhin, Samary Baranov, Jaan Raik, Valentin Tihhomirov

Retiming Scan Circuit to Eliminate Timing Penalty
Ozgur Sinanoglu, Vishwani Agrawal

12:40 – 14:00  Lunch and TTEP registrations
14:00 – 15:30  Test Technology Educational Program (TTEP)

TTEP 1: Statistical Adaptive Test Methods Targeting "Zero Defect" IC Quality and Reliability
Presenter: Adit D. Singh, Auburn University, USA
Email: adsingh@auburn.edu

15:30 – 16:00  Coffee break

16:00 – 17:30 Test Technology Educational Program (TTEP)

TTEP 2: Design for Yield and Reliability
Presenter: Yervant Zorian, Synopsys, USA
Email: Yervant.Zorian@synopsys.com

20:30 – 22:00  Welcome Reception

Thursday, April 12th

09:00 – 09:30  Invited talk
Title: Designing RFID Chips for Test & Security: Towards a Reliable Internet of Things
Presenter: Marcelo Lubaszewski

09:30 – 10:30  SESSION 3: Design Verification and Validation
Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis
Hanno Hantson, Urmas Repinski, Jaan Raik, Maksim Jenihhin, Raimund Ubar
A Guiding Heuristic for the Semi-Formal Verification of High-Level Designs
Alair Dias Junior, Diógenes Silva Junior
Manipulation of Training Sets for Improving Data Mining Coverage-Driven Verification
Edgar Romero, Marius Strum, Jiang Chau Wang

10:30 – 11:00  Coffee break
11:00 – 12:00  SESSION 4: Design Optimization

Self-Optimization of Dense Wireless Sensor Networks based on Simulated Annealing
Alex Roschildt Pinto, Adriano Cansian, José Machado, Carlos Montez

Design-for-manufacturability of MEMS convective accelerometers through adaptive electrical calibration strategy
Florence Azais, Ahmed Rekik, Frederick Mailly, Pascal Nouet

12:00 – 13:00  SESSION 5: Product Quality and Software Testing

Investigating the Use of An On-Chip Sensor to Monitor NBTI Effect in SRAM
Ceratti, T. Copetti, L. Bolzani, F. Vargas

Parametric DC and Noise Measurements for a Unified Production Line Characterization Framework Software Tool
Manuel Jimenez-Cedeno, William Morales, Lucianne Millan, Jose Rodriguez, Rogelio Palomera, Frank Hou

Mutation Operators for Concurrent Programs in MPI
Rodolfo Silva, Simone Souza, Paulo Souza

13h00 – 14:00  Lunch Break

14:00 – 15:00  SESSION 6: Automatic Test Generation

Automatic generation of an FPGA based embedded test system for printed circuit board testing
Jorge Hernan Meza Escobar, Jörg Sachsse, Steffen Ostendorff, Heinz-Dietrich Wuttke

Platform for Automated HW/SW Co-verification, Testing and Simulation of Microprocessors
Aleksandar Simevski, Rolf Kraemer, Milos Krstic

About Robustness of Test Patterns Regarding Multiple Faults
Raimund Ubar, Sergei Kostin, Jaan Rai

15:00 – 16:00  SPECIAL SESSION 1

Power- and Thermal-Aware Modelling and Design
Organizer: Jose Ayala, Complutense University of Madrid, Spain

Model-Based Design for Wireless Body Sensor Network Nodes
Ivan Beretta, Francisco Rincon, Nadia Khaled, Paolo Roberto Grassi, Vincenzo Rana, David Atienza, Donatella Sciuto
Fast and Scalable Temperature-driven Floorplan Design in 3D MPSoCs
Ignacio Arnaldo, Alessandro Vicenzi, Jose L. Ayala, Jose L. Risco, J. Ignacio Hidalgo, Martino Ruggiero, David Atienza

Fast Worst-Case Peak Temperature Evaluation for Real-Time Applications on Multi-Core Systems
Lars Schor, Iuliana Bacivarov, Hoeseok Yang, Lothar Thiele

16:00 – 16:30 Coffee break

16:30 – 17:30 SESSION 7: Analog and Mixed Signal Circuits
Built-in Tuning of RFIC Passive Polyphase Filter by Process and Thermal Monitoring
Fayrouz Haddad, Wenceslas Rahajandraibe, Hassen Aziza, Karine Castellani-Coulie, Jean Michel Portal

Multi-condition alternate test of analog, mixed-signal, and RF systems
Manuel Barragan, Gildas Leger, Jose Luis Huertas

Real-Time Built-in Self-Test of $\Sigma$-$\Delta$ A/D Converters
Drago Strle

20:00 – 23:00 Gala Dinner

Friday, April 13th

09:00 – 09:30 Invited talk
Title: TBD
Presenter: Vishwani Agrawal

09:30 – 10:30 SPECIAL SESSION 2

Thermal Aware Design and Test
Organizer: Marta Rencz, Technical University of Budapest, Hungary

Thermal-aware aging prognosis based on NBTI models
Sven Rosinger

Acquiring real-time heating of cells in standard cell designs
Andras Timar, Marta Rencz
Simulation Framework for Multilevel Power Estimation and Timing Analysis of Digital Systems Allowing the Consideration of Thermal Effects
Gergely Nagy, András Poppe

10:30 – 11:00 Coffee break

11:00 – 12:00 SPECIAL SESSION 3
Robust and Testable Designs in the Nano-Regime
Organizer: Kaushik Roy, Purdue University, USA

Low-Power Design under variation using error prevention and error tolerance
Kwanyeob Chae, Saibal Mukhopadhayay

Variation-aware and self–healing design methodology for a system-on-chip
Jangjoon Lee, Srikar Bhaggavatula, Kaushik Roy, Byunghoo Jung

12:00 – 13:00 SESSION 8: Harsh Environments: Radiation and EMI
Investigation of a CMOS Oscillator Concept for Particle Detection and Diagnosis
Karine Castellani-Coulie, Hassen Aziza, Wenceslas Rahajandraibe, Gilles Micolau, Jean Michel Portal

SITARe: a Simulation Tool for Analysis and diagnosis of Radiation Effects
Gilles Micolau, Karine Castellani-Coulie, Hassen Aziza, Jean Michel Portal

Impact of TID-induced Threshold Deviations in Analog Building-blocks of Operational Amplifiers
Guilherme Cardoso, Tiago Balen, Rafael Vaz, Marcelo Lubaszewski, Odair Gonçalvez

13:00 – 14:00 Lunch

14:00 – 15:00 SESSION 9: Dealing with Radiation Effects: SEUs and SETs
SET Susceptibility Estimation of Clock Tree Networks from Layout Extraction
Raul Chipana, Fernanda Kastensmidt, Ricardo Reis

Applying Adaptive Temporal Filtering for SET Mitigation based on the Propagation-Delay of Every Logical Path
Jose Eduardo Souza, Fernanda Kastensmidt

SEU fault-injection in VHDL-based processors: a case study
Wassim Mansour, Raoul Velazco
15:00 – 16:00  **SESSION 10: Software Fault Tolerance**

Configurable Tool to Protect Processors against SEE by Software-based Detection Techniques  
Eduardo Chielle, Raul Barth, Angelo Lapolli, Fernanda Kastensmidt

MoDiVHA: A Hierarchical Strategy for Distributed Test Assignment  
Jefferson Koppe, Luis Bona, Elias Duarte Junior

Detailed Analysis of Compilation Options for Robust Software-based Embedded Systems  
Antoine Wecxsteen, Salma Bergaoui, Regis Leveugle

16:00– 16:30  **Coffee Break**

16:30 – 17:30  **SESSION 11 Fault-Tolerant Architectures**

Selective Hardening Methodology for Combinational Logic  
Samuel Pagliarini, Gutemberg Junior, Lirida Naviner, Jean-François Naviner

Pattern-based Injections in Processors Implemented on SRAM-based FPGAs  
Mohamed Ben Jrad, Regis Leveugle

Non-intrusive fault tolerance in soft processors through circuit duplication  
Felipe Silva, Frederico Ferlini, Eduardo Bezerra, Djones Lettnin

17:30 – 17:50  **Closing Remarks**

Saturday, April 14th

**Departure to Galapagos**

Monday, April 16th

19:00 – 20:00  **PANEL SESSION: Challenges of advanced nanotechnologies to test development. Panelists TBD**