Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime

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Abstract

Thin-body transistors with silicide source/drains were fabricated with gate-lengths down to 15nm. Complementary low-barrier silicides were used to reduce contact and series resistance. Minimum gate-length transistors with T_{ox}=40Å show PMOS $|I_{dsat}|$=270μA/μm and NMOS $|I_{dsat}|$=190μA/μm with V_{ds}=1.5V, $|V_g-V_t|$=1.2V and, $I_{on}/I_{off}>10^4$. A simple transmission model, fitted to experimental data, is used to investigate effects of oxide scaling and extension doping.

Introduction

The single[1] and double[2] gate thin-body transistors are promising device designs for the 5-50nm gate-length regime. One of their major challenges is the large series resistance of the thin body layer. In this paper we present a method for reducing this resistance with the use of dual low-barrier silicide source/drains: PtSi for PMOS, and $ErSi_{1.7}$ for NMOS, **Fig. 1**. In previous studies, bulk-Si silicide source/drain MOSFETs[3] have exhibited large leakage currents. Our use of a thin body reduces leakage by orders of magnitude. This symbiotic relationship between leakage suppression by the thin-body structure and the low series resistance of the silicide source/drain structure results in a promising device technology that can be scaled down to 15nm gate-length. It also provides an alternative to the elevated source/drain approach as a general method for reducing series resistance of thin-body designs.

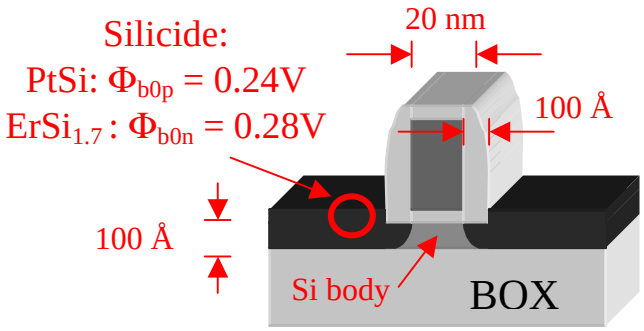


Figure 1: The thin-body silicide source/drain MOSFET in cross section. Source/drains are made in 100Å Si: NMOS uses $ErSi_{1.7}$ (Φ_{b0n}=0.28V), PMOS uses PtSi (Φ_{b0p}=0.24V). Spacer thickness is limited to 100Å, in order to guarantee that the metal diffuses underneath the gate.

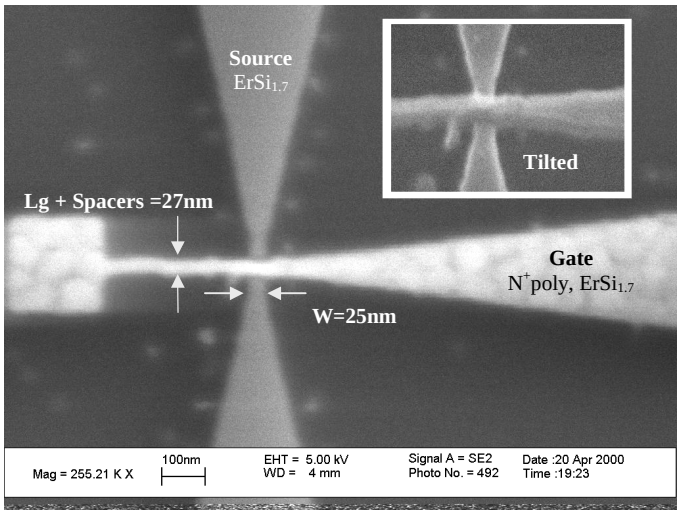
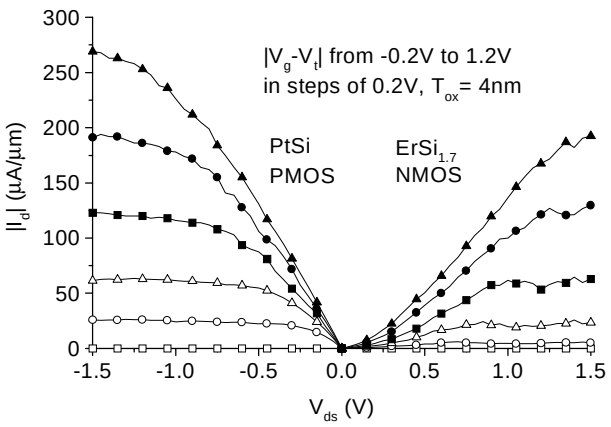


Figure 2: SEM image of an $ErSi_{1.7}$ device with a polysilicon gate length of 15nm and two 6nm SiO_2 spacers. Device width is 25nm.

Device Fabrication

A lightly doped (N_a=1E15 cm^{-3}), 100nm thick, silicon on insulator (SOI) film was thinned to 140Å using a two step thermal oxidation. The mesa was defined using a calixarene/G-line double exposure process. Optical exposure of coarse features in G-line resist was followed by 100keV e-beam lithography of fine features in calixarene resist and a dry etch. The gate stack consisted of a 40Å thermal gate oxide, a 550Å *in-situ* doped N-type polysilicon gate, and a 150Å deposited SiO_2 hard mask. Gate lithography also involved a calixarene/G-line double exposure process aligned to the previous layer using SiGe alignment marks. Following gate formation, 100Å SiO_2 spacers were formed. A HF-last clean was performed just prior to metal deposition, and SOI thickness was measured to be 85~100Å. PMOS devices received 75Å of Pt evaporated in an e-beam evaporator. PtSi was formed with a 400°C 1h anneal in a N_2 ambient. Unreacted Pt was then removed in a dilute Aqua Regia etch. NMOS devices received 70Å of Er evaporated in a UHV e-beam evaporator with the base pressure of the oxidizing ambient kept below 10^{-10} torr. $ErSi_{1.7}$ was formed using a 400°C 1h UHV anneal, and unreacted Er was then removed in a dilute nitric acid etch. **Fig. 2** shows an NMOS device with L_g=15nm. Neither NMOS nor PMOS devices used any significant doping in the source, drain, or body.



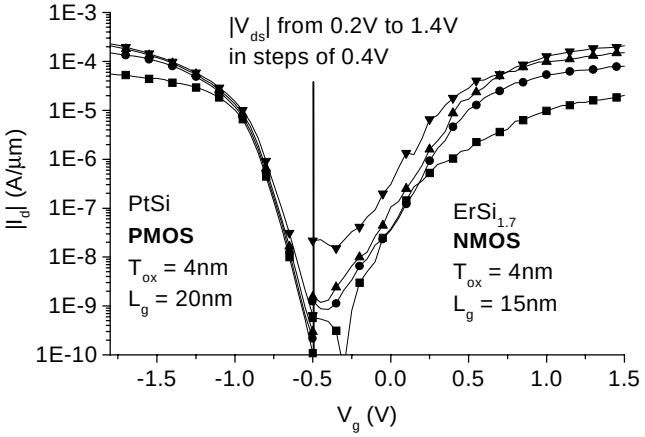


Figure 3,4: I-V characteristics of the minimum gate-length devices. For the **PMOS transistor, L=20nm**, $|I_{dsat}|$=270μA/μm at V_{ds}=1.5V and $|V_g-V_t|$=1.2V. Swing is 100mV/dec, I_{on}/I_{off}=5E5, and V_t = –0.7V. For the **NMOS transistor, L=15nm**, $|I_{dsat}|$=190μA/μm at V_{ds}=1.5V and $|V_g-V_t|$=1.2V. Swing is 150mV/dec, I_{on}/I_{off}=1E4, and V_t =–0.1V.

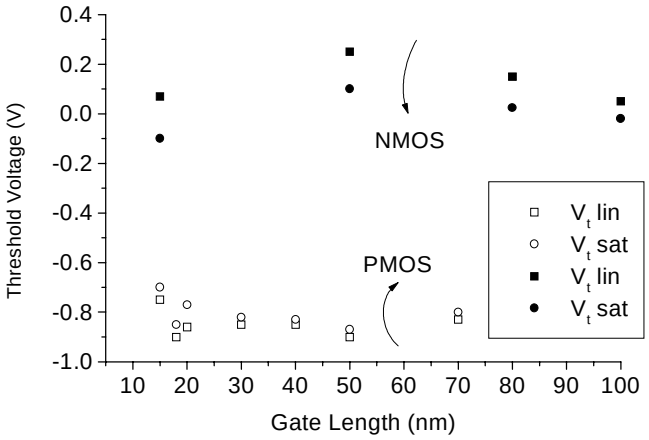


Figure 5: Linear and saturation threshold voltages as a function of gate length for both NMOS and PMOS.

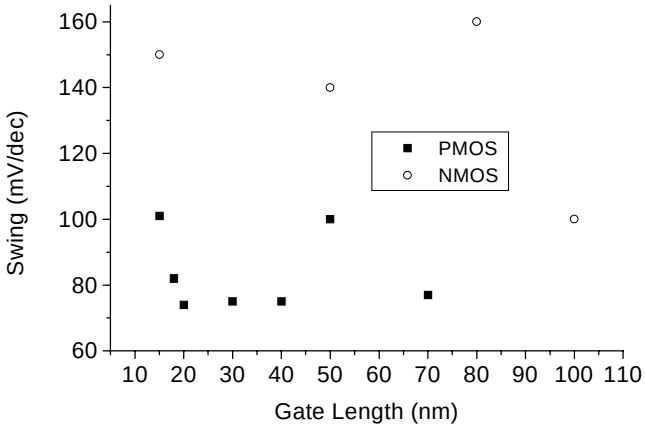


Figure 6: Swing dependence on gate length. For PMOS devices S=75mV/dec down to 20nm gate lengths. NMOS devices show a larger variation in swing with S=100-160mV/dec.

Device Characterization

Fig. 3,4 show the I-V characteristics of the minimum gate-length transistors. The PtSi PMOS transistor has a 20nm gate length, and $|I_{dsat}|$=270μA/μm with T_{ox}=40Å at $|V_{ds}|$=1.5V. Sub-threshold characteristics show excellent short-channel effects, and a V_t of –0.7V. The abnormally high V_t is due to the N^+poly gate, it can be reduced using a mid-gap gate material such as P^+SiGe[4]. The $ErSi_{1.7}$ NMOS transistor has a 15nm gate length, $|I_{dsat}|$=190μA/μm at $|V_{ds}|$=1.5V. The lower NMOS I_{dsat} is due to the higher $ErSi_{1.7}$ barrier of 0.28V. Still, this is the lowest flat-band NMOS barrier achieved for a silicide. NMOS sub-threshold characteristics show a swing of 150mV/dec, and a V_t of –0.1V, which can be adjusted to a higher value with the use of a mid-gap gate. The presence of the Schottky barrier can be seen in the exponential behavior of the I_d-V_d plot for the NMOS devices at low V_{ds}. The gate-length dependencies of the threshold voltages and swing characteristics are shown in **Fig. 5,6** respectively. PMOS devices show excellent short channel characteristics down to 15nm gate-length, with ΔV_t = 0.2V and S=100mV/dec. NMOS devices show a similar ΔV_t = 0.2V, but worse DIBL and S=150mV/dec. Since the swing and DIBL don't show a strong dependence on gate-length, they are probably determined by the silicon/silicide interface trap density. Annealing devices at 500°C decreases interface trap density but increases the barrier to 0.32V, **Fig. 7**. Long channel V_t values are –0.85V for PMOS, and 0.05V for

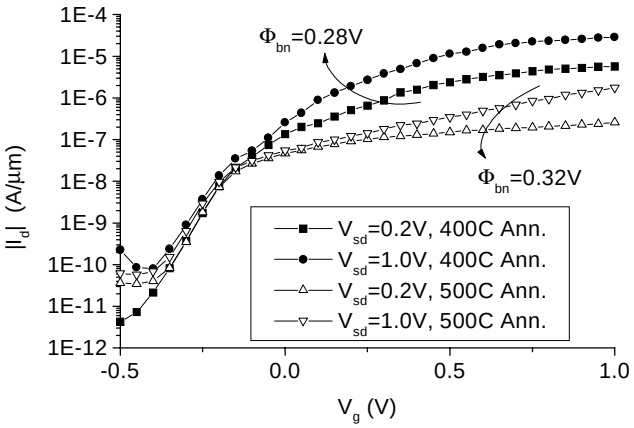


Figure 7: Id-Vg of a long channel $ErSi_{1.7}$ NMOS device before and after a 500°C anneal. Silicidation temperature is 400°C.

NMOS. These V_t values are similar to what would be expected for conventional thin-body transistors with N^+poly gate, indicating that the low Schottky barrier doesn't inhibit current flow at threshold. The threshold data also shows that with the use of a single gate of appropriate mid-gap work-function the $|V_t|$ can be adjusted to 0.45V. While this value may be acceptable for low-power applications, it is too high for high-performance logic.

Transmission Model

As the silicide source/drain device turns on, it passes through the source-body flat-band condition, $V_g=V_{sbfb}$. This transition can be seen clearly in long channel $ErSi_{1.7}$ devices, **Fig. 8**. For gate biases below V_{sbfb}, the Si body blocks the current flow; above V_{sbfb}, the Schottky barrier is the dominant current barrier. Below V_{sbfb} S is determined by the body potential and is ideally 60mV/dec; above the V_{sbfb}, S is determined by effective-barrier lowering mechanisms such as tunneling and image charge induction. The effective Schottky barrier, Φ_b , can be expressed as:

$$\Phi_b = \Phi_{b0} - \Delta\Phi_t - \Delta\Phi_i$$

where $\Delta\Phi_t$ and $\Delta\Phi_i$ are contributions from tunneling and image charge induction respectively, and Φ_{b0} is the source-body flat-band barrier height. Both of these lowering mechanisms depend on the lateral electric field E_y, which is proportional to the gate voltage through T_{ox} and a geometric factor G:

$$\Delta\Phi_t = \frac{1}{e}\left(\frac{3e\hbar(\ln 2)}{4\sqrt{2m^*}}\right)^{2/3}(E_y)^{2/3} \qquad E_y = \frac{GV_g^*}{t_{ox}}$$

with

$$\Delta\Phi_i = \left(\frac{e}{4\pi\varepsilon_s}\right)^{1/2}(E_y)^{1/2} \qquad V_g^* = |V_g - V_{sbfb}|$$

In the subthreshold region G is an electrostatically determined constant. However, in strong inversion G decreases due to the screening of the gate field by inversion charge. Two-dimensional simulations indicate that for our structure G ~0.25 in the subthreshold region and drops to ~0.1 in strong inversion. With a simple transmission model the Φ_b can be translated into I_d, **Fig 9**. Our model assumes that at Φ_b=0, $I_{dsat}=I_{dBAL}$, the ballistic current limit[5], and employs Boltzmann statistics, which give the 60mV/dec conversion between Φ_b and I_{dsat}.

Analysis/Discussion

Using the gate work-function, G, and Φ_{b0} as fitting parameters, a fit with the data is obtained, **Fig. 10**. In PMOS devices Φ_{b0p}=0.22V, slightly lower then the expected 0.24V; in NMOS devices Φ_{b0n}=0.28V, the reported value for $ErSi_{1.7}$[6]. **Fig. 10** also indicates that for $ErSi_{1.7}$ Φ_{b0n} changes from around 0.32V to 0.28V as the electric field at the interface is increased. This suggests the presence of donor states, or donor-like interface traps, at the silicide interface. With the states occupied by an electron the Φ_{b0n} =0.32V, and as the electrons are removed by the gate field Φ_{b0n} changes to

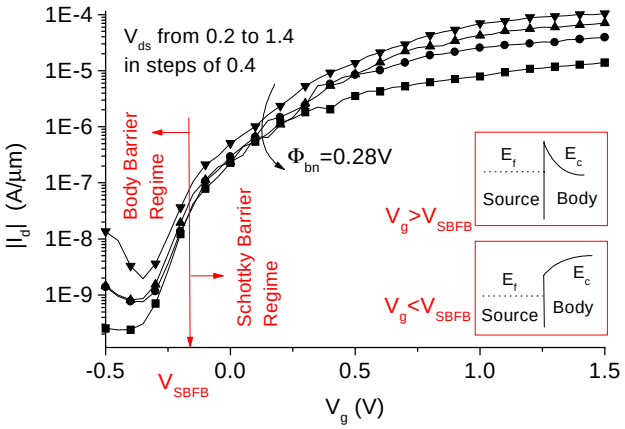


Figure 8: A 100nm NMOS device showing the two sub-threshold barrier mechanisms. Current barrier is controlled by the silicon body potential below the V_{sbfb}, and by the Schottky barrier above V_{sbfb}.

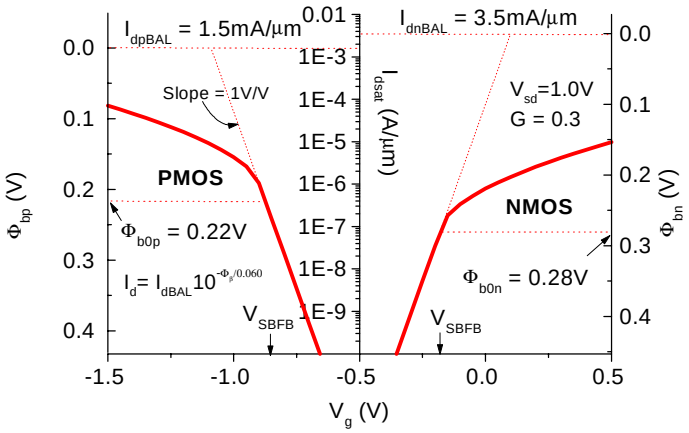


Figure 9: Construction of transmission model. Model includes barrier contributions from the silicon body, Φ_{b0}, $\Delta\Phi_i$, and $\Delta\Phi_t$. Current is derived from the barrier assuming a transmission probability of 1.

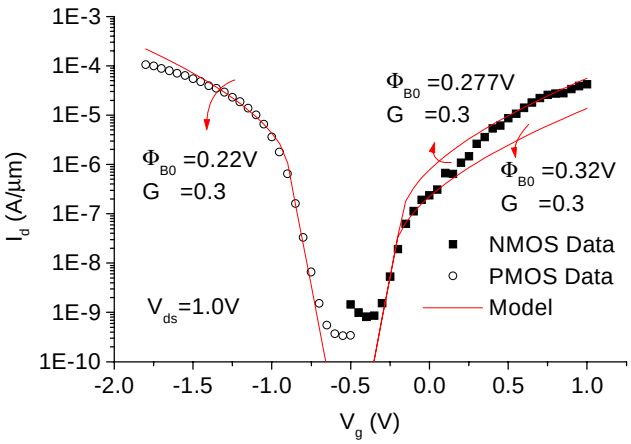


Figure 10: Barrier model fitting of 30nm wide PMOS and NMOS transistors. The G factor drops in strong inversion due to screening by the channel charge, leading to a deviation from the model at high gate biases.

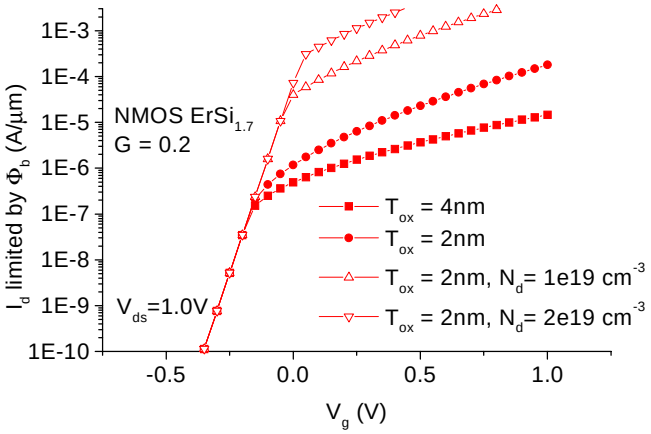


Figure 11: Investigation of the effect of oxide thickness scaling and extension doping on transmission current limit for NMOS. A conservative value of 0.2 is used for G. Reducing the oxide thickness to 20Å increases current for large V_g. A 40Å long extension doping (N-type) reduces the barrier height independently of V_g.

0.28V. This picture is consistent with the fact that Φ_{b0p} for $ErSi_{1.7}$ is 0.80V[7], indicating that the true Φ_{b0n} should be E_g-Φ_{b0p} =0.32V. At 500°C these interface states are annealed out and the Φ_{b0n} becomes 0.32V, **Fig. 7**. The presence of interface states is the likely cause of the higher variability in the NMOS device current, as well as the higher NMOS swing and DIBL values.

The I_{dsat} of our thin-body silicide source/drain devices needs to be improved to meet ITRS specifications, especially for the NMOSFET. The methods for improving device performance are: use a silicide with a lower barrier, reduce the oxide thickness, or add an extension doping to lower the barrier. Utilizing the transmission model described above, **Fig. 11** shows the effect of oxide scaling and the use of modest source/drain extension doping on the Schottky limit for I_{dsat} in NMOSFETs, assuming G=0.2. Oxide scaling improves I_{dsat} for $V_g > V_{sbfb}$, since it increases the electric field at the source/body interface. Adding an extension doping in the silicon drastically improves Schottky limit for I_{dsat} by providing a depletion layer at the source/body junction with an electric field largely independent of gate voltage, thereby directly reducing Φ_{b0}. The disadvantage of this approach is that it requires a high temperature annealing, while silicide source/drains without doping can be made below 400°C, making them compatible with a large array of gate electrode and dielectric materials. Doped source/drain devices will also show worse short channel effects, since the Schottky barrier will not be present to limit leakage current. **Fig. 12** shows the extension-doping level required to reach ITRS roadmap I_{dsat} specifications, with T_{ox} scaled to 2nm. Devices with the modest extension doping concentrations of $3E19cm^{-3}$ are projected to reach ballistic performance.

Conclusion

Complementary thin-body silicide source/drain devices with excellent turn-off characteristics have been demonstrated down to 15nm gate-length. Source/drains are fabricated from PtSi and $ErSi_{1.7}$ for PMOS and NMOS respectively. A simple transmission model fits device data and predicts that ballistic current levels can be obtained with the use of a 20Å oxide and 3E19 cm^{-3} extension doping.

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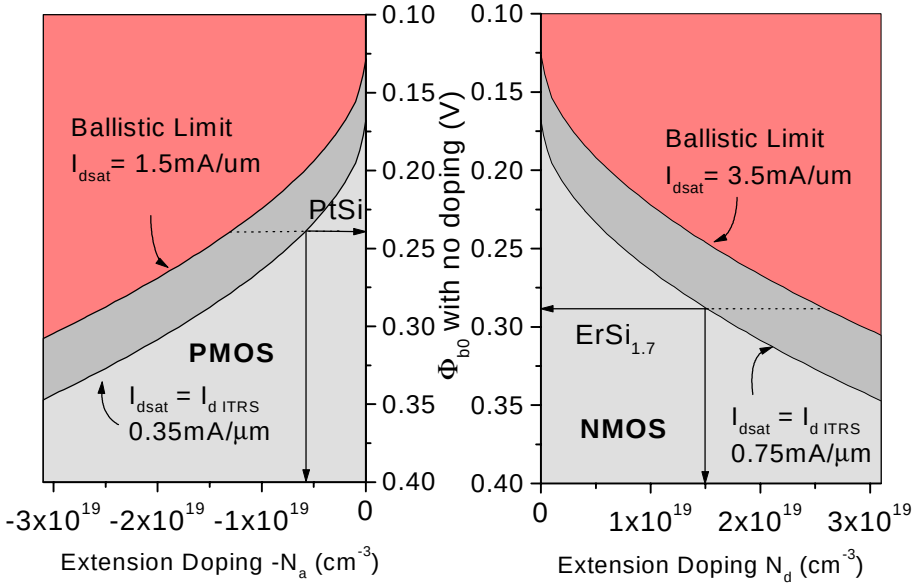

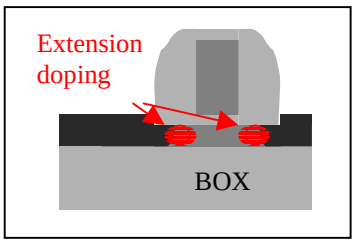

Figure 12: Contour plot of saturation current levels with Vdd=1.0V, for thin-body silicide source/drain transistors as a function of extension doping and flat-band barrier height. Strong screening is assumed, with G=0.1. Oxide thickness is 2nm. Ballistic current limits for both NMOS and PMOS can be reached with doping levels below 3E19 cm^{-3}.