A Generic Model of Memristors With Parasitic Components

Maheshwar Pd. Sah, Changju Yang, Hyongsuk Kim, Member, IEEE, Bharathwaj Muthuswamy, Jovan Jevtic, Member, IEEE, and Leon Chua, Life Fellow, IEEE

Abstract—In this paper, a generic model of memristive systems, which can emulate the behavior of real memristive devices is proposed. Non-ideal pinched hysteresis loops are sometimes observed in real memristive devices. For example, the hysteresis loops may deviate from the origin over a broad range of amplitude $A$ and frequency $f$ of the input signal. This deviation from the ideal case is often caused by parasitic circuit elements exhibited by real memristive devices. In this paper, we propose a generic memristive circuit model by adding four parasitic circuit elements, namely, a small capacitance, a small inductance, a small DC current source, and a small DC voltage source, to the memristive device. The adequacy of this model is verified experimentally and numerically with two thermistors (NTC and PTC) memristors.

Index Terms—Generic model, memristive devices, memristor, parasitic components, pinched hysteresis loop.

I. INTRODUCTION

The discovery of a physical model of a TiO$_2$ memristor [1] by a team of scientists from HP has attracted enormous interests from both industry and academia. The memristor was originally postulated by Leon Chua as the fourth basic circuit element in electrical circuits [2]–[4], and generalized in 1976 to a broader class of dynamical systems called memristive devices [5]. The most distinguished feature of memristive devices is the “pinched hysteresis loop” on the $i$-$v$ plane for any bipolar periodic voltage or current input signal that has a zero average value. Consequently, pinched hysteresis loops are used as the fingerprint to identify memristive devices. An “ideal” pinched hysteresis loop must pass through origin for any bipolar periodic input voltage $v(t)$ [resp., input current $i(t)$], which assumes both positive and negative voltages (resp., currents) and has a zero mean. The shape of the pinched hysteresis loop varies with frequency $f$ and shrinks to a single-valued function through the origin, as the frequency tends to infinity [6].

Another fingerprint of a memristor is the dependency of pinched hysteresis loop area on the frequency of the periodic excitation signal. Beyond some critical frequency $f_c$, the area of each of the two pinched hysteresis lobes in the first and third quadrant decreases monotonically as the frequency of the periodic input voltage $v(t)$ [resp., current $i(t)$] increases.

Although pinched hysteresis loops are the fingerprints of memristive devices, experimentally-measured pinched hysteresis loops of some real “physical” memristive devices may not pass through the origin [7]–[11], [20], [21]. In some cases, the pinched point may even disappear beyond some frequency $f$ of the applied voltage source $v(t)$, or current source $i(t)$ [7]. Also crucial impact of parasitic components may appear on the modeling the dynamics of log domain circuits [19]. Similarly, intelligence of the plasmodia and slime mould can be mapped to LC contour with a memristor [22], [23]. Fig. 1 shows some examples of experimentally measured non-zero crossing pinched hysteresis loops from real memristive devices, such as plants, Physisrum, TiO$_2$-based metal insulator devices, redox-based resistive switches, electrochemical systems, and venus fly trap [7]–[10], [20], [21]. The non-zero location of the pinched point may be caused by the presence of parasitic circuit elements and/or batteries.

The goal of this paper is to show, how to derive a composite 1-port circuit model $\mathcal{M}$ as shown in Fig. 2, which can emulate the measured pinched loops over a broad range of amplitude $A$ and frequency $f$, as closely as possible.

The concept of a “model” implies that there is no exact model for real-world devices [12]. In this paper, we propose a simple tractable 1-port memristor circuit model with a memristor plus four-small circuit elements, called parasitics, that can emulate the experimental pinched hysteresis loops as closely as possible over a set $\{A, f\}$ of amplitude $A$ and frequency $f$. Our proposed model can be applied to any memristive device whose measured pinched hysteresis loop did not pass through the origin [10], [20] where the pinched point occurs near the origin. The effect of the DC voltage source and/or current source is to translate this pinched point to the origin.

This paper is organized as follows: Section II reviews the characteristic fingerprints of an ideal memristor and memristive system. Section III presents our generic memristor circuit model using a memristor, a parasitic capacitance, a parasitic inductance, a small DC current source, and a small DC voltage source.
Section IV describes our generic memristor circuit model of an NTC thermistor, and a PTC thermistor. Comparison between the experimental and the simulated results from our generic NTC and PTC thermistor models are presented in Section V. Finally, some concluding remarks are presented in Section VI.

II. FINGERPRINTS OF MEMRISTORS

A memristor is defined as a two-terminal electrical device whose instantaneous voltage and current obey the state-dependent Ohm’s law. In this paper, we consider current-controlled memristors defined by

\[
\begin{align*}
    v &= M(x_1, x_2, \ldots, x_n) i \\
    \frac{dx_k}{dt} &= f_k(x_1, x_2, \ldots, x_n; i), \quad k = 1, 2, \ldots, n
\end{align*}
\]

where \( M \) is a continuous function of \( (x_1, x_2, \ldots, x_n) \), called the memristance, and \( x_i \)'s are the “n” state variables defined by a system of “n” ordinary differential equations.

Similarly, we consider voltage-controlled memristors defined by

\[
\begin{align*}
    i &= W(x_1, x_2, \ldots, x_n) v \\
    \frac{dx_k}{dt} &= f_k(x_1, x_2, \ldots, x_n; v), \quad k = 1, 2, \ldots, n
\end{align*}
\]

Another fingerprint of memristor is the dependency of the hysteresis lobe area on the frequency of the periodic excitation. For a bipolar periodic input voltage \( v(t) \), or current \( i(t) \), the pinched hysteresis loop has a typical shape depending on the memristor constitutive relation. Above a certain critical frequency \( f_c \), the magnitude of the area of the hysteresis lobe in the 1st or 3rd quadrant is inversely proportional to the excitation frequency \( f \). This property asserts that, the magnitude of the area of the pinched lobe gradually decreases with increasing frequency for \( f > f_c \), as shown in Fig. 3(b) for a memristor. The lobe area computed using Riemann-Stieltjes integral tracks the orientation of pinched hysteresis loop in clockwise or counterclockwise direction [15]. If the lobe area is positive (resp., negative) during a half cycle of the input signal, then the orientation of the pinched loop is clockwise (resp., counterclockwise) either in the 1st quadrant, or the 3rd quadrant, respectively and vice versa. The 1st and 3rd quadrant lobe area vs. frequency curve shown in Fig. 3(b) for a memristor is positive and negative respectively, which illustrate that the orientation of pinched hysteresis loop is clockwise and counterclockwise respectively.

III. GENERIC MEMRISTOR DEVICE MODEL

Our generic memristor device model is shown in Fig. 4. It consists of a voltage-controlled or current-controlled memristor \( M \) in parallel with a parasitic capacitor \( C_p \) and a parasitic DC current source \( I_F \), and a parasitic inductor \( L_p \), in series with a parasitic DC voltage source \( E_p \), is connected in series with the upper part of the circuit. The principle and circuit-theoretic concepts behind this generic circuit model date back to the mid-nineteen-sixties and had been presented at various conferences and applied in several publications on device modeling [12], [16], [18].

If \( v \) is the input voltage at time \( t \) in Fig. 4, then by KVL,

\[
v = v_1 + v_2,
\]
where $v_1$ is the voltage across the parallel connection of $M$ and $C_P$, and $v_2$ is the voltage across the serial connection of $L_P$ and $E_F$.

The current $i$ is given by KCL,

$$i = I_P + i_m + i_C,$$  \hspace{1cm} (4)

where $I_P, i_m, i_C$ denote the DC current source, the current through the memristor, and the current through the capacitor, respectively. Here, $M$ denotes the memristance $M(x_1, x_2, \ldots, x_n)$ which depends on the state variables $(x_1, x_2, \ldots, x_n)$ of the memristor.

It follows from (3) and (4) that,

$$\frac{dv_1}{dt} = -\frac{1}{C_P} \left[ i - M(x_1, x_2, \ldots, x_n) - I_P \right]$$  \hspace{1cm} (5)

$$\frac{di}{dt} = -\frac{1}{L_P} (v - v_1 - E_F)$$  \hspace{1cm} (6)

The state variables $(x_1, x_2, \ldots, x_n)$ are defined by “n” state equations

$$\frac{dx_1}{dt} = f_1(x_1, x_2, \ldots, x_n; v_1)$$

$$\frac{dx_2}{dt} = f_2(x_1, x_2, \ldots, x_n; v_1)$$

$$\vdots$$

$$\frac{dx_n}{dt} = f_n(x_1, x_2, \ldots, x_n; v_1),$$  \hspace{1cm} (7)

where we have assumed the memristor $M$ is voltage-controlled and described by

$$i_m = -\frac{1}{M(x_1, x_2, \ldots, x_n)} v_1.$$  \hspace{1cm} (8)

Altogether, (5), (6), and (7) constitute $n + 2$ state equations in $n + 2$ state variables $(v_1, i, x_1, x_2, \ldots, x_n)$.1 We will see in the following sections that the parasitic capacitance $C_P$, the parasitic inductance $L_P$, as well as the independent DC voltage $E_F$ and DC current $I_P$ can cause the Lissajous figure to deviate from the origin $(v, i) = (0, 0)$.

There exist many memristive devices made of “organic” materials or “electrolytes” which exhibit a pinched hysteresis loop where the “pinched point” occurs near, but not exactly at, the origin [10], [20]. Such devices are not passive because a small current will flow when a passive resistor is connected across the device. The energy in such memristive devices come from the internal chemical reactions, which can generate a small voltage, such as the classic Nernst potential.

IV. Modeling NTC and PTC Thermistors

Thermistors are physical devices whose steady-state DC resistance measured at a fixed applied DC voltage varies significantly with changes in the device temperature, which is a state variable whose dynamics is determined by some differential equation involving the state variable, and the input voltage.

1) Generic Memristor Circuit Model for a Physical NTC Thermistor: An ideal voltage-controlled, negative-temperature-coefficient (NTC) thermistor [5], [16] can be modeled by a voltage-controlled memristor with only one state variable $x \equiv T_N$:

$$i_N = W(T_N) v_N,$$  \hspace{1cm} (9)

$$W(T_N) = \left( R_{0N} e^{\beta_N (\frac{1}{T_N} - \frac{1}{T_{0N}})} \right)^{-1}$$  \hspace{1cm} (10)

where $v_N$ and $i_N$ denote respectively the terminal voltage and current of the NTC thermistor. $W(T_N)$ denotes the temperature-dependent conductance of the NTC thermistor, $R_{0N}$ denotes the thermistor resistance at ambient temperature $T_{0N}, T_N$ denotes a single state variable $x_1$ in (7) representing the absolute temperature of the NTC thermistor, and $\beta_N$ denotes a material-specific constant. Observe that the conductance $W(T_N)$ of the NTC thermistor with respect to $T_N$ in (10) increases as the temperature $T_N$ increases. Hence, the resistance $R(T_N) \equiv 1/W(T_N)$ decreases as $T_N$ increases.2 The state variable (temperature) $T_N$ depends on the power dissipation of the device via the heat balance equation,

$$\frac{dT_N}{dt} = -\frac{\delta_N}{H_{CN}} (T_{0N} - T_N) + \frac{W(T_N)}{H_{CN}} v_N^2,$$  \hspace{1cm} (11)

where $\delta_N$ denotes the dissipation constant, and $H_{CN}$ denotes the heat capacitance of the NTC thermistor.

In this paper, we will model a real physical NTC thermistor using the generic memristor device model in Fig. 4 via the three state (5), (6), and (7), with $E_F = 0$ and $I_P = 0$:

State equations describing a “physical” NTC thermistor

$$\frac{dv_1}{dt} = \frac{1}{C_P} \left[ i - M(x_1, x_2, \ldots, x_n) \right]$$  \hspace{1cm} (12)

$$\frac{di}{dt} = \frac{1}{L_P} [v - v_1 - E_F].$$  \hspace{1cm} (13)

$$\frac{dT_N}{dt} = -\frac{\delta_N}{H_{CN}} (T_{0N} - T_N) + \frac{W(T_N)}{H_{CN}} v_N^2.$$  \hspace{1cm} (14)

2) Generic Memristor Circuit Model for a Physical PTC Thermistor: An ideal voltage-controlled positive-temperature-
(PTC) thermistor is usually modeled with only one state variable $x \triangleq T_F$:

$$i_P = W(T_F)v_P$$

$$W(T_F) = \left( \frac{R_{OP}e^{\delta_P(T_F-T_0P)}}{R_{CF}(T_0P-T_F)} \right)^{1/4}$$

$$\frac{dT_F}{dt} = \frac{\delta_P}{H_{CF}}(T_0P - T_F) + \frac{W(T_F)}{H_{CF}}v_P^2.$$  \hspace{1cm} (16, 17)

where $v_P$ and $i_P$ denote respectively the terminal voltage and current of the PTC thermistor, $W(T_F)$ denotes the conductance of the PTC thermistor, $R_{OP}$ denotes the thermistor resistance at ambient temperature $T_0P$, $T_P$ denotes a single state variable (absolute temperature) $x_1$ in (7), $\delta_P$ denotes a material-specific constant, $\delta_P$ denotes the dissipation constant and $H_{CF}$ denotes the heat capacitance of the PTC thermistor. Observe from (16) that when the absolute temperature $T_F$ increases, then conductance $W(T_F)$ of the PTC thermistor decreases. Hence, the resistance $R(T_F) \propto 1/W(T_F)$ increases as $T_F$ increases.\footnote{The PTC thermistor is said to be a “positive-temperature dependent” resistor because its resistance increases as the temperature increases. The subscript “$P$” of $v$, $i$, and $T$ in (15)–(17) pertains to a “positive-temperature dependent” resistor.}

In this paper, we will model a real physical PTC thermistor using the generic memristor device model in Fig. 4 via the three state (5), (6), and (7), with $E_P = 0$, and $I_P = 0$:

State equations describing a “physical” PTC thermistor

$$\frac{dv_1}{dt} = \frac{1}{C_F} \left[ i - \frac{v_1}{R_{OP}e^{\delta_P(T_F-T_0P)}} - I_P \right]$$

$$\frac{di}{dt} = \frac{1}{I_P} \left[ v - v_1 - E_P \right]$$

$$\frac{dT_F}{dt} = \frac{\delta_P}{H_{CF}}(T_0P - T_F) + \frac{W(T_F)}{H_{CF}}v_1^2.$$  \hspace{1cm} (18, 19, 20)

V. EXPERIMENTAL AND SIMULATION RESULTS

In this section, we present hardware experiments and numerical simulations of negative-temperature coefficient (NTC) and positive-temperature coefficient (PTC) thermistors. The hardware experiments were performed with commercially available NTC and PTC thermistors at room temperature and their results were compared with simulations from our generic memristor device model.

The ideal mathematical models of NTC and PTC thermistors defined in (9)–(11) and (15)–(17) were simulated with a sinusoidal voltage source $v(t) = A \sin(2\pi ft)$ of amplitude $A$ and frequency $f$. The parameters used for the NTC and PTC thermistors in this paper are:

NTC thermistor: $T_0N = 300 \text{ K}$, $R_{0N} = 3.89 \text{ K}\Omega$, $H_{CN} = 0.14 \text{ J/K}$, $\delta_N = 0.1 \text{ W/K}$, $\delta_N = 5 \times 10^8 \text{ K}$,

PTC thermistor: $T_0P = 300 \text{ K}$, $R_{0P} = 40 \text{ \Omega}$, $H_{CP} = 0.6 \text{ J/K}$, $\delta_P = 0.05 \text{ W/K}$, $\delta_P = 2 \text{ K}$.

Fig. 5(a) and Fig. 5(b) show the numerically calculated pinched hysteresis loops of the NTC and the PTC thermistors at different frequencies of the applied sinusoidal voltage source (with amplitude $A = 6 \text{ V}$). Observe that, the loci in the current vs. voltage plane for the input signal exhibits zero-crossing pinched hysteresis loops for all the frequencies, as expected. Observe that the shape and lobe area of the pinched hysteresis loops shrink as the frequency of the input signal increases as expected. All pinched hysteresis loops of the ideal mathematical model of the NTC and the PTC thermistors satisfy the required fingerprints of a memristor, as expected.

Hardware experiments were conducted on both NTC and PTC thermistors to validate our generic memristive device model for real memristive devices. The first experiment was conducted on a commercially available Thermometric’s-NTC thermistor\footnote{The experiment was performed at lab environment on glass coated NTC Diode thermometrics thermistors (NTC-3.896KGJG). The device can be purchased and its specifications can be found from the following websites: http://www.devicemart.co.kr/goods/view.php?seq=8598, http://www-ge-mcs.com/download/temperature/920-320C.pdf.} in our laboratory. The initial small-signal resistance of the NTC thermistor was measured with an Ohm meter at zero DC applied voltage to be equal to 3.89 KΩ at room temperature. Fig. 6 shows the experimental results measured with the NTC thermistor driven by a sinusoidal voltage source with amplitude $A = 5 \text{ V}$ at different frequencies. When the frequency $f$ of the input signal is varied from 0.01 Hz to 100 Hz, the oscilloscope displays pinched hysteresis loops which pass through the origin. However, as the frequency of the input signal increases beyond 1 KHz, the pinched hysteresis loops on $i$-$v$ plane did not pass through the origin and the shape of the pinched loops also changes as the frequencies of the input signal increases. Fig. 6 also shows the simulation results of the NTC thermistor, when it is modeled with the generic memristor device model. The same input (sinusoidal source with amplitude $A = 5 \text{ V}$) is used in both tables. The parameters used for the simulation is $C_F = 5 \text{ nF}$, $L_P = 2 \text{ mH}$, $R_P = 0 \text{ V}$, $I_P = 0 \text{ A}$.

In order to see the role played by the parasitic capacitor $C_F$ and parasitic inductor $L_P$, Fig. 7 shows the corresponding results when only (9)–(11) (without the parasitic $C_F$ and $L_P$) are used for simulation, instead of the generic memristor device model. Comparing Fig. 6 and Fig. 7, we observe that the parasitics play an increasing role as the frequency increases beyond 100 Hz.

Fig. 8 shows simulation of the NTC thermistor when the effect of a parasitic voltage source $E_P$, and a parasitic current source $I_P$ are non-zero, and $C_F$ and $L_P$ are zero. When NTC
Fig. 6. Experimental measurements (blue) of a commercially available Thermometric’s-NTC thermistor (left side) and the corresponding simulated results (red) using the generic memristor device model (right side). The input is a sinusoidal source with amplitude of $A = 5 \text{ V}$. The experiment on the NTC thermistor was conducted at room temperature. The scale of $A$ and $v$ on the left side of each table is identical to that shown on the right side. The parameters used for simulations of the generic memristor device model of the NTC thermistor are: $T_{D} = 300 \text{ K}$, $R_{SN} = 3.89 \text{ K} \Omega$, $H_{CN} = 0.14 \text{ J/K}$, $\delta_{N} = 0.1 \text{ W/K}$, $\beta_{N} = 5 \times 10^{5} \text{ K}$, $C_{P} = 5 \text{ mF}$, $L_{P} = 2 \text{ mH}$, $E_{P} = 0 \text{ V}$, $I_{P} = 0 \text{ A}$.

Fig. 7. Simulated results using (9)–(11) (without parasitics) corresponding to Fig. 6.

is driven by a sinusoidal source with amplitude $A = 6 \text{ V}$ at frequencies $f = 0.1 \text{ Hz}$ and $0.3 \text{ Hz}$, the pinched hysteresis loops are not only translated to the pinched point but the shape of the pinched loops also changes as the value of $E_{P}$ and $I_{P}$ are varied. However, for higher frequencies $f = 100 \text{ Hz}$, the $i - v$ curve of the NTC thermistor is unchanged in shape except a translation to the point $(E_{P}, I_{P})$.

In order to see the effects of non-zero parasitic circuit elements in the NTC thermistor, the simulations are performed for different values of $C_{P}, L_{P}, E_{P}, I_{P}$ at various frequencies. Fig. 9 shows the pinched hysteresis loops in the NTC generic memristor device corresponding to frequencies $f = 0.08 \text{ Hz}$, $1 \text{ Hz}$, and $10 \text{ KHz}$ for sinusoidal source with amplitude $A = 6 \text{ V}$. Observe that the pinched hysteresis loops are changed to different shapes depending on the values of non-zero parasitic components.

We performed experiments on a commercially available Murata’s-PTC thermistor.\textsuperscript{6} The small-signal initial resistance at $v = 0$ was measured with an Ohm meter to be equal to $40 \Omega$, at room temperature. Fig. 10 shows the experimental and simulation results of the PTC thermistor using the PTC generic memristor device model for input voltage $v_{P} = A \sin(2\pi ft)$ with $A = 5 \text{ V}$, at different frequencies. The parameters used for the simulation are: $C_{P} = 0.1 \text{ mF}$, $L_{P} = 0.2 \text{ mH}$, $E_{P} = 0 \text{ V}$, $I_{P} = 0 \text{ A}$.

\textsuperscript{6}The experiment was performed at lab environment on Murata’s Lead type PTC thermistors (PTFM04BE471Q2N34B0). The device can be purchased and its specifications can be found from the following websites: http://www.eleparts.co.kr/EPXANC6G, http://search.murata.co.jp/Ceramy/CatalogAction.do?shHinnm=PTFM04BE471TS2F333shHinnm=PTFM04BE471Q2N34B0&shHin_key=PTFM04BE471Q2N34B0ShLang=enShParam=PTFM04BE471Q2N34B0.
Effects of parasitics on NTC generic thermistor model, when \( C_P \), \( L_p \), \( E_P \), and \( I_p \) are non-zero

<table>
<thead>
<tr>
<th>Simulation results without parasitic circuit elements</th>
<th>Simulation results when ( C_P = 5 \mu F ), ( L_p = 2 mH ), ( E_P = 1.5 V ), ( I_p = 0.8 mA )</th>
<th>Simulation results when ( C_P = 3 \mu F ), ( L_p = 2 mH ), ( E_P = 2 V ), ( I_p = 0.8 mA )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f = 0.08 ) Hz</td>
<td>( f = 0.08 ) Hz</td>
<td>( f = 0.08 ) Hz</td>
</tr>
<tr>
<td>( v = 0 V ) \n( i = 0 A )</td>
<td>( v = 1.5 V ) \n( i = 0.8 mA )</td>
<td>( v = 2 V ) \n( i = 0.8 mA )</td>
</tr>
<tr>
<td>( f = 1 ) Hz</td>
<td>( f = 1 ) Hz</td>
<td>( f = 1 ) Hz</td>
</tr>
<tr>
<td>( v = 0 V ) \n( i = 0 A )</td>
<td>( v = 1.5 V ) \n( i = 0.8 mA )</td>
<td>( v = 2 V ) \n( i = 0.8 mA )</td>
</tr>
<tr>
<td>( f = 10 KHz )</td>
<td>( f = 10 KHz )</td>
<td>( f = 10 KHz )</td>
</tr>
<tr>
<td>( v = 0 V ) \n( i = 0 A )</td>
<td>( v = 1.5 V ) \n( i = 0.8 mA )</td>
<td>( v = 2 V ) \n( i = 0.8 mA )</td>
</tr>
</tbody>
</table>

\( I_P = 0 A \). Observe that at low frequencies, the pinched hysteresis loops on the \( i \) vs. \( v \) plane are pinched at the origin. However, the loops are not pinched at higher frequencies. Observe that the experimental results (shown in blue) obtained from the PTC thermistor in the left side of each table is similar to the simulation results (shown in red) in the right side of the corresponding table in Fig. 10.

In order to see the role played by the parasitic capacitor \( C_P \) and parasitic inductor \( L_P \), Fig. 11 shows the corresponding results when only \((15)-(17)\) (without the parasitic \( C_P \) and \( L_P \)) are used for simulation, instead of the generic memristor device model. Observe that the parasitics play an increasing role as the frequency increases beyond 100 Hz.

Simulations are also performed in PTC generic memristor device to analyze the effects of \( C_P \) and \( L_P \) with zero and non-zero parasitic voltage source \( E_P \) and parasitic current source \( I_P \). Fig. 12 shows the pinched hysteresis loops corresponding to different values \( E_P \), \( I_P \) when \( C_P \) and \( L_P \) are zero. Observe that the pinched point and shape of the hysteresis loops are changed depending on the values of \( E_P \) and \( I_P \). At \( f = 0.01 \) Hz and 0.2 Hz, the parasitic voltage \( E_P \) and parasitic current \( I_P \) play an important role in not only shifting the pinched point to \((V, I) = (E_P, I_P)\), but also changing the shape of pinched hysteresis loops, as illustrated in Fig. 11. However at higher frequency \( f = 100 \) Hz, the pinched point is translated without changes in shape.

Simulations are also performed in PTC generic memristor device for non-zero parasitic circuit elements at different frequencies. Fig. 13 shows the pinched hysteresis loops.
The pinched point and the shape of the “pinched hysteresis loop” of real physical memristive devices may vary over a broad range of amplitude \( A \) and frequency \( f \). In this study, a generic model of a real memristor device is proposed to emulate the behavior of real memristor devices. It is shown that the changed of the pinched hysteresis loops of a memristive system from the ideal operation can be emulated by introducing appropriate parasitic circuit elements. The experimentally measured and numerically simulated pinched hysteresis loops of the NTC and the PTC thermistors illustrate that our generic model is adequate for emulating real physical memristive devices.

**REFERENCES**


Maheshwar Pd. Sah received the B.E. in electronics and communication engineering from Nepal Engineering College, Pokhara University, Nepal, in 2005, and the M.E. and Ph.D. in electronics engineering from Chonbuk National University, Korea, in 2010 and 2013 respectively, where he worked as a Postdoctoral Scholar from 2013 to 2014. He is currently a Visiting Scholar at the University of Notre Dame, IN, USA. His main research interests include emerging transistors technology, circuit design, cellular neural networks, analog Viterbi decoder, and analysis of memristor and memristive systems.

Changju Yang received the B.S and M.S. degrees in electronics and information engineering from Chonbuk National University, Korea, in 2008 and 2010 respectively, where he is currently studying toward the Ph.D. degree in electronics and information engineering. His main research interests include circuit design, analog Viterbi decoder, and analysis of memristor and memristive systems.

Hyongsuk Kim received the Ph.D. degree in electrical engineering from the University of Missouri, Columbia, MO, USA, in 1992. Since 1993, he has been a Professor with the Division of Electronics Engineering, Chonbuk National University, Korea. From 2000 to 2002 and again from 2009 to 2010, he was with the Nonlinear Electronics Laboratory, EECS Department, University of California, Berkeley, CA, USA, as a Visiting Scholar. His current research interests include memristors and their application to cellular neural/nonlinear networks.

Bharathwaj Muthuswamy received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 2002, 2005, and 2009 respectively. He is an Assistant Professor of Electrical Engineering at the Milwaukee School of Engineering (MSOE), Milwaukee, WI, USA. His areas of interest are nonlinear dynamical (chaotic) systems and embedded systems. His research involves investigating chaotic dynamics of the Muthuswamy-Chua system, understanding memristive behavior in discharge tubes, PIN junction diodes and superconducting Josephson junctions, studying applications of nonlinear dynamical systems using field programmable gate arrays, understanding the non-linear dynamics of atrial fibrillation and introducing nonlinear dynamics education at the undergraduate level.

Dr. Muthuswamy has held visiting professor appointments for teaching/research at the University of California, Berkeley; Vellore Institute of Technology; and the University of Western Australia.

Jovan Jevtic received a Ph.D. degree in computational electromagnetics from Ohio State University, Columbus, OH, USA, in 1999. He is an Assistant Professor of Electrical Engineering at the Milwaukee School of Engineering (MSOE), Milwaukee, WI, USA. Prior to joining MSOE, he worked in semiconductor processing and medical device industries as a Technology Program Manager and Senior Staff Scientist with a focus on new product development. He has published over 40 scientific works, including over 16 U.S. and international patents. His research is in the area of electromagnetic field applications for radio-frequency and microwave plasmas, magnetic resonance imaging, and induction heating.

Dr. Jevtic was recognized by James Clerk Maxwell foundation of Scotland for solving Smith's Prize problems set by Maxwell that remained unsolved since the 19th century.

Leon Chua (LF’02) received the M.S. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1961 and the Ph.D. degree in electrical engineering from the University of Illinois at Champaign-Urbana, IL, USA, in 1964. He has been a Professor at the University of California, Berkeley, CA, USA, since 1971. In 2011, he was appointed a Distinguished Professor at the Technical University of Munich. He was awarded seven patents and 14 honorary doctorates. When not immersed in science, he relaxes by searching for Wagner’s leitmotifs, musing over Kandinsky’s chaos, and contemplating Wittgenstein’s inner thoughts.

Prof. Chua received many awards including the first recipient of the Gustav Kirchhoff award, the Guggenheim Fellow award, and the European EC Marie Curie Fellow award. He was elected a foreign member of the Academia Europaea and of the Hungarian Academy of the Sciences. He was elected Chevaliers du Tastevin in 2000.