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A Low Power 1-MHz Continuous-Time Σ∆M Using a Passive Loop Filter Designed With a Genetic Algorithm Tool

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Abstract—This paper describes the design of a continuous-time amplifier-less second-order Sigma-Delta modulator (Σ∆M). In modern CMOS technologies the intrinsic gain of the transistors is low, which increases the difficulty of designing high gain amplifiers. The proposed Σ∆M uses a passive filter topology and therefore does not require an amplifier circuit. In order to maximize the performance, the circuit is optimized using genetic algorithms. The resulting circuit, designed in a 130 nm CMOS technology, has a bandwidth of 1 MHz for a clock frequency of 200 MHz. The electrical simulation results show that it achieves a maximum signal-to-noise-plus-distortion ratio (SNDR) of 52.8 dB and a dynamic range of 58 dB while dissipating 95 µW which corresponds to an efficiency of 133 fJ/conv.

I. INTRODUCTION

Σ∆Ms are very attractive for the design of power efficiency analog-to-digital converters (ADCs) mainly due to their insensitivity to components variations. This type of ADCs has a wide range of applications ranging from audio to communications and, despite their long use, they are still intensively investigated.

The downscaling of transistors in advanced nanometer CMOS technologies results in the reduction of the intrinsic gain (g_m/g_ds) [1] and in an increase in the variability, making the design of high gain opamps increasingly difficult, specially for larger bandwidths. In the case of Σ∆Ms this problem can be solved by using a passive filter topology [2], where a passive loop filter circuit is used. In this case, the only active block in the circuit is the comparator. An ideal comparator (or a comparator with positive feedback) will always produce a valid digital output, this infinite gain inside the Σ∆M will correspond to a finite processing gain, defined as a ratio of the rms value of the output of the comparator to rms value of its input.

The traditional approaches to implement a continuous-time (CT) or a discrete-time (DT) Σ∆M, normally, requires a number of amplifiers equal to the order of the loop filter. However, during the last few years, many design strategies have been developed in order to reduce the number of amplifiers and consequently the power consumption. Many implementations using hybrid active-passive loop filter can be found in [3]–[7] with improved results in terms of power consumption.

Unfortunately, they still depends of active elements such as operational amplifiers.

In [2], the authors present a low-pass passive Σ∆M with built-in mixer. Nevertheless, the approach entails problems and concerns about using cascaded resistor-capacitor (RC) sections. In order to avoid these concerns, a switched capacitor based loop filter is implemented instead of using a continuous-time RC one. An idea of a total passive loop filter for a CT Σ∆M is discussed in [8]. The design approach to implement the CT loop filter is based on the equivalent DT loop filter, which may be mathematically intractable for high orders. Furthermore, only few high-level results are presented and no output spectrum of the whole system is provided to corroborate the concept.

In this paper is presented a passive CT Σ∆M only using a comparator as active element. Most of the referenced solutions, relate problems and difficulty of using only cascade RC sections to implement the loop filter of the Σ∆M. In order to solve these issues, a modified tool is used based on a genetic algorithm (GA) [9] (modified for passive CT Σ∆Ms). With this tool, all the system can be optimized taking into account several parameters. Also, it is demonstrated that is not necessary to design a CT Σ∆M based on the equivalent DT loop filter or based in the direct CT synthesis method which is based on ordinary loop filters (e.g., Butterworth, Chebyshev, etc.) [10].

II. DESIGN STRATEGY

A block diagram of the 2nd order CT Σ∆M with feedforward structure is shown in Fig. 1.

![Block diagram of the 2nd order CT Σ∆M with feedforward structure.](image-url)
Typically a feed-forward architecture can work with only one feedback because the zero created by the feedforward path helps to stabilize the closed loop system. The negative feedback path in a \(\Sigma\Delta M\) reduces the quantization noise since it compares the quantized signal with the input signal and it then minimizes the error signal. In order for this procedure to work it is necessary to have gain in the feedback loop. In the case of a passive \(\Sigma\Delta M\) the only gain is the comparator gain. This means that if more than one feedback path is used the inner feedback path will have most of the processing gain of the comparator. Therefore, in order to have a stable loop with only one feedback path it is necessary to add a zero to the loop gain. This can be achieved by adding a resistor in series with the capacitor in the second RC circuit.

For the design of the loop filter, a modified tool based on a GA (modified for passive CT \(\Sigma\Delta M\)s) was used. In this tool, a initial randomly population constituted by \(N\) chromosomes is created. Each chromosome, containing the values of the resistors and capacitors used in the modulator, is evaluated and its total fitness \(f_T\) is calculated based on the desired specifications.

The \(f_T\) is obtained as the product of \(N\) partial fitnesses, \(f_i\), each one depending on the \(i\)-th specification, \(s_i\), as follows

\[
f_T = \prod_{i=1}^{N} f_i(s_i).
\]

where the functions \(f_i(s_i)\) may assume two forms, depending on the desired target: maximize (6) or minimize (7) (e.g. maximize the signal-to-noise-plus-distortion ratio (SNDR) and minimize the area).

\[
f_i(s_i) = 1 - e^{-w_i(s_i/\bar{s}_i)}
\]

\[
f_i(s_i) = e^{-w_i(s_i/\bar{s}_i)}
\]

The \(s_i\) and \(\bar{s}_i\) represent the achieved and desired specification, respectively. The variable \(w_i\) is a weight factor used to prioritize a given partial fitness.

### III. Circuit Design

In this section, the design of the loop filter (designed with the GA tool) and the latched comparator design is presented.

#### A. CT Loop Filter

The electrical schematic of the differential 2\textsuperscript{nd} order passive CT \(\Sigma\Delta M\) with feedforward structure is shown Fig.3. This electrical circuit was analyzed and its exact transfer function, including load effect, was obtained and used in SIMULINK\textsuperscript{®} to obtain the exactly behavior of the circuit.
on author’s experience. The evolution of the average SNDR\(^1\) during each generation is shown in Fig. 4. After the 100 generations, the best possible result was given by the genetic tool. The optimized modulator design parameters are summarized in TABLE I. Fig. 5 depicts the output spectrum of the passive CT \(\Sigma\Delta M\) performed by the GA tool showing it achieved a peak SNDR about 65 dB. For a RC passive filter, the thermal noise is limited only by the size of the capacitor and high resistors are not a concern in terms of thermal noise [11].

### B. Latched Comparator

The comparator used in the \(\Sigma\Delta M\) is shown in Fig. 6 [12]. It consists of a differential input stage, two regenerative flip-flops, and a set-reset (S-R) output latch built with two NAND gates. The input stage is important to reduce the input-referred offset of the regenerative flip-flops, which is too big (tens of mV) for the purpose of this work.

The comparator works as follows: When \(\text{ latch}\) signal goes low, transistors M4-M6 are turned on and M7-M8 are turned off. Hence, the input of the S-R latch is tied to \(V_{DD}\) and the S-R latch behaves as two back-to-back inverters, holding the previous state. In this reset phase, also, the input difference (\(V_{op} - V_{in}\)) is amplified. When \(\text{ latch}\) signal goes high, transistors M4-M6 are turned off and M7-M8 are turned on. Consequently, the NMOS (M11-M12) and PMOS (M9-M10) flip-flops regenerate the amplified difference, pulling one of the output towards \(V_{DD}\) and the other towards \(V_{SS}\). This new state is stored in the S-R latch when \(\text{ latch}\) signal goes low again.

\(^1\)Average SNDR after the performance of all individuals (50 individuals per generation).

**TABLE I**

<table>
<thead>
<tr>
<th>Passive Component Values After Optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>(R_1 = R_2)</td>
</tr>
<tr>
<td>(R_3 = R_4)</td>
</tr>
<tr>
<td>(C_{11} = C_{22})</td>
</tr>
<tr>
<td>(R_5 = R_6)</td>
</tr>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>(R_7 = R_8)</td>
</tr>
<tr>
<td>(C_{11} = 1.198 \text{ pF})</td>
</tr>
<tr>
<td>(R_9 = R_{10})</td>
</tr>
<tr>
<td>(C_{22} = -)</td>
</tr>
</tbody>
</table>

![Fig. 4. Number of generations versus SNDR.](image)

![Fig. 5. Output spectrum (high level model) of the passive CT \(\Sigma\Delta M\) (2\(^{16}\) points FFT).](image)

![Fig. 6. Electrical schematic of the CMOS comparator.](image)

In order to improve the driving capability of the comparator, allowing it to drive at \(R_2\) and \(R'_2\), non-minimum-sized CMOS inverters are used. The sizing of these inverters trades off driving strength with power dissipation. The comparator has a maximum delay time around 400 ps for an input signal of about 1 mV.

**IV. Simulation Results**

The circuit was designed in 130 nm 1.2 V CMOS technology. An electrical transient noise simulation shows that the \(\Sigma\Delta M\) circuit achieves a peak SNDR of 52.8 dB (for \(BW = 1\) MHz) and a dynamic range of 58 dB (Fig. 8). The FFT of the output signal of the \(\Sigma\Delta M\) for an input signal with differential amplitude of 400 mV is shown in Fig. 7.

**TABLE II** summarizes the electrical performance of the modulator and also compare the results with other works. The achieved FoM (simulation results) shows that the proposed \(\Sigma\Delta M\) has good energy efficiency and was calculated based in (8).

\[
\text{FoM} = \frac{\text{POWER}}{2 \cdot \text{BW} \cdot 2^{\text{ENOB}}} 
\]

(8)
95 µW which corresponds to an efficiency of 133 fJ/conv for a 1 MHz bandwidth. Since the only active block in the circuit is a comparator, additional studies with others types of comparators could eventually improve the results of this architecture.

ACKNOWLEDGMENT

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REFERENCES


V. CONCLUSION

A CT ΔΣM amplifier-less second-order with a passive loop-filter was proposed. In order to maximize the performance, the circuit is optimized using genetic algorithms. The electrical simulation results of the circuit, designed in a 130 nm CMOS technology, shows that it achieves a maximum SNDR of 52.8 dB and a dynamic range of 58 dB while dissipating...