Evaluation of Transition Untestable Faults Using a Multi-Cycle Capture Test Generation Method

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Abstract—Overtesting induces unnecessary yield loss. Untestable faults have no effect on normal functions of circuits. However, in scan testing, untestable faults may be detected through scan chains. Detected untestable faults cause overtesting. Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults. Uncontrollable faults may be detected under invalid states through scan chains by shift-in operations. Unobservable faults cannot be observed at primary outputs, but their effects may be propagated to scan flip-flops. Thus, unobservable faults may be detected through scan chains by shift-out operations. Several methods to reduce the number of detected untestable faults were recently proposed. These methods identify invalid states and generate test patterns avoiding invalid states. As the result, the number of detected uncontrollable faults was reduced. However, they cannot reduce the number of detected unobservable faults. In this paper, both uncontrollable and unobservable faults are identified using a multi-cycle capture test generation method. We evaluate the relationship between the numbers of untestable faults and the number of time expansions for ISCAS’89 benchmark circuits, and also evaluate factors that untestable faults are identified.

I. INTRODUCTION

Recently, many design methodologies have been developed to resolve the yield loss problem. One of methodologies for yield loss is to improve the test quality on manufacturing VLSIs.

Currently, Design for Testability (DFT) is one of methods to improve the test quality for VLSIs. A scan design method [1] is one of popular DFT methods for logic circuits. In full scan design method, all Flip-Flops (FFs) are replace with scan FFs. A scan FF is equivalent to a primary input and a primary output at the scan mode. In full scan designed circuits, each test pattern can be set to scan FFs using scan chains. However, in scan testing, untestable faults may be detected through scan chains. On the other hand, Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults. Uncontrollable faults may be detected under invalid states through scan chains by shift-in operations. Unobservable faults cannot be observed at primary outputs, but their effects may be propagated to scan flip-flops. Thus, unobservable faults may be detected through scan chains by shift-out operations. Detected untestable transition faults cause overtesting[2]. In this paper, our target fault model is a transition fault model.

Overtesting induces unnecessary yield loss. Untestable faults have no effect on normal functions of circuits. Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults. First, uncontrollable faults may be detected under invalid states through scan chains by shift-in operations. Second, unobservable faults cannot observe at primary outputs, but their effects may be propagate to scan flip-flop. Thus, unobservable faults may be detected through scan chains by shift-out operations. Several methods[3][4][5] to reduce the number of untestable faults were proposed. These methods identify invalid state and generate test pattern avoid invalid states. As the result, the number of detected uncontrollable faults was reduced. However, they cannot reduce the number of detected unobservable faults. These methods cannot reduce the number of detected unobservable faults.

Multi-cycle capture test methods [6] generate test patterns with multiple capture cycles. Circuits under the test sequentially operate with test sequences generated by multi-cycle capture test generation (MCTG). Let $k$ be the number of sequential operations. If $k$ is larger, the test generation complexity becomes one for sequential circuits and it is difficult to generate test sequence. On the other hand, If $k$ is smaller, the test generation complexity is nearly equal to one for combinational circuits and it is easy to generate test sequence. When $k$ is large, many untestable faults can be identified. A MCTG method identifies not only faults detected under only invalid states but also faults whose effects cannot be observed at primary outputs.

In this paper, we evaluate the relationship between the number of untestable faults and the number of time expansions($k$). Next, we evaluate factors that untestable faults are identified. We classify the factors for untestable fault identification into four categories.

1) the condition of primary inputs controllability
2) the condition of primary outputs observability
3) the condition of justification
4) the condition of propagation for fault effects

This paper is organized as follows. In Section 2, preliminaries are introduced to transition fault model, untestable faults, multi-cycle capture test and detection of untestable
faults. In Section 3, we propose factors that untestable faults are identified and classify the factors for untestable fault identification. Experimental results for ISCAS’89 benchmark circuits are shown in Section 4. Finally, Section 5 concludes the paper.

II. PRELIMINARIES

In this section, we introduce transition fault model, untestable faults, multi-cycle capture test and the detection of untestable faults using scan chains.

A. Transition fault model

Let \( T \) be clock period, \( T_g \) be delay time of a path without transition fault and \( Del \) be additional delay time for a transition fault in Figure 1. If \( Del > T - T_g \), the effect of transition faults propagate FFs. In broadside test which are equal to 2 cycle capture test, \( Del \) which can be observed FFs is from \( 2T - T_g \) to \( T - T_g \). Figure 2 shows a 2 cycle transition fault model on 3-times expansion model.

In Figure 2, \( Del \) which can be observed FFs is from \( 3T - T_g \) to \( T - T_g \) using 3 cycle capture test. Because we aim to reduce the overtesting of broadside testing, our target delay fault size \( Del \) is is from \( 2T - T_g \) to \( T - T_g \) in this paper.

B. Untestable faults

Untestable faults are classified into combinational redundant faults sequentially redundant faults. The combinational redundant faults cannot be detected by any combinational test patterns. The sequential redundant faults do not affect the functions of circuits. Methods to identify these untestable faults use sequential ATPG [7][8][9] based on time expansion models [10] and invalid states identification [11][12].

C. Multi-Cycle Capture Test

Multi-cycle capture test methods for transition faults [6][13][14] generate test sequences with multiple capture cycles. Circuits under the test sequentially operates for two or more clock cycles by the generated test sequence. Let \( k \) be the number of sequential operations. Fig. 3 shows a waveform of \( k = 4 \) cycle capture test sequence. There are four capture clock cycles on one capture cycle in Fig. 3. If \( k \) is larger, the test generation complexity becomes one for sequential circuits. When \( k \) is large, the possibility of setting invalid states to scan FFs by multi-cycle capture test sequence is low. The possibility of detection of untestable faults by multi-cycle capture test sequences is low and many untestable faults can be identified. However, the MCTG is difficult for \( k \)-time expansion model. On the other hand, if \( k \) is smaller, the test generation complexity is nearly equal to one for combinational circuits. When \( k \) is small, the possibility of setting invalid states to scan FFs by multi-cycle capture test sequences is high. The possibility of detection of untestable faults by multi-cycle capture test sequences is high.

The relationship between \( k \) which is the number of time expansion and difficulty to generate multi-cycle test sequence is considered. If \( k \) is larger, the number of time expansions is large. Therefore, the size of test generation model is bigger and test generation is difficult. If \( k \) is smaller, the number of time expansion is small. Therefore, the size of test generation model is smaller and test generation is easy.

Next, the relationship between \( k \) and valid / invalid states is considered. If \( k \) is larger, the possibility of valid states after sequential operations of test sequences generated by multi-cycle capture test is higher. It is possible to transfer from invalid states to valid states. However, it is impossible to transfer from valid state to invalid state using sequential operations.

D. Detection of untestable faults using scan chains

On full scan designed circuits, each test pattern can be set to scan FFs and be observed to scan FFs through scan chains. A scan FF is equivalent to a primary input and a primary output at the scan mode. The test generation for full scan designed circuits is easy for ability to set each test pattern to scan FFs. On the other hand, untestable faults may be detected through scan chains. Detected untestable faults cause overtesting. Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults.

Invalid states [11][12] cannot reach from any valid states using sequential operation. However, invalid states can be set using only scan chains. Uncontrollable faults may be detected under only invalid states through scan chains by
shift-in operations. Unobservable faults cannot be observed at primary outputs, but their effects may be propagated to scan flip-flops. Thus, unobservable faults may be detected through scan chains by shift-out operations.

A transition fault is detected with 2 cycle capture test pattern and may not be generated test pattern which is detected with 3 cycle capture test pattern. There are two cases. First, the fault effects cannot propagate to observable scan flip-flops. Second, states to detect the fault cannot be justified. This fault cannot be identified as untestable fault using 2 cycle capture test generation. Fig. 4 shows a untestable transition faults on 3-times expansion model.

III. AN EVALUATION METHOD OF TRANSITION UNTESTABLE FAULTS

A. k-time expansion model for transition faults

In k-time expansion model, pseudo primary inputs are outputs of scan FFs at time frame 1, pseudo primary outputs are inputs of scan FFs at time frame k, and combinational circuits are expanded sequential circuits to k-times frame. It is difficult to synchronize the frequencies of primary inputs and primary outputs on ATE with the frequency of internal FFs. Thus, the value of primary inputs is fixed at all the time frame and the effect of faults cannot be observed on primary outputs in k-time expansion model. Figure 5 shows k-time expansion model for transition faults.

B. Test generation method using multi-cycle capture test

In a transition fault test generation method using multi-cycle capture test, transition faults are detected using k-time expansion model. Target circuits are full scan designed circuits. Figure 6 shows an example of full scan designed circuits. In Fig. 6, Z(1), Y1(1), and Y2(1) denote primary outputs, inputs of FFs and output of FFs, respectively. A transition fault test generation method using multi-cycle capture test transforms full scan designed circuits in Fig. 6 to the 3-time expansion model in Fig. 7. In Fig. 7, Z(i) denote primary outputs for time i(1 ≤ i ≤ 3), Y1(1) and Y2(1) denote pseudo primary inputs, Y1(3) and Y2(3) denote pseudo primary outputs. The fault model assumes a single transition fault model in this paper. There are multiple faults at a corresponding signal line each time frame.

C. Untestable fault identification

The time frame where transition faults are activated influences the fault classification results. Figure 6 shows an example of full scan designed circuits. Figure 8 shows 2-time expansion model of Fig. 6. Figure 7 shows 3-time expansion model of Fig. 6. The value of primary inputs is fixed at all the time frame and the effect of faults cannot be observed on primary outputs in the time expansion model. The slow-to-rise faults of line a on Time 2 in Fig 8 and Time 2, 3 in Figure 7 are target faults of MCTG.

First, the slow-to-rise fault of line a on Time 2 in Fig 8 is targeted. It is necessary that assignment values of Y1(1) = 1 and Y2(1) = 0 to excite the fault. The effect of the slow-to-rise fault on line a is propagated to Y2(2) by those assignment values. Thus, the slow-to-rise fault of line a on Time 2 in Fig 8 can be detected.

Second, the slow-to-rise fault of line a on Time 3 in Fig 9 is targeted. It is necessary that assignment values of Y1(1) = 1 and Y2(1) = 1 to excite the fault. On Time 3, the value of line a changes from 0 to 1. The effect of the slow-to-rise fault of
line \( a \) on Time 3 is propagated to \( Y2(3) \) by those assignment values. The effect of the slow-to-rise fault of line \( a \) on Time 2 is not activated because the value of line \( a \) does not change from 0 to 1 on Time 2. Thus, the slow-to-rise fault of line \( a \) on Time 3 in Fig 9 can be detected.

Finally, the slow-to-rise fault of line \( a \) on Time 2 in Fig 10 is targeted. It is necessary that assignment values of \( Y1(1) = 1 \) and \( Y2(1) = 0 \) excite the fault. On Time 2, the value of line \( a \) changes from 0 to 1. However, the effect of the slow-to-rise fault of line \( a \) on Time 3 is not propagated to \( Y1(3) \) or \( Y2(3) \). Because the input value of the AND gate \( U1 \) is 0 on Time 3. Thus, the slow-to-rise fault of line \( a \) on Time 2 in Fig 10 cannot be detected and can be identified as untestable faults.

In these results, the slow-to-rise fault classification results of line \( a \) on Time 2 and that on Time 3 are different. When a fault is identified as untestable fault at least one excitation time, the fault is classified as untestable fault[9]. Therefore, it is necessary to excite faults on each time frame in order to identify untestable fault correctly.

**D. Test generation for transition faults in \( k \)-time expansion models**

A Soc (System-on-a-Chip) has multi clock domains. The test patterns for transition faults in each clock domain are generated. When FFs in the same clock domain capture the effects of transition faults, transition faults influence the circuit. Even if the effects of transition faults propagate to FFs in other clock domain or primary outputs, these transition faults do not generally be detected. The effects of transition fault in a clock domain do not always influence the circuit of other clock domain and systems which connected to primary outputs. Therefore, the value of primary inputs is fixed at all the time frame and the effect of faults cannot be observed on primary outputs in broad-side model.

Figure 11 shows a 3-time expansion model with \( PO_3 \) on Time 3. In Fig 11, when an effect of the transition fault which excited on Time 2 is captured a \( FFs_2 \) on Time 2 and the effect propagate to \( PO_3 \) on Time 3, the effect of the transition fault cannot be detected at \( PO_3 \). Because the value of \( FFs_2 \) on Time 2 propagates to \( PO_3 \), the effects of the transition fault do not propagate to \( PO_3 \). Therefore, if \( a < b \), when effects of the transition fault which excited on Time \( a \) is captured FFs on Time \( a \) and the effect propagate to PO on Time \( b \), the effect of the transition fault can be detected at PO on Time \( b \).

In time expansion model whose \( k \) is 3 or more, the value of primary inputs is normally fixed at all the time frame. It is difficult to synchronize the frequencies of primary inputs on ATE with the frequency of internal FF’s. However, the value of a primary input is not always fixed on sequential operation. Therefore, the condition that the value of primary inputs is fixed at all the time frame may be superfluous when untestable faults are identified.

There are four condition models for time expansion model whose \( k \) is 3 or more.

- **Model A** the value of primary inputs is fixed and the effects of transition faults cannot be detected at primary outputs.
- **Model B** the value of primary inputs is **not** fixed and the effects of transition faults cannot be detected at primary outputs.
- **Model C** the value of primary inputs is fixed and the effects of transition faults **can** be detected at primary outputs.
experiments, there are five kinds of excited times for transition faults (from Time 2 to Time 6). Test patterns are generated for each fault 5 times, changing the excitation time. Table II shows experimental results. In Tab.II, Cir, UT2, UT6, UT4D, UT1 denote the circuit name, the number of untestable faults on 2-time expansion model, the number of untestable faults on 4-time expansion model, the number of faults which are identified as untestable faults under only one excitation time and which are identified as detected faults under other five excitation time on 6-time expansion model, and the number of faults which are identified as detected faults under only one excitation time and are identified as untestable faults under other five excitation time on 6-time expansion model, respectively. In these results, there is no fault identified as untestable faults (UT1) under only one excitation time. However, there are detected faults (UT1) under only one excitation time and which are identified as untestable faults under other excitation time. Finally, these faults (UT1) are identified as untestable faults[9]. The excitation time is 6 for faults. Thus, Time 6 is the last time frame. When the test pattern is generated for the transition fault excited at the only last time frame, the fault might be identified to be not the untestable fault but detected fault.

Next, we evaluate the relationship between Model A, Model B, Model C and Model D. Target faults on each Model B, Model C and Model D are identified as untestable faults on Model A and identified as detected untestable faults on 2-time expansion model. Table III shows experimental results. In Tab.III, Cir, UT2, UT6, UT4D denote the circuit name, the number of target faults, the number of untestable faults on Model B, the number of untestable faults on Model C, the number of untestable faults on Model D, respectively. In Tab.III, the number of untestable faults on Model B is smaller than that of Model C in each the
TABLE III

A RELATIONSHIP OF BETWEEN MODEL A, MODEL B, MODEL C AND MODEL D

<table>
<thead>
<tr>
<th>Cir</th>
<th>$UT_0 - UT_2$</th>
<th>$UT_B$</th>
<th>$UT_C$</th>
<th>$UT_D$</th>
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<tr>
<td>s5378</td>
<td>384</td>
<td>256</td>
<td>338</td>
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<td>422</td>
<td>162</td>
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<td>645</td>
<td>678</td>
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<tr>
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<td>809</td>
<td>280</td>
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<tr>
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<tr>
<td>s38417</td>
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<td>740</td>
<td>1,004</td>
<td>676</td>
</tr>
</tbody>
</table>

TABLE IV

FACTORS OF IDENTIFIED UNTESTABLE FAULTS

<table>
<thead>
<tr>
<th>Cir</th>
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<th>Just</th>
<th>Prop</th>
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<tbody>
<tr>
<td>s5378</td>
<td>384</td>
<td>181</td>
<td>79</td>
<td>124</td>
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<td>s9234</td>
<td>453</td>
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<td>886</td>
<td>208</td>
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<td>474</td>
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<td>1,050</td>
<td>374</td>
<td>283</td>
<td>393</td>
</tr>
</tbody>
</table>

circuits. The number of untestable faults of Model D is larger than that of Model B and Model C in s35932. On the other hand, the number of untestable faults of Model D is smaller than that of Model B and Model C in s13207. Under only one excitation time and which are identified as untestable faults under other excitation time and are identified as untestable faults, finally. We show the relationship of the number of untestable faults under each condition of Model A, Model B, Model C and Model D.

In our future work, an efficient method to identify untestable faults and a multi-cycle capture test generation methods for 0 detected untestable faults must be developed.

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