GaAs MESFET MODELING FOR DIGITAL INTEGRATED CIRCUIT SIMULATION

A Licentiate’s Thesis

by

Mikael Andersson

Electron Physics Laboratory
Department of Electrical Engineering
Helsinki University of Technology

Otaniemi, Finland

1991
The most popular gallium arsenide MESFET models are reviewed and compared. A new developed model with physical input parameters is described, as well as techniques for modeling the subthreshold region of the device. The implementation of all the treated models into a SPICE circuit simulator version is outlined, and simulation examples using these models are shown. Model parameter extraction and optimization techniques are also discussed, and a computer program developed for this purpose is briefly described.

Keywords: Gallium Arsenide, MESFET, modeling, simulation
Preface

First of all, I wish to thank Professor Juha Sinkkonen for his friendly attitude and his interest in this work.

The writing of this thesis was greatly aided by the strongly encouraging and patient attitude of the leader of the IC Design Group at the Semiconductor Laboratory of the Technical Research Centre of Finland, Lic. Tech. Helena Pohjonen. Many thanks are also due to all my colleagues in the IC Design Group for their friendly and helpful attitude and constructive criticism.

Most of this work was done during the NOrdic Gallium Arsenide Program (NOGAP) 1986 - 88. I would like to thank all my colleagues in Finland, Sweden and Norway, who participated in this project, for an interesting and stimulating collaboration. The circuits designed during NOGAP, including the devices used in this work, were fabricated by TriQuint Semiconductor Inc. I would like to thank the people at this company for their splendid foundry services.

Special thanks are also due to Professor Stephen Long of the University of California, Santa Barbara, whose laboratory I visited during January - February 1987. I learned a lot from his excellent course in GaAs IC design, and the suggestions by him and his students concerning the computer program MESFETOPT have aided its development greatly.

Finally, the patience and encouragement of my wife is warmly acknowledged.

Olarinluoma
January 25, 1991

Mikael Andersson
## Contents

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preface .................................................................</td>
</tr>
<tr>
<td>Contents .........................................................................</td>
</tr>
<tr>
<td>List of symbols and abbreviations ................................</td>
</tr>
<tr>
<td>1. Introduction ..........................................................</td>
</tr>
<tr>
<td>2. GaAs transistors .......................................................</td>
</tr>
<tr>
<td>2.1 The JFET and MESFET ..............................................</td>
</tr>
<tr>
<td>2.2 The HFET and HBT ..................................................</td>
</tr>
<tr>
<td>3. GaAs MESFET characteristics .......................................</td>
</tr>
<tr>
<td>4. GaAs MESFET digital logic ..........................................</td>
</tr>
<tr>
<td>4.1 Buffered FET logic ..................................................</td>
</tr>
<tr>
<td>4.2 Schottky diode FET logic .........................................</td>
</tr>
<tr>
<td>4.3 Direct coupled FET logic ..........................................</td>
</tr>
<tr>
<td>5. The SPICE program ....................................................</td>
</tr>
<tr>
<td>5.1 SPICE capabilities ..................................................</td>
</tr>
<tr>
<td>5.2 DC analysis ............................................................</td>
</tr>
<tr>
<td>5.3 AC analysis .............................................................</td>
</tr>
<tr>
<td>5.4 Transient analysis ...................................................</td>
</tr>
<tr>
<td>6. The MESFETOPT program .............................................</td>
</tr>
<tr>
<td>7. General device DC analysis theory ..................................</td>
</tr>
<tr>
<td>8. GaAs MESFET models ..................................................</td>
</tr>
<tr>
<td>8.1 Semiconductor device model types ...............................</td>
</tr>
<tr>
<td>8.2 General MESFET circuit model topics ...........................</td>
</tr>
<tr>
<td>8.3 Basic device theory ..................................................</td>
</tr>
<tr>
<td>8.4 The Shockley model .................................................</td>
</tr>
<tr>
<td>8.5 The JFET model .......................................................</td>
</tr>
</tbody>
</table>
8.6 The hyperbolic tangent model ............................................................... 35
8.7 The Statz model ................................................................................ 37
8.8 The cubic model .............................................................................. 39
8.9 The VTT model .............................................................................. 40
8.10 Other models ................................................................................ 45
8.11 Subthreshold models .................................................................... 46
8.12 Schottky barrier diode models ...................................................... 50
8.13 Gate-source and gate-drain capacitance models ......................... 54

9. Parameter extraction ........................................................................... 58
   9.1 Extraction methods ....................................................................... 58
   9.2 Manual extraction ................................................................ ...... 59
   9.3 Computer extraction methods .................................................... 60

10. SPICE model implementation ......................................................... 63

11. Simulation results ........................................................................... 65
   11.1 DC analysis speed ..................................................................... 65
   11.2 Transient analysis example ...................................................... 67

12. Conclusions .................................................................................... 70

13. References .................................................................................... 71

Appendix 1, SPICE input file, 4 pages
List of symbols and abbreviations

\( \alpha \)  \quad \text{ALPHA - hyperbolic tangent parameter}

\( a \)  \quad \text{Thickness of the MESFET channel}

\( A_0 - A_3 \)  \quad \text{Polynomial factors}

\( A^\# \)  \quad \text{Schottky barrier Richardson constant}

\( \text{AlGaAs} \)  \quad \text{Aluminium Gallium Arsenide}

\( \text{ALE} \)  \quad \text{Atomic Layer Epitaxy}

\( A_n \)  \quad \text{Coefficients for the solution of Laplace’s equation}

\( \beta \)  \quad \text{BETA - transconductance coefficient}

\( b(x) \)  \quad \text{Thickness of conducting part of channel as a function of position}

\( b_1 \)  \quad \text{Thickness of conducting part of channel at the beginning of the saturation region}

\( b_2 \)  \quad \text{Thickness of conducting part of channel at the drain end, in the saturation region}

\( B \)  \quad \text{Doping profile parameter}

\( \text{BFL} \)  \quad \text{Buffered FET Logic}

\( \text{BJT} \)  \quad \text{Bipolar Junction Transistor}

\( \text{CDFL} \)  \quad \text{Capacitor-Diode FET Logic}

\( C_{DS} \)  \quad \text{Drain-source capacitance}

\( C_{GD} \)  \quad \text{Gate-drain capacitance}

\( C_{GD0} \)  \quad \text{Zero-bias/asymptotic gate-drain capacitance}

\( C_{GS} \)  \quad \text{Gate-source capacitance}

\( C_{GS0} \)  \quad \text{Zero-bias/asymptotic gate-source capacitance}

\( C_t \)  \quad \text{Transit time capacitance}

\( \partial I_X \)  \quad \text{Differential of the current } I_X \text{ }

\( \delta \)  \quad \text{Transition width parameter}

\( \Delta \)  \quad \text{Beyond-pinchoff capacitance interpolation voltage range}

\( \text{DCFL} \)  \quad \text{Direct Coupled FET Logic}

\( \text{DGMESFET} \)  \quad \text{Dual-Gate MESFET}

\( \text{DMESFET} \)  \quad \text{Depletion MESFET}

\( \varepsilon_{\text{GaAs}} \)  \quad \text{GaAs absolute dielectric constant}

\( \text{EMESFET} \)  \quad \text{Enhancement MESFET}

\( E_{\text{sat}} \)  \quad \text{Electron velocity saturation field}

\( E_{VGS} \)  \quad \text{Factor for } V_{GS} \text{ voltage source}

\( \text{Exp} \)  \quad \text{Gate voltage control expression exponent}

\( \phi_{Bl} \)  \quad \text{Schottky junction barrier height}

\( \text{FC} \)  \quad \text{Forward bias depletion capacitance coefficient}

\( F_D \)  \quad \text{Drain current error function}

\( \text{FET} \)  \quad \text{Field Effect Transistor}

\( F_G \)  \quad \text{Gate current error function}

\( F_S \)  \quad \text{Source current error function}

\( g_D \)  \quad \text{Intrinsic drain conductance}

\( g_m \)  \quad \text{Intrinsic transconductance}

\( \text{GaAs} \)  \quad \text{Gallium Arsenide}

\( G_D \)  \quad \text{Extrinsic drain conductance}
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_m$</td>
<td>Extrinsic transconductance</td>
</tr>
<tr>
<td>$G_{leak}$</td>
<td>Drain-source leakage conductance</td>
</tr>
<tr>
<td>$\eta$</td>
<td>ETA - subthreshold slope parameter</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction Bipolar Transistor</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>$I$</td>
<td>Current vector</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current</td>
</tr>
<tr>
<td>$I_{DS}$</td>
<td>Drain-source current</td>
</tr>
<tr>
<td>$I_{DSsat}$</td>
<td>Drain-source saturation current</td>
</tr>
<tr>
<td>$I_G$</td>
<td>Gate current</td>
</tr>
<tr>
<td>$I_{GD}$</td>
<td>Gate-drain current</td>
</tr>
<tr>
<td>$I_{GS}$</td>
<td>Gate-source current</td>
</tr>
<tr>
<td>$I_{inf}$</td>
<td>Schottky spreading resistance inflection current</td>
</tr>
<tr>
<td>$I_P$</td>
<td>Pinchoff current</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Source current, diode saturation current</td>
</tr>
<tr>
<td>$I_{Saux}$</td>
<td>Auxiliary diode saturation current</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction FET</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann’s constant</td>
</tr>
<tr>
<td>$K_1$</td>
<td>Capacitance model coefficients</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>LAMBDA - channel length modification coefficient</td>
</tr>
<tr>
<td>$L$</td>
<td>Gate electrode length</td>
</tr>
<tr>
<td>LSI</td>
<td>Large Scale Integration</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>Electron mobility</td>
</tr>
<tr>
<td>$M$</td>
<td>Capacitance grading coefficient</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>MISFET</td>
<td>Metal-Insulator-Semiconductor FET</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal-Organic Vapour Epitaxy</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor FET</td>
</tr>
<tr>
<td>MSI</td>
<td>Medium Scale Integration</td>
</tr>
<tr>
<td>$n$</td>
<td>Diode ideality parameter</td>
</tr>
<tr>
<td>$n_{aux}$</td>
<td>Auxiliary diode ideality parameter</td>
</tr>
<tr>
<td>$N$</td>
<td>Channel doping concentration</td>
</tr>
<tr>
<td>NMS</td>
<td>Nelder &amp; Mead Simplex</td>
</tr>
<tr>
<td>$p$</td>
<td>Non-dimensional channel potential</td>
</tr>
<tr>
<td>$q$</td>
<td>Electron charge</td>
</tr>
<tr>
<td>$Q_D$</td>
<td>Drain charge</td>
</tr>
<tr>
<td>$Q_{DS}$</td>
<td>Drain-source charge</td>
</tr>
<tr>
<td>$Q_S$</td>
<td>Source charge</td>
</tr>
<tr>
<td>$\rho$</td>
<td>Channel charge density</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>$R_B$</td>
<td>Bulk resistance</td>
</tr>
<tr>
<td>$R_G$</td>
<td>Gate resistance</td>
</tr>
<tr>
<td>$R_D$</td>
<td>Drain resistance, diode series resistance</td>
</tr>
<tr>
<td>$R_{DS}$</td>
<td>Drain-source (leakage) resistance</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced Instruction Set Computer</td>
</tr>
</tbody>
</table>
\( R_{rev} \) Reverse-biased gate diode resistance
\( R_s \) Source resistance
\( R_{SS\text{max}} \) Schottky spreading resistance maximum value
\( s \) Non-dimensional gate potential
\( \text{SBFL} \) SuperBuffer FET Logic
\( \text{SCFL} \) Source Coupled FET Logic
\( \text{SDFL} \) Schottky Diode FET Logic
\( \text{SPICE} \) Simulation Program with Integrated Circuit Emphasis
\( \tau \) Transit time for electrons under the MESFET gate
\( T \) Temperature
\( v_e \) Electron drift velocity
\( v_{sat} \) Saturated electron drift velocity
\( \vec{V} \) Voltage vector
\( V_0 \) Polynomial coefficient evaluation \( V_{DS} \) value
\( V_1 \) Voltage over linear region in channel
\( V_2 \) Voltage over saturation region in channel
\( V_{BL} \) Schottky barrier voltage
\( V_C \) Control voltage
\( V_D \) Drain voltage, diode voltage
\( V_{DS} \) Drain-source voltage
\( V_{DSat} \) Drain-source saturation voltage
\( V_{GS} \) Gate-source voltage
\( V_{GSi} \) Intrinsic gate-source voltage
\( V_{GS\text{new}} \) Modified gate-source voltage
\( V_{\text{incr}} \) Subthreshold increment voltage
\( \text{VLSI} \) Very Large Scale Integration
\( V_{\text{max}} \) Maximum forward bias
\( V_{\text{new}} \) Intermediate voltage
\( V_p \) Pinchoff voltage
\( V_{\text{sub}} \) Subthreshold starting gate-source voltage
\( V_{TH} \) Threshold voltage
\( W \) Gate electrode width
\( \text{Y} \) Conductance matrix
1. Introduction

Gallium arsenide devices have been widely used since the late 1960s for microwave applications, and they are still dominating this field. The use of GaAs for digital circuit applications began in the early 1970s, and it has developed over the years into a well-established LSI technology, with an increasing number of VLSI applications in recent years. Two examples of this are the GaAs supercomputer CRAY-3 under development at Cray Research [1], and the 32-bit GaAs RISC microprocessor designed at McDonnel Douglas [2]. Manufacturers of existing, silicon-based computer architectures are also starting to replace critical ICs like cache memories and disc controllers with plug-in compatible GaAs circuits in order to increase performance [3].

GaAs technology is still 2 - 4 times more expensive than silicon technology, depending on the complexity of the process in question, but its use is justified in applications that require very high speed and low power consumption. With the increasing volume of portable electronic equipment, from telephones to computers, the low power dissipation of certain GaAs logic families is making them very attractive for the systems designer.

The design of high-speed GaAs digital integrated circuits requires accurate models for the active devices and for the passive circuit elements. The activity in the modeling area has increased considerably along with the use of GaAs ICs, but the models used in GaAs circuit design still have a long way to go before they reach the level of sophistication and accuracy of existing silicon MOSFET or bipolar models. This lack of accurate and nonproprietary models for circuit simulation programs such as SPICE has been hampering the use of GaAs technology.

In recent years, however, a large number of GaAs MESFET models have been proposed, and some have been implemented in SPICE with far better results than the old, inadequate models. As the model complexity increases, however, it gets more difficult to extract the model parameters from measurement data, and it becomes necessary to resort to nonlinear optimization techniques. To meet this need, the program MESFETOPT was developed [4] at the Technical Research Centre of Finland (VTT), in the Semiconductor Laboratory during the NOGAP research project. MESFETOPT contains subroutines for the most popular GaAs MESFET models in use today, and it can measure I-V characteristics and extract model parameters from the measurement data. The program is also serving as a ‘test bench’ for the development of a new model.

This work concentrates on GaAs MESFET models and their use for digital integrated circuit design. The models are compared in terms of accuracy and computational speed. Parameter extraction and optimization methods are also treated. The development of a new model and its implementation into SPICE, together with the other presented models, is described.
2. GaAs transistors

2.1 The JFET and MESFET

Due to the fact that a high-quality native oxide does not form on GaAs as on silicon, it is very difficult to fabricate metal-insulator-semiconductor (MIS) devices on this material. Attempts using deposited dielectrics have failed because of the very high surface state density (\(10^{12} \text{ I/cm}^2\) or higher) of GaAs, which pins the Fermi level near the middle of the bandgap and prevents the inversion of the surface. The control electrode structure of a GaAs FET is therefore limited to either a pn junction (JFET) or a metal-semiconductor junction (MESFET). The cross-sections of these devices are shown in Figure 1.

**Figure 1.** Schematic cross-section of a) JFET, b) MESFET. Observe the normally-on depletion regions.

The conducting channel in these devices consists of an ion-implanted n'-region. p-type devices are not used, because the hole mobility in GaAs is very small, and the biggest advantage of GaAs devices over Si devices, speed, is achieved by exploiting the high electron mobility in GaAs at low electric fields.

The gate voltage of both the JFET and MESFET is constrained by the forward conduction of the respective gate junctions, which gets significant at gate voltages near and higher than the built-in gate voltages. For GaAs MESFETs, the built-in Schottky voltage is about 0.7 V for virtually all useful gate metals like Al, Au or Pt, while the p'\text{n'} junction voltage in a GaAs JFET can be as high as 1.4 V. However, the implanted p' region takes up a lot of space, and a pn junction has a larger capacitance than a metal-semiconductor junction and is thereby slower. Therefore, the MESFET currently is the most used GaAs transistor.
The first fabricated MESFETs were of *depletion* type. These DMESFETs are ‘normally on’ devices requiring a negative gate-source potential to deplete the carriers through the channel region and turn the device off. The negative voltage at which no current flows from the drain to the source is called the *pinchoff* voltage, $V_p$, and it is a function of the implanted channel depth and doping concentration. The built-in voltage of the Schottky gate, $V_{BI}$, also gives rise to a small depletion region without external biasing, so in practice the channel is pinched off already when $V_{GS}$ reaches the *threshold* voltage, $V_{TH}$, which is equal to $V_{BI} - V_P$. DMESFETs are the most mature and easiest GaAs transistors to produce in terms of fabrication techniques and IC yield.

By using a combination of thin channel and/or low doping concentration, it is possible to fabricate a device that is pinched off only by the built-in voltage of the Schottky gate. This is an *enhancement* MESFET (EMESFET), for which a positive gate potential must be applied in order to start drain-source conduction. An enhancement JFET can be fabricated in a similar way. The cross-section of an enhancement MESFET is shown in Figure 2.

![Figure 2. Schematic cross-section of an enhancement MESFET. Observe the normally-off depletion region.](image)

An additional complication with the use of EMESFETs is that the surface states between the gate electrode and the source contact give rise to a depletion region that tends to pinch off the lightly doped channel. This leads to a higher parasitic source resistance that degrades the transconductance. The effect can be avoided by using either a recessed gate or a self-aligned gate process, both of which make the...
fabrication more complex and difficult. In a recessed gate process the gate is recessed into the GaAs surface by etching into a slightly thicker channel region. In a self-aligned gate process the gate acts as a mask for the source and drain implants, and so the final distance between the gate electrode and the source and drain contacts is minimized. However, a refractory silicide, such as WSi₂, must be used instead of the usual Al or Ti/Pt/Au gate in order to avoid Schottky barrier degradation during the high-temperature implantation annealing. Most manufacturers of ICs containing EMESFETs today use either a self-aligned gate process or a combined, recessed and self-aligned gate process.

2.2 The HFET and HBT

While the JFET and the MESFET can be fabricated using the same processes and equipment as in standard silicon technology, the high electron mobility transistor (HEMT) and the heterojunction bipolar transistor (HBT) require more sophisticated fabrication methods. Techniques like molecular beam epitaxial growth (MBE), metal-organic chemical vapour deposition (MOCVD) or atomic layer epitaxy (ALE) [5] are needed to produce the very thin semiconductor layers in these devices. Mainly because of the slow and difficult processing their use has not yet become commercially attractive.

The new processing techniques for making very thin semiconductor layers of high quality has opened up possibilities for a whole new group of semiconductor devices, of which the HEMT and the HBT are so far the most promising. The dominant theme for these new devices is ‘bandgap engineering’ through the use of the heterojunction, an abrupt or intentionally graded junction between two semiconductors of different bandgap [6]. This makes it possible to control the force acting on electrons and holes independently by adjusting both the bandgap and the doping.

The structure of a typical HEMT is shown in Figure 3. It consists of a thick layer of undoped GaAs covered with a thin (~ 70 nm) n⁺ AlGaAs layer, which serves to furnish the electrons for the channel and also acts as a gate insulator, although the gate will begin to conduct at a gate voltage above 0.9 - 1.1 V, depending on the AlGaAs doping concentration. The n⁺ GaAs layer under the source and drain improves the contacts.

![Figure 3. Schematic cross-section of a HEMT structure.](image-url)
The channel is based on the abrupt junction between the wide bandgap AlGaAs and the narrow bandgap GaAs layers. The electrons will move from the AlGaAs layer to the surface of the GaAs layer and collect there in a potential well. The layer of electrons is typically only 10 nm thick, so it will form a so-called two-dimensional electron gas, where the electron mobility along the junction is very high due to the lack of impurity scattering. Values of about 8500 \( \text{cm}^2/\text{Vs} \) at room temperature and 50000 \( \text{cm}^2/\text{Vs} \) at 77 K have been achieved, as compared with typical GaAs MESFET channel mobilities of 4000 - 5000 \( \text{cm}^2/\text{Vs} \) at room temperature. This gives the HEMT a fast ‘turn-on’ characteristic, that is, it develops nearly its full transconductance with gate logic swings only a small amount, about 200 mV, above threshold. The dynamic switching energies of HEMT logic are 1 - 2 orders of magnitude lower than those of MESFET logic, which is the key driving force behind present research in this technology. The low noise figure of the HEMT makes it useful for microwave applications, but threshold voltage control problems inhibit its use for digital circuits. Indeed discrete HEMTs are today fabricated and sold mostly for microwave circuit applications, but so far there are no semiconductor companies offering foundry services for HEMT IC processing.

In a HBT structure shown in Figure 4., the emitter consists of n-type AlGaAs, the base of p-type GaAs and the collector of n-type GaAs.

![Figure 4. Schematic cross-section of a HBT structure.](image)

The use of a wide bandgap n-type AlGaAs emitter allows the doping level in the p\(^+\) GaAs base region to be made very high without degrading the current gain, since hole injection from the base into the wider bandgap emitter is virtually impossible. Because of the high base doping levels, the base width can be very small, less than 0.1 \( \mu \text{m} \), which results in short electron transit times through the base. If the emitter resistance also can be made very low, the HBT will perform extremely well in a high-speed digital circuit. Devices with maximum operation frequencies of 105 GHz have been reported [7]. Another advantage of HBT technology is that the threshold voltage is determined strictly by the inherent bandgap of the GaAs and AlGaAs layers, which varies very little compared to the channel thickness and doping concentration of GaAs FETs. Threshold uniformities of a few millivolts over a wafer are typically achievable. For this reason the HBT is perhaps a more suitable candidate for very high-speed LSI and VLSI circuits than the HEMT.
3. GaAs MESFET characteristics

The operation of any FET is characterized by several regions of operation which are illustrated in Figure 5. They are the linear or ohmic region, saturation region, cutoff, subthreshold region and inverse region.

In the linear region, the drain current increases linearly with $V_{DS}$ for a given $V_{GS}$ value. This linearity is however limited to rather small values of $V_{DS}$ due to the voltage drop along the channel. The bias on the gate-channel junction will become more reverse biased at the drain end of the channel than at the source end as $V_{DS}$ is increased, and the slope of the I-V curve will decrease gradually. This slope, the small-signal drain-source conductance, is defined by

$$g_{DS} = \frac{dI_{DS}}{dV_{DS}}|_{V_{GS} = \text{constant}}$$  \hspace{1cm}(1)$$

When $V_{DS}$ reaches the saturation voltage, $V_{DSat}$, the drain current ‘flattens out’ and remains relatively constant for further increases in $V_{DS}$. $V_{DSat}$ is a function of $V_{GS}$ in such a way that I-V curves for more negative $V_{GS}$ will saturate at smaller $V_{DS}$ values, because the depletion region extends deeper into the channel. The behaviour of a MESFET in the saturation region can be explained in two common ways. The classical explanation is the gradual channel model, which attributes the current saturation to the pinching off of the drain end of the channel [8]. The second explanation is the velocity saturation model, which takes into account the saturation of the electron velocity at high electric fields [9,10].

**Figure 5.** Regions of operation for a FET.
These two models yield different I-V characteristics for the same set of parameters. The saturation voltage will be smaller and much less dependent on $V_{GS}$ in the velocity saturation model than in the gradual channel model. The drain current in saturation will also be smaller for the velocity saturation model, because in this model the electron velocity is limited. The actual mechanism resulting in drain current saturation may be thought of as a combination of the two common models, and the properties of the FET in question - mainly the gate length versus the channel thickness - will determine which model fits the I-V characteristics best. The theory behind the gradual channel model and the velocity saturation model will be presented in chapters 8.4 and 8.9, respectively.

The small drain current increase with $V_{DS}$ in the saturation region can be attributed to channel length modulation; the pinch-off point or the velocity saturation point moves toward the source as $V_{DS}$ is increased. If the gradual channel explanation is applicable, then the current increase is attributed to an increase in electron velocity due to higher electric field in the region between the source and the pinch-off point. When the velocity saturation model is appropriate, the channel voltage at the velocity saturation point will decrease as the point moves toward the source. Therefore, the depletion layer depth will also decrease at this point, yielding an increase in the conducting area, so the drain current will also increase.

Another small-signal model parameter, the transconductance $g_m$, is of importance to the MESFET. The transconductance is defined by

$$g_m = \frac{dI_{DS}}{dV_{GS}}_{V_{DS} = \text{constant}}$$

(2)

The transconductance is significant because it relates the increase in $I_{DS}$ to and increase in the control voltage of the FET, $V_{GS}$. Thus, it is closely related to the gain of the device, which is an important quantity both for analog and digital circuit applications.

Subthreshold current is the residual leakage current that flows from drain to source when $V_{GS}$ is biased more negatively than $V_{TH}$. Pinchoff or cutoff is really a transition between a region of normal conduction dominated by drift of free electrons in the device channel and a region of subthreshold conduction in which electrons are transported by diffusion and drift. The resulting current is an exponential function of $V_{GS}$ and $V_{DS}$.

In addition to the device leakage current beyond pinchoff there is also leakage current through the substrate which occurs due to injection of charge from a forward-biased contact. At moderate drain-source voltages this current is predominantly ohmic, and can be modeled simply by placing a large resistor between the drain and the source. Subthreshold models are further discussed in chapter 8.11.

In the inverse region, the roles of the source and drain become reversed, and $V_{GD}$ becomes the controlling voltage. It is important to understand that the inverse I-V characteristics depicted in Figure 5. can be obtained only by interchanging the source
and the drain, not by just making the drain voltage negative with respect to the source. In this case, if the gate voltage is not also changed correspondingly, the control voltage will be quite different from the positive drain voltage case, and at some point forward gate-drain conduction will begin and the I-V characteristics will be severely distorted.

Unfortunately, the behaviour of the MESFET also includes a number of second-order effects, which are quite difficult to model. The most important of these effects are:

1. Backgating
2. Drain lag effects
3. Temperature dependence

Backgating or sidegating is a widely reported effect [11,12] in which the drain current of a MESFET is reduced by the presence of other nearby neighbouring FETs which happen to be biased negatively with respect to the source of the first device. Because FETs are laid out side by side in a circuit, the applied voltage is sometimes referred to as the sidegate voltage. This effect can have a very strong influence on the I-V characteristics, as shown in Figure 6.

**Figure 6.** Sidegating characteristics of two 1 x 20 μm depletion MESFETs fabricated at the VTT Semiconductor Laboratory [13]. In a) and b), no sidegate voltage is applied, and $V_{GS}$ is swept from 0.0 to -1.0 V. In c) and d), $V_{GS}$ is held at zero volts, and the voltage of the sidegate electrode is swept instead, having an equally strong effect on the drain current. The two devices differ in the position of the sidegate electrode (B), shown by the simplified layouts in c) and d).
The cause of this effect is that the substrate, when becoming more negatively biased than the source, will act as a second gate and deplete the channel from the backside. The same kind of phenomenon is known for MOSFETs, for which it is called the body effect and accounted for in all accurate MOSFET models. This is possible because of the relatively large conductivity of the silicon substrate, which yields a known substrate potential. For the GaAs MESFET, due to the high resistivity of the substrate, the potential is not well known and depends on other FETs in the local environment on the surface of the wafer. The situation is aggravated by the fact that the backgating characteristics for the same circuit can vary significantly between wafers cut from different GaAs ingots, or even from the ends of the same ingot. Backgating is a big problem especially for GaAs LSI and VLSI circuits, because it increases as the spacing between devices is reduced.

The modeling of this effect is difficult also because it is very dependent on the circuit layout. However, for comparatively small circuits like logic gates, it is feasible to add a voltage-dependent voltage source to the gate electrode of the MESFET, and use this voltage source to model the increase in the threshold voltage of the FET caused by backgating. This method is explained in detail in [14].

The drain lag effect refers to the tendency for the drain current to overshoot and recover slowly - during 10-100 µs - from a step change in $V_{DS}$. Another manifestation of this effect is observed in the frequency domain; the small-signal output conductance, $g_{DS}$, in the saturation region increases with frequency by as much as a factor of three. This effect occurs between 100 Hz and 1 MHz at room temperature, but only when the device is biased in the saturation region.

![Figure 7](image_url)  
*Figure 7.* Output resistance (the inverse of $g_{DS}$) of a $1 \times 300 \, \mu m$ GaAs DMESFET as a function of frequency [15].
The effect can be explained by the presence of slow, deep-level traps in the semi-insulating substrate below the channel [16]. The effect only shows in the saturation region because of the electron accumulation and high electric fields that are present only in this region of operation. The AC I-V characteristics of a MESFET will therefore be different from the DC characteristics measured with a curve tracer or parameter analyzer, which makes circuit simulation difficult. Also, because the effect only shows in the saturation region, the behaviour of a logic gate may be different depending on whether its input is changing from low to high or high to low.

Drain lag can be modeled quite accurately by adding two parasitic MOSFETs [16] or a RC network [17,18] to the MESFET equivalent circuit. However, the simulation time will increase significantly, and just like for backgating, there are large differences between devices fabricated on different GaAs wafers. It has been shown that the drain lag effect can be eliminated by new device structures [19] or designed away by using feedback techniques [20].

The temperature dependence of the MESFET drain current is influenced by two related mechanisms; the variation of the built-in voltage of the channel/substrate interface and the variation in the electron mobility. The first mechanism will make the threshold voltage, $V_{TH}$, more negative with increasing temperature, and it will also increase the effective thickness of the channel. Because $g_m$ is inversely proportional to the effective channel thickness, $g_m$ will decrease. This second mechanism, the decrease of electron mobility with increasing temperature, will also contribute to this effect. The total effect on the drain current is dependent on the relative strengths of these two mechanisms. Additionally, the behaviour of the MESFET Schottky barrier gate also changes with temperature.

While it is possible to incorporate these temperature dependencies into the model equations, as has actually been done for some simulators containing MESFET models, it is often more convenient and just as effective to use separate model parameter sets for low, nominal and high temperatures. Using these parameter sets the circuit can be analyzed in a worst-case manner to ensure error-free operation in the specified temperature range.

A more demanding task is to take into account self-heating or heating by the surrounding devices during operation. This may be important for power circuits, for example amplifiers, or for high-speed digital circuits with a very tight layout. Again, the situation is very layout-dependent, and so it is difficult to develop a general method. An effort to model the temperature-dependent output conductance with respect to self-heating can be found in [18].
4. GaAs MESFET digital logic

The principal devices used in GaAs MESFET digital integrated circuits are the MESFET and the Schottky barrier diode. Diodes are used both for non-linear logic elements and for voltage level shifting. Logic diodes are designed to have low series resistance and low capacitance, while level shifting diodes also have low series resistance but relatively high capacitance, because this increases the displacement current in the diode, which is beneficial for the operation of high-speed circuits. A quite large number of different GaAs MESFET logic families have been proposed, and the most mature of these are the following:

Depletion mode logic circuits
- Buffered FET logic, BFL
- Schottky diode FET logic, SDFL
- Capacitor-diode FET logic, CDFL
- Source coupled FET logic, SCFL

Enhancement/depletion (E/D) mode logic circuits
- Direct coupled FET logic, DCFL
- Superbuffer FET logic, SBFL
- E/D buffered FET logic, E/D BFL

All these logic families belong to a category called static logic, in which direct current flows at all times from the power supply. Properties like logic levels and noise margins are controlled by varying the width ratios of the MESFETs in the logic circuit, hence the term ratioed logic is often used. There is another type, dynamic logic, that has the potential to yield faster operation, lower power dissipation and increased circuit density compared to static logic. A dynamic circuit performs logic functions by the storage and evaluation of charge on circuit nodes which can be isolated temporarily from the rest of the circuit. Logic levels are not established through width ratios, but by clock signals and device threshold voltages; hence dynamic circuits are often described as being nonratioed. So far, dynamic circuits have been used almost only for frequency dividers [21,22]. A presentation of these circuits is beyond the scope of this work; the interested reader is referred to [23].

When selecting the type of static logic to be used for a certain application, it is necessary to consider at least the following properties of the available logic families:

- propagation delay → speed
- power dissipation
- noise margins
- fan-in and fan-out capability
- logic gate complexity → circuit area, fabrication yield

Of course, several different types of logic may be used in a circuit to perform those functions that suit their respective characteristics best. In designing the circuits for a given logic family, however, the biggest problem is usually to maximize speed and minimize power dissipation. This is possible to some extent by allowing the noise
margins to decrease. Therefore, it is important to design the layout of a high-speed low-power circuit in such a way that internal noise source are minimized. These include crosstalk-producing mutual inductance and capacitance, inductive and resistive voltage spikes, and voltage drops on power supply and ground lines.

In the following, three important GaAs logic families will be presented: BFL, SDFL and DCFL logic.

### 4.1 Buffered FET logic

The first significant GaAs ICs reported [24] utilized DMESFETs in a circuit design later called buffered FET logic (BFL) [25]. Schematics for inverter, NOR and NAND implementations of BFL logic are shown in Figure 8.

![Figure 8. BFL a) inverter, b) NAND gate, c) NOR gate implementations.](image)

This type of logic typically uses depletion mode MESFETs with a threshold voltage in the range -2.5 ... -1.0 V and hence requires two power supplies with typical voltages of 2.5 and -2.0 V, respectively. Since a negative gate voltage is required to
turn off a DMESFET, and its drain voltage is positive, level shifting must be introduced at some point so that the output logic levels match the input levels. In BFL circuits, this is accomplished by placing two or three level shifting diodes in the source follower output stage of every gate. The diodes are always forward biased, each one giving a voltage drop of about 0.8 V.

In Figure 8.b a NAND gate is realized by stacking two MESFETs. In this type of circuit, however, the logic low level will be degraded by the combined series resistance of the stacked devices, and this prevents the use of more than two series FETs. To reduce this effect it is common practice to combine the two devices into one with a single channel implant and two gates located close together. This is a dual-gate MESFET (DGMESFET) which has a lower parasitic series resistance and takes up less layout area than two stacked FETs.

BFL gates are fast, have good fan-out capability and large noise margins, but they consume a lot of power, typically 10 - 40 mW per gate. By lowering the threshold voltage of the MESFETs to -1 V and below, and by using only one level shifting diode it is possible to achieve power levels of about 5 mW per gate. However, this strategy will decrease the logic voltage swing and thereby the noise margins. Because other GaAs MESFET logic families can operate at even lower power levels, BFL logic applications will probably be limited to MSI and low-level LSI implementations of circuits with speed requirements of 3 - 4 GHz and above.
4.2 Schottky diode FET logic

The Schottky diode FET logic (SDFL) approach retains the high speed of the BFL approach, while providing a reduction in power dissipation of up to an order of magnitude. SDFL utilizes clusters of small, low series resistance and capacitance Schottky logic diodes to perform the logical positive OR function on groups of inputs, which may then be further processed with the normal MESFET logic functions. Figure 9. shows SDFL schematic diagrams for a NOR gate and a OR/NAND gate.

![SDFL Gate Diagrams](image)

**Figure 9.** SDFL gate configurations: a) NOR gate, b) OR/NAND gate realized with a DGMESFET in the inverter stage.

The SDFL circuit approach also saves circuit area compared to BFL gates, due to the replacement of large comparatively MESFET with very small (typically 1 x 2 μm) Schottky diodes for most logic functions. However, SDFL gates are slower and have lower fan-out capabilities than BFL gates.
4.3 Direct coupled FET logic

The first, simplest and most widely used enhancement/depletion mode GaAs logic family is the direct coupled FET logic (DCFL) circuit. Schematics of a DCFL inverter and NOR gate are shown in Figure 10.

![Figure 10. Schematics of DCFL a) inverter, b) 3-input NOR gate.](image)

The DCFL inverter consists only of an EMESFET connected to the power supply via a pull-up DMESFET. This configuration is very similar to that of E/D NMOS logic circuits. Since the EMESFET begins to conduct at gate voltages above zero volts, no level shifting is needed. Also, the saturation voltage, $V_{DS_{sat}}$, of an EMESFET is less than that of a DMESFET, which means that power supply voltages can be lower for enhancement mode circuits than their depletion mode equivalents. These properties can result in considerable reductions in power dissipation and circuit area. DCFL logic gates can achieve power dissipation figures of 0.1 ... 0.5 mW while functioning at clock frequencies up to 1.5 GHz. However, the fan-out capabilities and noise margins are rather low for this type of logic. The typical worst-case noise margins of DCFL gates is 200 mV or less, which is why it is not advisable to implement DCFL NAND gates with stacked EMESFETs in the same way that BFL NAND gates can be realized, Figure 8.b. The small noise margins are a result of the limited logic swing of about 0.5 V, due to the forward conduction of the EMESFET gate at higher voltages. This means that the uniformity of the devices, especially with respect to the threshold voltage, needs to be very good. One requirement for increasing the integration level of DCFL circuits further is therefore a more accurate modeling of the MESFETs, especially in terms of subthreshold behaviour and forward gate conduction characteristics.

In spite of the problems associated with DCFL circuit logic, gate arrays containing up to 200 000 ‘raw’ gates have recently been announced. The arrays use a combination of DCFL and superbuffer gates.
5. The SPICE program

5.1 SPICE capabilities

SPICE, which stands for Simulation Program with Integrated Circuit Emphasis, is a general-purpose circuit simulation program developed at the University of California at Berkeley for nonlinear DC, nonlinear transient and linear AC analyses [26]. The first version of this program dates back to 1973, and since then a large number of different versions have been developed, some with new capabilities like Monte Carlo analysis, digital element simulation and nonlinear optimization. However, the basic structure of the program and the input format have remained essentially the same, and today SPICE is the de facto standard in circuit simulation.

The original version of SPICE was capable of analyzing circuits containing the following elements: Resistors, capacitors, inductors, independent and dependent voltage and current sources, transmission lines, and the four most common semiconductor devices - diodes, BJTs, JFETs and MOSFETs. The models for these elements have since then been improved upon considerably, and new elements have been added, for example switches and GaAs MESFETs.

Each type of component is analyzed in SPICE by its own subroutine. The component is defined in terms of a lumped model including resistors, capacitors and voltage-dependent current sources. The behaviour of the model is determined by the model parameters, which have to be specified by the user in the input file. Thus, the accuracy of the simulation depends on two factors: The accuracy of the device model equations, and the validity of the given model parameters. The model equations must be a compromise between accuracy and excessive computation time. Finding a valid parameter set for a very complex model can also be quite difficult, so even if the model could reproduce the device behaviour very accurately, nobody might want to use it. However, the penalty of slow program execution can be acceptable for the accurate evaluation of comparatively small ‘building blocks’ like logic gates, and also for worst case path analysis of large designs.

SPICE is node-voltage oriented, so any node voltage in the circuit can be requested. Element currents flowing through independent voltage sources can also be requested. Tabular lists and printer plots are available, and some of the newer SPICE versions offer graphical postprocessor programs that can display the simulation data as graphs on the computer screen.

5.2 DC analysis

The DC analysis portion of SPICE determines the DC operating point of the circuit with capacitors opened and inductors shorted. The analysis is performed by applying the Kirchhoff current law on the circuit nodes,

\[ \mathbf{Y} \cdot \mathbf{V} = \mathbf{I} \]

(3)

where \( \mathbf{V} \) and \( \mathbf{I} \) are the voltage and current vectors, respectively, and \( \mathbf{Y} \) is the conductance matrix for the circuit. This matrix is constructed by assuming initial
values for the node voltages and calling the individual device subroutines to calculate branch currents and conductances for the initial voltages. Each routine calculates its own currents and conductances using a linearized model for its initial voltages, and adds them to the $\mathbf{Y}$ matrix and $\mathbf{I}$ vector. A linearized model is meaningful only if all the derivatives of branch currents with respect to branch voltages are defined at all points. This means that the device models in the simulator must not contain discontinuities, because then the convergence of the analysis can be severely hampered.

After this phase is completed, new node voltages are produced from Eq. (3) by a matrix inversion. The process is repeated until convergence is achieved, i.e. Eq. (3) is satisfied to the wanted accuracy. This is, of course, a simplified account of the analysis; there are special routines to handle difficult cases, and different SPICE versions usually have their own ‘bag of tricks’ to overcome convergence problems.

### 5.3 AC analysis

The AC small-signal portion of SPICE computes the AC output variables as a function of frequency. The program first computes the DC operating point of the circuit and determines linearized, small-signal models for all the nonlinear devices in the circuit. The resultant linear circuit is then analyzed over a user-specified range of frequencies. In this analysis, all input sources are sinusoidal with the same input frequency, although sources may be assigned different values of relative phase.

The equations for a linear AC analysis are assembled by the same method used for the DC analysis, except for the fact that the equations are complex for AC analysis. This results in a system of equations similar to (3) which can be solved using similar techniques.

### 5.4 Transient analysis

Transient analysis is performed to determine the time domain response of a circuit over a specified time interval $[0, T]$. The initial conditions are automatically determined by a DC analysis. All sources that are not time dependent, for example power supplies, are set to their dc value. For large signal sinusoidal simulations, a Fourier analysis of the output waveform can be specified to obtain the frequency-domain Fourier coefficients.

The transient solution is determined computationally by dividing the time interval $[0, T]$ into discrete time points $[0, t_1, t_2, ..., T]$. At each time point, a numerical integration algorithm is employed to transform the differential model equations of energy storage elements into equivalent algebraic equations. After this transformation, the solution is determined iteratively in the same fashion as the nonlinear DC operating point.

The way the equations for the semiconductor devices are implemented can give rise to charge nonconservation problems in transient analysis. As explained above, it is necessary during the analysis to compute the charges associated with each of the terminals of the nonlinear circuit elements. Usually, it is easier to express the terminal
capacitances as functions of the nonlinear element terminal voltages. Thus, if only capacitance equations are available, then the charges are obtained through the numerical approximation

\[ Q = \int C(V_x) dV_x \]  \hspace{1cm} (4)

However, in this case the charges will be path dependent, that is, even if the voltage starts at a particular value and ends at the same value, the computed charge will be different if the intermediate voltages are different. This discrepancy increases even more when the nonlinear capacitances are not controlled only by their terminal voltages alone. Charge conservation and continuity can be very important for the behaviour of certain types of logic circuits, for example dynamic logic circuits, where charge storage on an isolated node is the central design principle. It is also important for circuit using pass transistors. Hence, models that give the capacitances as functions of the voltages will yield erroneous simulation results for these circuits.

The problem can be avoided by using analytical charge equations for the nonlinear circuit elements instead of capacitance equations. In this case, the capacitances are obtained by analytical derivation of the charge equations:

\[ C = \frac{\partial}{\partial V_x} Q(V_x) \]  \hspace{1cm} (5)

This approach is perhaps more complicated, but it avoids all charge nonconservation problems and is physically more correct than the method represented by Eq. (4).
6. The MESFETOPT program

The computer program MESFETOPT was developed for the extraction and optimization of MESFET model parameters, data storage and curve plotting. It contains all the GaAs MESFET channel current, gate diode and capacitance models presented in this work. Routines for the measurement of I-V characteristics using the Hewlett-Packard 4145A Semiconductor Parameter Analyzer are also included. The program is interactive and forms a complete environment for performing measurements and model parameter extraction and optimization for GaAs MESFETs.

The program runs on Hewlett-Packard desktop computers and workstations equipped with HP BASIC, version 5.1. This language uses structures similar to those in Pascal combined with FORTRAN-style subroutines and common blocks. The eight byte precision REAL numbers make it possible to perform mathematical calculations without loss of accuracy. The language is very versatile and easy to use, but suffers from almost nonexistent portability to other types of computers. However, the excellent mathematical, graphics and IEEE-488 bus control routines that it offers makes it very useful for device measurement and modeling. New algorithms can easily be tested and debugged before implementation in a more portable but also more difficult programming language, for example C.

At this time, the program consist of about 7000 lines of BASIC code, so it is fairly complicated. Figure 11. shows a simplified block diagram of the program.

![Block diagram of the MESFETOPT program and the peripherals.](image)

Universities and research institutions outside of Finland have expressed some interest in the program, and copies of it have therefore been given to about 20 sites, most of these in USA.
7. General device DC analysis theory

The basic difficulty in modeling semiconductor devices is that they are extremely complex internally and simple external models cannot accurately describe their behaviour under all conditions. Some device characteristics will have to be ignored or drastically simplified in order to keep the model evaluation time reasonably short. On the other hand, even relatively simple equations for the currents in a FET are not easy to solve, because the intrinsic voltages are functions of the currents, and vice versa. Figure 12 shows a self-aligned MESFET, where the gate has been used as a mask for the strongly doped n⁺ regions under the drain and source electrodes.

![Figure 12](image)

**Figure 12.** A schematic cross-section of a self-aligned MESFET, with parasitic source, gate and drain resistances marked.

Although the gate-source and gate-drain distances are almost zero, there is still some resistance - or channel current mechanisms that can be modeled as resistance - between the channel and the electrodes. There is also some resistance in the gate metal layer and at the gate Schottky junction. An accurate model must include these resistances, and this automatically makes the model non-analytical; the model equations have to be solved by iteration.

Another problem with simulating the MESFET is the fact that the gate is a Schottky diode, which begins to conduct significantly if the junction potential reaches about 0.7 V. To simulate a device like this, it is therefore necessary to consider three currents, namely the gate-source, gate-drain, and drain-source currents.

The most used method for DC analysis is **nodal analysis**, where the node voltages are the unknown circuit variables, and this method is also used in SPICE. However, in the developed computer program MESFETOPT a different method is used, where the **currents** between the nodes are the variables. Figure 13 shows the complete set of voltages and currents for the GaAs MESFET, excluding substrate currents.
Figure 13. MESFET voltages and currents. The current directions shown here are used in the equations throughout this chapter.

With the current directions as in Figure 13., the intrinsic voltages can be written as:

\[ V_{GS} = V_G - V_S - I_S R_S - I_G R_G \]  \hspace{1cm} (6)
\[ V_{GD} = V_G - V_D - I_D R_D - I_G R_G \]  \hspace{1cm} (7)
\[ V_{DS} = V_D - V_S + I_D R_D - I_S R_S \]  \hspace{1cm} (8)

On the other hand, the currents are functions of the voltages as follows:

\[ I_G = I_{GS}(V_{GS}) + I_{GD}(V_{GD}) \]  \hspace{1cm} (9)

**If** \( V_D - V_S \geq 0 \):

\[ I_D = I_{GD}(V_{GD}) - I_{DS}(V_{GS}, V_{DS}) \]  \hspace{1cm} (10)
\[ I_S = I_{GS}(V_{GS}) + I_{DS}(V_{GS}, V_{DS}) \]  \hspace{1cm} (11)

**If** \( V_D - V_S < 0 \):

\[ I_D = I_{GD}(V_{GD}) - (-I_{DS}(V_{GD}, |V_{DS}|)) \]  \hspace{1cm} (12)
\[ I_S = I_{GS}(V_{GS}) + (-I_{DS}(V_{GD}, |V_{DS}|)) \]  \hspace{1cm} (13)

The functions \( I_{GS} \) and \( I_{GD} \) are usually the same for positive and negative values of \( V_{GS} \) and \( V_{GD} \) (forward and reverse diode characteristics). If one desires to model these regimes of operation with different equations, the used functions and their first-order derivatives must be continuous at \( V_{GS} = 0 \) and \( V_{GD} = 0 \).

In order to solve these three equations, it is necessary to rewrite the expressions into three error functions, which must be minimized in order to find a solution: a set of voltage and current values that satisfy Eqs. (6) - (8) to the desired precision. The functions represent the summing of current contributions at each node, according to the Kirchoff current law, and they are the following:
\[ F_G = I_G - I_{GS} - I_{GD} \]  \hspace{1cm} (14)
\[ F_D = I_D - I_{GD} + I_{DS} \]  \hspace{1cm} (15)
\[ F_S = I_S - I_{GS} - I_{DS} \]  \hspace{1cm} (16)

Since there are three currents, the value of each current depending on the values of the other two, the problem consists of solving a system of three nonlinear simultaneous equations. The solution to such a system is obtained by an iterative sequence of linearized solutions. The Newton-Raphson algorithm is the most common method of linearization. This method can generally be expressed, using matrix notation, as

\[ \bar{F}(\bar{x}_{i+1}) = \bar{F}(\bar{x}_i) + \frac{\partial}{\partial \bar{x}_j} \bar{F}(\bar{x}_i) (\bar{x}_{i+1} - \bar{x}_i) = 0 \]  \hspace{1cm} (17)

which, in this particular case of three equations and three unknowns becomes

\[
\begin{bmatrix}
\frac{\partial F_1}{\partial x_1} & \frac{\partial F_1}{\partial x_2} & \frac{\partial F_1}{\partial x_3} \\
\frac{\partial F_2}{\partial x_1} & \frac{\partial F_2}{\partial x_2} & \frac{\partial F_2}{\partial x_3} \\
\frac{\partial F_3}{\partial x_1} & \frac{\partial F_3}{\partial x_2} & \frac{\partial F_3}{\partial x_3}
\end{bmatrix}
\begin{bmatrix}
x_1(i+1) - x_1(i) \\
x_2(i+1) - x_2(i) \\
x_3(i+1) - x_3(i)
\end{bmatrix}
= \begin{bmatrix}
-F_1(i) \\
-F_2(i) \\
-F_3(i)
\end{bmatrix}
\]  \hspace{1cm} (18)

where the functions \( F_n \) and their partial derivatives \( \partial F_n/\partial x_n \) are evaluated at points \( x_n(i) \). Here, the goal is to get \( F_n(i+1) \) equal to zero, hence only \( F_n(i) \) appears in the result matrix. The matrix containing the partial derivatives of the error functions is the Jacobian. By solving this equation for \( x_n(i+1) \) one obtains the new values to be used in the iteration. However, first the values of the derivatives must somehow be calculated. As long as the functions are not too complicated, this can be done analytically.

In this case \( F_1 = F_G, F_2 = F_D, F_3 = F_S \), and \( x_1 = I_G, x_2 = I_D, x_3 = I_S \). Taking the partial derivatives of the functions \( F_G, F_D, \) and \( F_S \) with respect to \( I_G, I_D, \) and \( I_S \), we get the following expressions:

\[
\frac{\partial F_G}{\partial I_G} = 1 - \frac{\partial I_{GS}}{\partial I_G} - \frac{\partial I_{GD}}{\partial I_G} \]  \hspace{1cm} (19)
\[
\frac{\partial F_G}{\partial I_D} = -\frac{\partial I_{GS}}{\partial I_D} - \frac{\partial I_{GD}}{\partial I_D} \]  \hspace{1cm} (20)
\[
\frac{\partial F_G}{\partial I_S} = -\frac{\partial I_{GS}}{\partial I_S} - \frac{\partial I_{GD}}{\partial I_S} \]  \hspace{1cm} (21)
\[
\frac{\partial F_D}{\partial I_G} = -\frac{\partial I_{GD}}{\partial I_G} + \frac{\partial I_{DS}}{\partial I_G} \]  \hspace{1cm} (22)
\[
\frac{\partial F_D}{\partial I_D} = 1 - \frac{\partial I_{GD}}{\partial I_D} + \frac{\partial I_{DS}}{\partial I_D} \]  \hspace{1cm} (23)

\[
\text{In this case } F_1 = F_G, F_2 = F_D, F_3 = F_S, \text{ and } x_1 = I_G, x_2 = I_D, x_3 = I_S. \text{ Taking the partial derivatives of the functions } F_G, F_D, \text{ and } F_S \text{ with respect to } I_G, I_D, \text{ and } I_S, \text{ we get the following expressions:}
\]
Considering Eqs. (6), (7), and (8) the derivatives in the right-hand side of the above equations can now be evaluated. Without knowing the exact mathematical expressions used in the functions for $I_{GD}$, $I_{GS}$, and $I_{DS}$, we can still write the final results in a general form as:

\[
\begin{align*}
\frac{\partial F_D}{\partial I_S} &= -\frac{\partial I_{GD}}{\partial I_S} + \frac{\partial I_{DS}}{\partial I_S} \\
\frac{\partial F_S}{\partial I_G} &= -\frac{\partial I_{GS}}{\partial I_G} - \frac{\partial I_{DS}}{\partial I_G} \\
\frac{\partial F_S}{\partial I_D} &= -\frac{\partial I_{GS}}{\partial I_D} - \frac{\partial I_{DS}}{\partial I_D} \\
\frac{\partial F_S}{\partial I_S} &= 1 - \frac{\partial I_{GS}}{\partial I_S} - \frac{\partial I_{DS}}{\partial I_S}
\end{align*}
\]  

(24) (25) (26) (27)

The three equations above are valid on the condition that $I_{GS}$ and $I_{GD}$ are functions of $V_{GS}$ or $V_{GD}$, but not of both voltages.

If $V_D - V_S \geq 0$ ($g_m \geq 0, \ g_D \geq 0)$:

\[
\begin{align*}
\frac{\partial F_D}{\partial I_G} &= 1 + R_G \left( \partial I_{GS} + \partial I_{GD} \right) \\
\frac{\partial F_D}{\partial I_D} &= R_D \partial I_{GD} \\
\frac{\partial F_D}{\partial I_S} &= R_S \partial I_{GS}
\end{align*}
\]  

(28) (29) (30)

\[
\begin{align*}
\frac{\partial F_D}{\partial I_D} &= R_G \left( \partial I_{GD} - g_m \right) \\
\frac{\partial F_D}{\partial I_D} &= 1 + R_D \left( \partial I_{GD} + g_D \right) \\
\frac{\partial F_D}{\partial I_S} &= -R_S \left( g_m + g_D \right) \\
\frac{\partial F_S}{\partial I_G} &= R_G \left( \partial I_{GS} + g_m \right) \\
\frac{\partial F_S}{\partial I_D} &= -R_D g_D \\
\frac{\partial F_S}{\partial I_S} &= 1 + R_S \left( \partial I_{GS} + g_m + g_D \right)
\end{align*}
\]  

(31) (32) (33) (34) (35) (36)
If \( V_D - V_S < 0 \): \((g_m < 0, g_D > 0)\):

\[
\frac{\partial F_D}{\partial I_G} = R_G \left( \frac{\partial I_{GD}}{\partial I_G} - g_m \right)
\]

\[
\frac{\partial F_D}{\partial I_D} = 1 + R_D \left( \frac{\partial I_{GD}}{\partial I_D} - g_m + g_D \right)
\]

\[
\frac{\partial F_D}{\partial I_S} = -R_S g_D
\]

\[
\frac{\partial F_S}{\partial I_G} = R_G \left( \frac{\partial I_{GS}}{\partial I_G} + g_m \right)
\]

\[
\frac{\partial F_S}{\partial I_D} = R_D \left( g_m - g_D \right)
\]

\[
\frac{\partial F_S}{\partial I_S} = 1 + R_S \left( \frac{\partial I_{GS}}{\partial I_S} + g_D \right)
\]

Here, \( \partial I_{GD} \) and \( \partial I_{GS} \) are the differentials of \( I_{GD} \) and \( I_{GS} \). The inner derivative of these differentials varies, depending on which current the derivation has been performed with respect to. In Eqs. (28), (31), (34), (37) and (40) the inner derivative is \( R_G \) (current \( I_G \)), in Eqs. (29), (32), (35), (38) and (41) \( R_D \) (current \( I_D \)), and in Eqs. (30), (33), (36), (39) and (42) \( R_S \) (current \( I_S \)). \( g_m \) is the intrinsic transconductance and \( g_D \) is the intrinsic drain, or output conductance. These parameters are obtained using the following equations:

\[
g_m = \frac{\partial I_{DS}}{\partial V_{GS}}
\]

\[
g_D = \frac{\partial I_{DS}}{\partial V_{DS}}
\]

It should be emphasized that due to the parasitic resistances and forward gate conduction, these are not the conductances that can be measured from the electrodes of a MESFET. The extrinsic transconductance \( G_m \) and extrinsic drain conductance \( G_D \) can be expressed as:

If \( V_D - V_S \geq 0 \):

\[
G_m = \frac{-\partial I_D}{\partial (V_G - V_S)} = \frac{g_m}{1 + R_S (g_m + \partial I_{GS}) + R_G \partial I_{GS}}
\]

\[
G_D = \frac{-\partial I_D}{\partial (V_D - V_S)} = \frac{g_D}{1 + g_D (R_S + R_D)}
\]
If $V_D - V_S < 0$:

$$G_m = -\frac{\partial I_S}{\partial (V_G - V_D)} = \frac{g_m}{1 + R_D (g_m + g_{GD}) + R_S g_{GD}}$$

(47)

$$G_D = -\frac{\partial I_S}{\partial (V_S - V_D)} = \frac{g_D}{1 + g_D (R_S + R_D)}$$

(48)

These parameters have no direct significance for the single MESFET current iteration, but they are needed for the circuit’s conductance matrix in SPICE. Note that if the MESFET is symmetrical ($R_S = R_D$), the expressions for $G_m$ and $G_D$ are the same for positive and negative values of $V_{DS}$. However, for negative values, in the inverse region of operation, the drain and source are interchanged.

Using Eq. (18) it is now possible to obtain the currents and voltages in the MESFET to the wanted precision by performing an iteration. This iteration is continued until the absolute values of all three current functions $F_G$, $F_D$, and $F_S$ have been reduced to the wanted maximum error limit. Strictly speaking, a more exact measure of convergence is obtained by looking at the absolute values of the differences between the previous and current values of $I_G$, $I_D$, and $I_S$. For an arbitrary function these will always get smaller at each iteration step, whereas this is not necessarily always true for the error functions. Actually, in SPICE this is done by specifying a relative tolerance (RELTOL) for the voltages and currents. However, in the program MESFETOPT, the error functions alone have been considered to be sufficient for determining when the iteration can be stopped.

Since the Newton-Raphson method converges rapidly, a suitable maximum error of 1 µA or smaller can be used. However, the convergence speed also depends on the start values of the voltages and currents, and in practice it may be necessary to enforce restrictions on these values during the iteration, because of the often complicated nature of the current-voltage relationships. Especially exponential expressions, for example those used for diode I-V characteristics, can easily make the iteration ‘go astray’ and cause a real number under- or overflow error in the computer.
8. GaAs MESFET models

8.1 Semiconductor device model types

The goal in semiconductor device simulation is, of course, to maximize the physical accuracy and minimize the computational cost - the time and hardware required to perform the simulation. However, as these two demands usually are mutually exclusive, the complexity of the simulation model has to be adjusted to the minimal needs of the user. The two extremes here are circuit simulation versus discrete device simulation, and on this basis simulation models can roughly be divided into two categories: *Interpolative* and *extrapolative* models.

An interpolative model (sometimes referred to as an *empirical* model) is generated by assuming that some functional form describes experimental data and then fitting parameters into the functional form by minimizing the error between the experimental data and simulated data over the range of the experimental data. Clearly, there is no reason why this functional form should fit the data outside the range of the experimental data. The GaAs MESFET models implemented in different versions of SPICE are typical interpolative models. An example of an extremely empirical model can be found in [27], where piecewise polynomials are used to approximate the I-V curves of FETs.

In contrast to the interpolative model, the extrapolative model is strongly based on the physics of the device. Model parameters are fitted in a similar way, but because of the physical basis of the model, the parameters have a strong physical meaning and can be considered to hold true outside the range of experimental data. In this case the model can be used outside the experimentally determined range with considerable confidence. Therefore, an extrapolative model is very useful in predicting behaviour outside the range of known behaviour or in determining the behaviour of devices not yet fabricated. Unfortunately, this type of model is not ideally suitable for circuit simulation. Already when the model complexity is of the order of the SPICE level 2 MOSFET model, SPICE spends 60 - 70% of the total CPU time evaluating the model equations [28]. However, none of the models presented in this work are this complex.

Simulation models can also be divided into *analytical* and *numerical* models. An analytical model is a model whose solution can be represented as a closed form mathematical expression. In some cases, however, the relationships in the analytical model are implicit in nature and an analytical inversion does not exist. In this case the computational cost of the model is still small, because analytic expressions can usually be inverted without much numerical complexity. However, the actual model becomes numerical, and this is actually the case with all useful analytical GaAs MESFET models. To achieve even modest degrees of physical accuracy, iterative equation solving has to be used. A numerical model is one in which the solution to the model equations must be obtained by numerical computation. This is the case with two- or three-dimensional models involving large matrix operations and integration of partial differential equations. The computational cost of these models is usually very high, and they are therefore unsuitable for circuit simulation.
8.2 General MESFET circuit model topics

Before going into the details of various MESFET circuit models, a couple of points must be discussed. The first one is about how the device is actually described in a circuit simulation program, i.e. the structure of the equivalent circuit. Figure 14 shows a general equivalent circuit for the MESFET.

![Figure 14. General MESFET equivalent circuit. The elements in the shaded area are usually ignored.](image)

The Schottky gate junction is modeled by two diodes going from the gate contact to the source and the drain, and the channel is modeled by a voltage-dependent current source. The parasitic gate, drain and source resistances are also included, as well as the gate-drain and gate-source capacitances. These may include both constant and voltage-dependent parts, and can be implemented either through capacitance equations, or by charge equations for charge conservation.

Most MESFET models of today use an equivalent circuit like this, and only differ in the equations for $I_{DS}$, and maybe for $C_{GD}$ and $C_{GS}$. Newer, more sophisticated models are also starting to include the circuit elements in the shaded area in Figure 14. However, the equivalent circuit of the MESFET does not need to be substantially more accurate than the expected device variations within a given circuit. If it were, processing variations would inevitably mask any performance improvement that might be predicted by the model. Since device uniformity in GaAs technology is still relatively poor compared with silicon technology, MESFET modeling should concentrate more on correctly predicting device trends than on precise matching to given device characteristics.
Another important point is the geometry dependencies of the model parameters. Ideally, one would like to use only one set of model parameters to cover the entire spectrum of possible device sizes, that is, gate widths and lengths. However, if a very wide range of device sizes is used the available model(s) will probably not be able to reproduce all the device characteristics accurately enough. Generally, the characteristics scale much more accurately with gate width than with gate length, so in purely digital designs where all the devices usually have the same gate length, one parameter set is enough in most cases. This is not true for GaAs analog circuits, and as the number of these is rapidly increasing, and the design of digital GaAs VLSI circuits also needs increasingly accurate simulations, it is necessary to pay more attention to model parameter geometry dependence.

In chapters 8.5 - 8.9, the most popular GaAs MESFET models of today and the new analytical model are presented. The parameter geometry dependencies that are usually employed are shown in the parameter lists in the column titled ‘Scaling’. Also, for these models the parasitic resistances $R_S$ and $R_D$ are listed as model parameters, but their effect on the I-V characteristics is not directly shown. However, in all the models the intrinsic voltages are calculated according to Eqs. (6), (7) and (8) from chapter 7.

Examples of simulated versus measured I-V characteristics for a DMESFET with a gate length of 1 µm and a gate width of 20 µm are given for every model. The parasitic resistances $R_S$ and $R_D$ have been measured and are the same for all models, but the other parameters have been obtained by nonlinear optimization using the developed computer program MESFETOPT. In this optimization, the average absolute difference between simulated and measured drain current was minimized. The errors at the beginning of the optimizations were approximately equal for all models, and optimizations were continued until the variance of the parameter values was less than $10^{-20}$. 
8.3 Basic device theory

When developing a MESFET model for circuit simulation, a number of approximations have to be made in order to simplify the calculations. The most important of these approximations are:

1. **Uniform charge distribution.** The MESFET channel is assumed to consist of a uniformly doped n' region, which ends abruptly at a specific depth.

2. **Gradual channel approximation.** The potential in the channel at the gate junction is assumed to be a slowly varying function of the position in the x direction. This is strictly true only for MESFETs in which the channel thickness is much smaller than the gate length.

3. **Abrupt depletion layer.** The depletion layer that forms in the channel under the MESFET gate is assumed to end abruptly.

4. **Piecewise-linear approximation** of the electron velocity as a function of the electric field in the channel. This approximation is used in MESFET models that attribute the drain current saturation to the saturation of the electron velocity at high electric fields. The electron velocity is assumed to be proportional to the electric field until the saturation velocity, $v_{sat}$, is reached at a field strength of $E_{sat}$, and then to become constant. This is shown in Figure 15.

![Figure 15. Piecewise-linear approximation of GaAs electron velocity $v_e$ versus electric field $E$. $\mu_0$ is the electron mobility.](image)

For the channel doping levels used in most MESFETs, the negative differential mobility region is negligible, and the piecewise-linear approximation is sufficient.

For a uniformly doped n region, under the gradual channel approximation, the depletion-layer width $w$ varies only gradually along the channel (x direction) and one can solve the one-dimensional Poisson equation in the y direction:

$$-\frac{d^2V}{dy^2} = \frac{dE_y}{dy} = \frac{\rho(y)}{\varepsilon_{GaAs}}$$

(49)
or

\[-\frac{d^2 V}{dy^2} = \frac{qN}{\varepsilon_{GaAs}}\]  \hspace{1cm} (50)

where \(E_y\) is the electric field in the \(y\) direction, \(\rho(y)\) the channel charge density as a function of \(y\), \(\varepsilon_{GaAs}\) the absolute dielectric constant of GaAs, \(q\) the electron charge and \(N\) the channel doping concentration. This situation is depicted in Figure 16.

**Figure 16.** Channel-to-gate potential and electric field under the gradual channel approximation.

The channel-to-gate potential \(V(x)\) is obtained by integration of the one-dimensional Poisson equation in the \(y\) direction in the depletion region, for a volume charge density \(N\). This treatment of the depletion layer potential is justified on the basis that the potential changes along the channel are gradual (gradual channel approximation) or, equivalently, that the longitudinal field in the channel is negligible compared to the transverse field in the depletion region. This condition is fulfilled if the channel thickness is much smaller than the total gate length. Since there is no surface charge density at the boundaries of the conducting channel, i.e., the edges of the depletion region, the transverse electric field vanishes there. With this boundary condition, we obtain for \(V(x)\) the expression

\[V(x) = V_p \left(1 - \frac{b(x)}{a}\right)^2\]  \hspace{1cm} (51)

where \(a\) is the total thickness of the channel, \(b(x)\) is the ‘height’ or opening of the channel at the point \(x\), and \(V_p\) the so-called pinchoff voltage required to make the depletion layer width equal to the channel thickness. The expression for \(V_p\) is

\[V_p = \frac{qNa^2}{2\varepsilon_{GaAs}}\]  \hspace{1cm} (52)

However, because of the Schottky gate junction built-in voltage drop \(V_{BI}\), the channel will be completely depleted at a less negative voltage than \(-V_p\). This *threshold voltage* is defined as

\[V_{TH} = V_{BI} - V_p\]  \hspace{1cm} (53)
8.4 The Shockley model

The field effect transistor was analyzed by W. Shockley in the early 1950s [8]. In this analysis the approximations 1 - 3 presented in the preceding chapter were used.

The Shockley model assumes that the electron drift velocity

\[ v_e = \mu_0 E \]  

(54)

is proportional to the longitudinal electric field \( E \) up to the point where the channel is pinched off at the drain side of the gate, which happens when

\[ V_{GS} - V_{DS} \leq V_{TH} \]  

(55)

At this point, the longitudinal component of the electric field at the drain side of the gate becomes infinite from the formal point of view. In spite of this obvious failure of this model to adequately represent the electron transport in the drain region, it provides good agreement with the I-V characteristics of devices with long gates, large pinch-off voltages, low electron mobility and large saturation velocity. This may be due to the fact that the pinched-off region is only a small fraction of the total channel length. An often used rule-of-thumb is that the gate length should be larger than or equal to three times the channel thickness in order for the Schockley model to be applicable.

Under the assumptions presented previously the channel drain-source current can be expressed by Ohm’s law as follows:

\[ I_{DS} = qNWb(x)v_e(x) \]  

(56)

where \( b(x) \) is the opening of the conducting channel from Eq. (51), and \( v_e(x) \) is the electron velocity in the channel at point \( x \), equal to \( \mu_0 E(x) \) as agreed. Noting that \( E(x) \) equals \( \frac{V(x)}{V_p} \) and solving Eq. (51) for \( b(x) \) yields

\[ I_{DS} = qNW\mu_0a \sqrt{1 - \frac{V(x)}{V_p}} \frac{d}{dx}V(x) \]  

(57)

Rearranging the terms and determining integration limits gives

\[ \int_0^L I_{DS}dx = (qNW\mu_0a) \int_{V_{BI}-V_{GS}}^{(V_{BI}-V_{GS}+V_{DS})} \left(1 - \frac{V(x)}{V_p}\right)dV(x) \]  

(58)

Integration finally results in

\[ I_{DS} = \frac{qNW\mu_0a}{L} \left( V_{DS} - \frac{2}{3q\sqrt{V_p}} \left( (V_{BI}-V_{GS}+V_{DS})^{3/2} - (V_{BI}-V_{GS})^{3/2} \right) \right) \]  

(59)

This is the fundamental equation of field-effect transistors.
By setting $V_{DS}$ equal to $V_{GS} - V_{TH}$ in Eq. (59), taking Eq. (53) into account, and defining the pinchoff current $I_p$ as

$$I_p = \frac{qN\mu_0 W a V_p}{3L}$$  \hspace{1cm} (60)

the maximum, or saturation current for a given $V_{GS}$ can be expressed as

$$I_{DS_{sat}} = I_p \left( 1 - 3 \left( \frac{V_{BI} - V_{GS}}{V_p} \right) + 2 \left( \frac{V_{BI} - V_{GS}}{V_p} \right)^{3/2} \right)$$  \hspace{1cm} (61)

For gate voltages near the threshold voltage $V_{TH}$ this expression can be simplified. By replacing $V_{BI}$ in Eq. (61) with $V_{TH} + V_P$ one gets

$$I_{DS_{sat}} = I_p \left( 1 - 3 \left( \frac{V_{TH} + V_P - V_{GS}}{V_p} \right) + 2 \left( \frac{V_{TH} + V_P - V_{GS}}{V_p} \right)^{3/2} \right)$$  \hspace{1cm} (62)

Applying the Taylor series expansion around the point $V_{GS} = V_{TH}$ and taking the first three terms yields

$$I_{DS_{sat}} = I_p \frac{3}{2V_p} (V_{GS} - V_{TH})^2 = \frac{W\mu_0 \varepsilon_{GaAs}}{aL} (V_{GS} - V_{TH})^2$$  \hspace{1cm} (63)

This quadratic dependence of the saturation current on the gate-source voltage is used in most empirical MESFET circuit models of today. It has been demonstrated that this ‘square law’ fits the measured characteristics of long gate FETs quite well even for nonuniform doping profiles [29]. Eq. (63) is usually written as

$$I_{DS_{sat}} = \beta (V_{GS} - V_{TH})^2$$  \hspace{1cm} (64)

where $\beta$ is called the transconductance coefficient. From Eq. (63) it can be seen that $\beta$ depends on the gate width and length, channel thickness and electron drift mobility. However, Shur has hypothesized that [30]

$$\beta = \frac{2W\mu_0 \varepsilon_{GaAs} V_{sat}}{a (\mu_0 V_p + 3 V_{sat} a L)}$$  \hspace{1cm} (65)

which would add a dependence of the saturated drift velocity and weaken the dependence of $1/L$.

For drain-source voltages beyond the saturation point, the channel current is usually assumed to remain essentially the same as the saturation current. In order to model the small drain current increase with $V_{DS}$ in the saturation region, the current can be multiplied by the expression

$$1 + \lambda V_{DS}$$

where $\lambda$, the channel length modification coefficient, corresponds to the saturated drain conductance.
8.5 The JFET model

The JFET or Shichman-Hodges model [8,31] was originally intended for Si JFETs, but has also been used for GaAs MESFETs, mainly due to the lack of better MESFET models. The version of this model used in this work has one modification: An extra voltage source controlling $V_{GS}$, $E_{VGS}$, has been added [32]. Setting $E_{VGS} = 1$ gives the same result as the original JFET model. The equations are the following:

\[
V_{DS} \leq E_{VGS} V_{GS} - V_{TH} \text{ (linear region):}
\]

\[
I_{DS} = \beta V_{DS} (2 (E_{VGS} V_{GS} - V_{TH}) - V_{DS}) (1 + \lambda V_{DS})
\] (66)

\[
V_{DS} > E_{VGS} V_{GS} - V_{TH} \text{ (saturation region):}
\]

\[
I_{DS} = \beta (E_{VGS} V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})
\] (67)

The model has 6 parameters:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta$</td>
<td>BETA</td>
<td>transconductance coefficient</td>
<td>A/V$^2$</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>VTO</td>
<td>threshold voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$E_{VGS}$</td>
<td>EVGS</td>
<td>factor for $V_{GS}$ voltage source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\lambda$</td>
<td>LAMBDA</td>
<td>channel length modification coefficient</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$R_S$</td>
<td>RS</td>
<td>source resistance</td>
<td>$\Omega$</td>
<td>1/W</td>
</tr>
<tr>
<td>$R_D$</td>
<td>RD</td>
<td>drain resistance</td>
<td>$\Omega$</td>
<td>1/W</td>
</tr>
</tbody>
</table>

The main advantage of this model is its simplicity. The simulation times are short, and it’s quite easy to extract the parameters manually from a measured set of $I_{DS}$-$V_{DS}$ curves. But as the model does not include velocity saturation, nonphysical values of $\beta$ and $R_S$ are required to fit the saturation current $I_{DS_{Sat}}$ of the lower curves, especially for short-channel devices. This leads to a $R_S$ value of zero when fitting the linear region, and thus the symmetry of the device is destroyed, which means the inverse region ($V_{DS} < 0$) will not be properly represented. Also, the saturation voltage $V_{DS_{Sat}}$, which is taken as $V_{GS} - V_{TH}$ or $E_{VGS} V_{GS} - V_{TH}$, is overpredicted.

Parameter values:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$</td>
<td>-1.13 V</td>
</tr>
<tr>
<td>$E_{VGS}$</td>
<td>1.0</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$1.65 \times 10^{-3}$ A/V$^2$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>$5.19 \times 10^{-6}$ 1/V</td>
</tr>
<tr>
<td>$R_S$</td>
<td>23.61 $\Omega$</td>
</tr>
<tr>
<td>$R_D$</td>
<td>23.61 $\Omega$</td>
</tr>
</tbody>
</table>

Average absolute $I_D$ error 97.5 $\mu$A

Figure 17. Example fit of JFET model I-V characteristics to those of a 1 x 20 $\mu$m depletion MESFET.
Figure 17. clearly shows that the JFET model gives a poor fit to the I-V characteristics of a GaAs MESFET if the values of the parasitic resistors are kept constant, as measured. The extra $E_{VGS}$ gate voltage coefficient helps to correct the error to some extent, as can be seen from Figure 18.

![Figure 18: Example fit of extra voltage source JFET model I-V characteristics to those of a 1 x 20 $\mu$m depletion MESFET.](image)

Parameter values:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$</td>
<td>-0.75 V</td>
</tr>
<tr>
<td>$E_{VGS}$</td>
<td>0.64</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$3.29 \times 10^{-3}$ A/V$^2$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>$55.56 \times 10^{-3}$ 1/V</td>
</tr>
<tr>
<td>$R_s$</td>
<td>23.61 $\Omega$</td>
</tr>
<tr>
<td>$R_D$</td>
<td>23.61 $\Omega$</td>
</tr>
</tbody>
</table>

Average absolute $I_D$ error 60.7 $\mu$A

Figure 18. Example fit of extra voltage source JFET model I-V characteristics to those of a 1 x 20 $\mu$m depletion MESFET.

The JFET model is available in most SPICE versions, but in order to include the $E_{VGS}$ parameter, a subcircuit containing a JFET and a voltage-controlled voltage source must be used. However, with the standard SPICE input commands it is not possible to make the voltage source control symmetrical with respect to $V_{DS}$, and this means that the inverse region of the MESFET will be distorted.
The hyperbolic tangent model of Curtice [33,34] is an attempt to correct the worst shortcomings of the JFET model. Since the function tanh(x) starts from the origin and approaches 1 as x increases, it can be used to get a good linear region that connects smoothly with the saturation region. Some versions of the model implemented in various circuit simulators have a variable gate voltage expression exponent Exp [35,36]. The value of Exp is 2 for the original Curtice model, but other values may produce better fits to measurements of devices with different doping profiles. The equation is of the form:

\[
I_{DS} = \beta (V_{GS} - V_{TH})^{\text{Exp}} (1 + \lambda V_{DS}) \tanh (\alpha V_{DS})
\] (68)

The model has 7 parameters:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>β</td>
<td>BETA</td>
<td>transconductance coefficient</td>
<td>A/V²</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>V_{TH}</td>
<td>VTO</td>
<td>threshold voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Exp</td>
<td>EXP</td>
<td>variable exponent</td>
<td></td>
<td></td>
</tr>
<tr>
<td>α</td>
<td>ALPHA</td>
<td>tanh constant</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>λ</td>
<td>LAMBDA</td>
<td>channel length modification coefficient</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>R_S</td>
<td>RS</td>
<td>source resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
<tr>
<td>R_D</td>
<td>RD</td>
<td>drain resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
</tbody>
</table>

This model already makes it possible to get a much better fit than with the JFET model. One disadvantage is that evaluation of the tanh function slows down the simulation. The I-V characteristics fit of the original tanh model are shown in the figure below.

Parameter values:

- \( V_{TH} \) = -1.21 V
- \( \text{Exp} \) = 2.0
- \( \beta \) = 1.36 \times 10^{-3} \text{ A/V}^2
- \( \alpha \) = 2.25 1/V
- \( \lambda \) = 35.23 \times 10^{-3} 1/V
- \( R_S \) = 23.61 Ω
- \( R_D \) = 23.61 Ω

Average absolute \( I_D \) error 47.8 μA

Figure 19. Example fit of hyperbolic tangent model I-V characteristics to those of a 1 x 20 μm depletion MESFET.
When the gate voltage expression exponent is varied, the fit improves even more. Usually Exp values smaller than 2 give the best results.

Parameter values:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$</td>
<td>-0.96 V</td>
</tr>
<tr>
<td>Exp</td>
<td>1.51</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$2.17 \times 10^{-3}$ A/V$^2$</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>2.25 1/V</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>$29.20 \times 10^{-3}$ 1/V</td>
</tr>
<tr>
<td>$R_s$</td>
<td>23.61 Ω</td>
</tr>
<tr>
<td>$R_D$</td>
<td>23.61 Ω</td>
</tr>
</tbody>
</table>

Average absolute $I_D$ error 19.2 μA

**Figure 20.** Example fit of variable exponent hyperbolic tangent model I-V characteristics to those of a 1 x 20 μm depletion MESFET.
8.7 The Statz model

The model by Statz et. al. [37], also called the Raytheon model, is based on the tanh model, but has two main improvements that make it very interesting. $I_{DS}$ is calculated as:

$V_{DS} \leq 3/\alpha$ (linear region):

$$I_{DS} = \frac{\beta (V_{GS} - V_{TH})^2}{1 + B (V_{GS} - V_{TH})} \left(1 - \left(1 - \frac{\alpha V_{DS}}{3}\right)^3\right) (1 + \lambda V_{DS})$$

(69)

$V_{DS} > 3/\alpha$ (saturation region):

$$I_{DS} = \frac{\beta (V_{GS} - V_{TH})^2}{1 + B (V_{GS} - V_{TH})} (1 + \lambda V_{DS})$$

(70)

The model has 7 parameters:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta$</td>
<td>BETA</td>
<td>transconductance coefficient</td>
<td>A/V²</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>VTO</td>
<td>threshold voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>B</td>
<td>doping profile parameter</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$\alpha$</td>
<td>ALPHA</td>
<td>tanh constant</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$\lambda$</td>
<td>LAMBDA</td>
<td>channel length modification coefficient</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$R_S$</td>
<td>RS</td>
<td>source resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
<tr>
<td>$R_D$</td>
<td>RD</td>
<td>drain resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
</tbody>
</table>

The middle term in the expression for the linear region is a polynomial approximation of the tanh function that saves CPU time without sacrificing too much accuracy. It is replaced by 1 in the saturation region. The denominator containing the parameter B, $1 + B (V_{GS} - V_{TH})$, is empirically chosen to give a good fit for both large and small values of $(V_{GS} - V_{TH})$. It has been shown that the current of a MESFET can be well described by a quadratic expression like

$$(V_{GS} - V_{TH})^2$$

only near the pinchoff point, elsewhere the behaviour is better described by a square root expression, which behaves quite linearly at high $V_{GS}$ values. The use of the denominator smoothly connects the quadratic law at low $V_{GS}$ values to the linear behaviour at high $V_{GS}$ values.

The value of B for a ‘bare’ transistor, that is, a transistor for which the voltage drops over $R_S$ and $R_D$ have been taken into account, is a measure of the doping profile extending into the insulating substrate. This profile depends on the fabrication process and thus B has a physical meaning in some sense. Also, the use of this denominator makes the model rather forgiving, permitting a good fit even when $R_S$ and $R_D$ are neglected.
Divekar [38] has proposed that the saturation current of a MESFET could be modeled by the general expression

\[ I_{DS_{sat}} = \frac{\beta (V_{GS} - V_{TH})^n}{1 + B (V_{GS} - V_{TH})^m} \]  \hspace{1cm} (71)

where the exponents n and m are treated as user input parameters. With this kind of variable-exponent Statz model, it would be possible to simulate the gate voltage dependence of FETs with almost any conceivable doping profiles very accurately. However, non-integer powers tend to consume considerable computer time.
8.8 The cubic model

The cubic model by Curtice and Ettenberg [39,40] relies on a third-order polynomial to model the saturation current as a function of both $V_{GS}$ and $V_{DS}$:

$$I_{DS} = (A_3 V_1^3 + A_2 V_1^2 + A_1 V_1 + A_0) \tanh (\alpha V_{DS})$$

where

$$V_1 = V_{GS} \left( 1 + \lambda (V_0 - V_{DS}) \right)$$

The model has 9 parameters:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_0$</td>
<td>A0</td>
<td>polynomial factor 0</td>
<td>A</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>$A_1$</td>
<td>A1</td>
<td>polynomial factor 1</td>
<td>A/V</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>$A_2$</td>
<td>A2</td>
<td>polynomial factor 2</td>
<td>A/V^2</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>$A_3$</td>
<td>A3</td>
<td>polynomial factor 3</td>
<td>A/V^3</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>$V_0$</td>
<td>V0</td>
<td>$A_0 - A_3$ evaluation $V_{DS}$ value</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$\alpha$</td>
<td>ALPHA</td>
<td>tanh constant</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$\lambda$</td>
<td>LAMBDA</td>
<td>coefficient for pinchoff change</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$R_S$</td>
<td>RS</td>
<td>source resistance</td>
<td>$\Omega$</td>
<td>1/W</td>
</tr>
<tr>
<td>$R_D$</td>
<td>RD</td>
<td>drain resistance</td>
<td>$\Omega$</td>
<td>1/W</td>
</tr>
</tbody>
</table>

Eq. (73) models the increase of the threshold voltage with the drain-source voltage, and $\lambda$ is the coefficient for pinchoff change as a function of $V_{DS}$. This means that if it is necessary to obtain the threshold voltage for this model, for example for capacitance modeling, it must be calculated by solving the third-order equation

$$A_3 V_1^3 + A_2 V_1^2 + A_1 V_1 + A_0 = 0$$

for $V_1$, and then solving Eq. (73) for $V_{GS}$. $V_0$ is the $V_{DS}$ value at which the coefficients $A_0 - A_3$ were evaluated. The model gives a good fit, as can be seen from Figure 22., but also uses up a lot of CPU time because of the relatively complicated equations.

Parameter values:

- $A_0$ = 2.17⋅10^{-3} A
- $A_1$ = 3.46⋅10^{-3} A/V
- $A_2$ = 0.82⋅10^{-3} A/V^2
- $A_3$ = -0.40⋅10^{-3} A/V^3
- $V_0$ = 1.49 V
- $\alpha$ = 2.03 1/V
- $\lambda$ = 36.45⋅10^{-3} 1/V
- $R_S$ = 23.61 $\Omega$
- $R_D$ = 23.61 $\Omega$

Average absolute $I_D$ error 22.9 $\mu$A

Figure 22. Example fit of cubic model I-V characteristics to those of a 1 x 20 $\mu$m depletion MESFET.
8.9 The VTT model

This is a semi-analytical velocity saturation model originally proposed by Pucel et al. [10, 41], which has been developed further at VTT [42]. The equations presented here form the current version of this model as used by the author, and the input parameters for these equations are as follows:

**Basic parameters:**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>gate length</td>
<td>m</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>W</td>
<td>gate width</td>
<td>m</td>
<td></td>
</tr>
<tr>
<td>a</td>
<td>CHA</td>
<td>channel thickness</td>
<td>m</td>
<td></td>
</tr>
<tr>
<td>V_{BI}</td>
<td>VBI</td>
<td>gate Schottky barrier voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(\mu_0)</td>
<td>UO</td>
<td>electron mobility</td>
<td>m^2/Vs</td>
<td></td>
</tr>
<tr>
<td>E_{sat}</td>
<td>ES</td>
<td>saturation field</td>
<td>kV/cm</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>ND</td>
<td>channel doping concentration</td>
<td>1/m^3</td>
<td></td>
</tr>
<tr>
<td>R_S</td>
<td>RS</td>
<td>source resistance</td>
<td>(\Omega)</td>
<td>1/W</td>
</tr>
<tr>
<td>R_D</td>
<td>RD</td>
<td>drain resistance</td>
<td>(\Omega)</td>
<td>1/W</td>
</tr>
</tbody>
</table>

**Optional parameters:**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_P</td>
<td>VP</td>
<td>pinchoff voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{DSat}</td>
<td>IDSAT</td>
<td>saturation current</td>
<td>A</td>
<td>W, 1/L</td>
</tr>
<tr>
<td>(\lambda)</td>
<td>LAMBDA</td>
<td>channel length modification coefficient</td>
<td>1/V</td>
<td></td>
</tr>
</tbody>
</table>

There is a total of 12 variable parameters, of which 3 are optional. These optional parameters affect the simulation only if their values are changed from the default values. The first two optional parameters are the pinchoff voltage, \(V_P\), and saturation current, \(I_{DSat}\), which can be specified directly by the user for greater flexibility. However, the default values for these parameters are 100 and 0, respectively, and if these values are not changed by the user, then \(V_P\) and \(I_{DSat}\) will be calculated from the basic parameters.

Because the channel current is a much more complicated function of the parameters than in the nonphysical SPICE models, it is more difficult to get a good fit of simulation data to measurement data, but the fit can be extremely good, and still retain physically reasonable parameter values.

The model uses the same expressions as the Shockley model in the linear region. However, instead of assuming that the electron drift velocity is proportional to the electric field in the channel up to pinchoff, the piecewise-linear approximation shown in Figure 15. is used. Saturation begins when the field in the channel reaches the saturation field \(E_{sat}\). In order to simplify the used expressions, two non-dimensional potentials are introduced:
With these potentials, Eq. (59) can be re-written as

$$I_{DS} = \frac{I_{DSsat}}{E_{sat}} V_P f_1(s, p) = \frac{I_{DSsat}}{E_{sat}} V_P \left( p^2 - s^2 - \frac{2}{3} (p^3 - s^3) \right)$$

(77)

where the saturation current, $I_{DSsat}$, now is defined as

$$I_{DSsat} = q N \mu \rho_{sat} W a$$

(78)

Unlike the Schockley model, this model does not assume a constant current in the saturation region. Instead, the current in the saturation region is calculated as

$$I_{DS} = I_{DSsat} (1 - p)$$

(79)

where $p$ now is defined as

$$p = \sqrt{\frac{V_{BI} - V_{GS} + V_1}{V_P}} = \sqrt{s^2 + \frac{V_1}{V_P}}$$

(80)

$V_1$ is the voltage drop over the linear region in the MESFET channel. The situation is clarified in Figure 23.

**Figure 23.** Schematic cross-section of a MESFET channel region.

The voltage drop $V_1$ occurs over the linear region that has the length $L_1$. In the saturation region of length $L_2$ the longitudinal electric field is determined entirely by free charges on the drain electrode - if carrier accumulation is neglected - since the carriers travel at their saturation velocity. The potential produced by the free charges satisfies Laplace’ equation. The most general solution of this equation valid for the interval $L_1 \leq x \leq L$ which vanishes at the boundary plane $x = L_1$, and at the gate electrode $y = a$, is of the form
where the coefficients $A_n$ are determined from the boundary conditions at points $x = L_1$ and $x = L$. The potential in the channel is given by $V(x, y = a - b_2)$. Taking only the lowest-order term of the series in Eq. (81) and using the boundary condition

$$E_x(L_1) = \frac{d}{dx} V(x) \big|_{x = L_1} = E_{sat}$$

(82)

yields

$$V_2 = \frac{2E_{sat} (a - b_2)}{\pi} \sinh \left( \frac{\pi (L - L_1)}{2(a - b_2)} \right)$$

(83)

Taking more terms gives a more accurate solution, and also the value of $b_2$, the thickness of the conducting part of the channel at the drain end [43,44]. However, for circuit simulation this approach is too time-consuming, so in this model the following approximation is used for $b_2$:

$$b_2 \approx b_1 = a (1 - p)$$

(84)

where $b_1$ is the known thickness at the beginning of the saturated region ($x = L_1$). In other words, the thickness of the conducting channel layer at $x = L$ is assumed to be equal to the thickness at $x = L_1$. Now that $V_2$ is known, $V_1$ can be calculated

$$V_1 = V_{DS} - V_2$$

(85)

The length of the linear region, $L_1$, is calculated using the current continuity between the linear and saturation regions. By setting Eqs. (77) and (79) equal and solving for $L$ (equal to $L_1$ in this case) one gets

$$L_1 = \frac{V_p f_1(s, p)}{E_{sat} (1 - p)}$$

(86)

where $f_1(s,p)$ is the same as in Eq. (77).

The region of operation at each voltage point ($V_{GS}, V_{DS}$) can be determined by assuming that the device is saturated and solving for $V_1$ by iteration with Eq. (85) as the goal. In the program MESFETOPT, this iteration is stopped when the error has decreased below 1 $\mu$V, but in the SPICE implementation described in chapter 10, the voltage accuracy option VNTOL is used as the stopping criterion. If $L_1$ turns out to be equal to or greater than $L$, it means that the MESFET is operating in the linear region instead of the saturation region.

Alternatively, the drain voltage at which the device saturates, $V_{DSSat}$, can first be calculated by setting Eq. (86) equal to $L$, solving the resulting third-order equation numerically for $p$, and then calculating $V_{DSSat}$ from $p$ through Eq. (76). This strategy is used in the actual model, because the exact value of $V_{DSSat}$ is needed in the capacitance modeling. Also, knowing $V_{DSSat}$ it is possible to get a good first approximation for $V_1$, which makes the iteration in the saturation region converge much faster. The trigonometric method is used to solve the third-order equation.
In the other GaAs MESFET models, the channel length modification coefficient \( \lambda \) is used in order to get the right slope for the \( I_{DS} - V_{DS} \) curves in saturation. In the VTT MESFET model this slope is normally correct even without \( \lambda \). However, for greater flexibility, and also because the increased AC drain conductance can be approximately modeled this way, a modification of the drain-source conductance is performed through the use of \( \lambda \):

\[
egin{align*}
I_{DS\text{ (new)}} &= I_{DS\text{ (old)}} \left( 1 + \lambda V_{DS} \right) \\
g_m\text{ (new)} &= g_m\text{ (old)} \left( 1 + \lambda V_{DS} \right) \\
g_D\text{ (new)} &= g_D\text{ (old)} \left( 1 + \lambda V_{DS} \right) + I_{DS\text{ (old)}} \lambda
\end{align*}
\]

(87)  (88)  (89)

For DC curves, \( \lambda \) is very small or equal to zero, and for AC curves the value of the parameter can be increased to some value that gives a good fit to measured curves.

Figure 24. demonstrates that the fit given by this model is very good indeed, in fact the best of the models presented here.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure.png}
\caption{Example fit of analytical model I-V characteristics to those of a 1 x 20 \( \mu m \) depletion MESFET. The parameters \( V_{TH} \) and \( I_{DS\text{sat}} \) are not optimized but calculated from the other parameters according to Eqs. (53) and (78), respectively.}
\end{figure}

A model implemented using the equations presented this far works very well for “normal” \( V_{GS} \) values between the threshold voltage and the Schottky diode voltage:

\[
V_{BI} - V_P < V_{GS} < V_{BI}
\]

(90)

However, the derivative of \( I_{DS} \) with respect \( V_{GS} \), that is, the intrinsic transconduction, is discontinuous at \( V_{GS} = V_{TH} = V_{BI} - V_P \) and \( V_{GS} = V_{BI} \). The reason for this lies in the definition of the parameter \( s \), Eq. (75). This parameter gives the opening of the channel at the source end of the gate, as can be seen from Figure 23., and it’s value can range from zero to one. Figure 25. shows the behaviour of \( s \) as a function of \( V_{GS} \).
Figure 25. The parameter s as a function of $V_{GS}$. The insets show the parabolic smoothing used at points $V_{GS} = V_{TH}$ and $V_{GS} = V_{BI}$.

The discontinuities arise from the fact that the derivative of s is not equal to zero at $V_{GS} = V_{TH}$ and $V_{GS} = V_{BI}$, even though s cannot become greater than one or less than zero beyond these values. This causes convergence problems, and the resulting I-V characteristics are incorrect at low and high $V_{GS}$ values. Furthermore, as was noted in chapter 8.7 about the Statz model, a square root expression like $a \cdot (1 - s)$ models the dependence of the channel opening of gate voltage accurately at high $V_{GS}$ values, but not at low values where a quadratic expression is better.

These problems are solved in the VTT model by connecting the $s(V_{GS})$-curve to two parabolic expressions at $V_{GS} = 0.99 \cdot V_{TH}$ and $V_{GS} = 0.99 \cdot V_{BI}$. The values and derivatives of these expression are equal to those of the $s(V_{GS})$-curve at these points, and they equal one and zero somewhat beyond the points $V_{GS} = V_{TH}$ and $V_{GS} = V_{BI}$ respectively. This eliminates the convergence problems, and the MESFET characteristics are modeled more realistically at high $V_{GS}$ values than with other models, since the drain-source current can never exceed the saturation current $I_{DSsat}$. However, in the current version of the model, only the high-end smoothing is used, since the proper behaviour of the drain current at $V_{GS}$ values near $V_{TH}$ can be taken care of by a separate subthreshold model, as shown in the next chapter.

In future versions of this model, the function $s = f(V_{GS})$ may be changed to better model the $V_{GS}$ dependence of the device. It would be possible, for example, to introduce separate equations for different doping profiles. This should be done by replacing the $b(x) - V(x)$ relationship expressed in Eq. (51) with another, more flexible one, and deriving the channel current as shown in chapter 8.4.

A small drawback of the model is the abrupt change from linear behaviour to saturation, that is, $G_{m}$ and $G_D$ are not always continuous at $V_{DS} = V_{DSsat}$. This problem can be solved by polynomial interpolation between two I-V points on both sides of the saturation point, but so far the model seems to perform quite well in circuit simulations without this correction.
8.10 Other models

Many more GaAs MESFET models have been proposed than those presented in this work. Because of the continuous rapid development of the GaAs technology the demands on model accuracy and speed are growing. Some models are aimed more towards extremely accurate reproduction of device characteristics, while others, developed specifically for SPICE circuit simulation, take a more practical approach. To review all these models would be beyond the scope of this work; however, a few more will be briefly described:

The model of Golio et. al. [45] takes into consideration electron drift velocity saturation, channel length modulation and subthreshold current effects. The model parameters consist of material and geometric properties of the device rather than empirical values, except for the capacitance expressions. The model has been implemented in SPICE and demonstrated on analog and digital circuit simulations.

The model of Pelton et. al. [46] can be described as an improvement of the Shichman-Hodges model through empirical expressions. The model divides the $I_{DS}-V_{DS}$ characteristics of the MESFET into three regions, which are joined smoothly by parabolic functions. This method yields accurate results, especially in the linear region, while maintaining a model simplicity necessary for fast simulations. The model was developed at the University of California, Santa Barbara, and has since then been used successfully for the simulation of digital GaAs circuits.

The model of George et. al. [47] is a semi-heuristic model with single continuous expressions for drain current and capacitances that are valid for both subthreshold and above-threshold regions of device operation. The predictions of the model follow the actual measured device current and capacitance characteristics very accurately. However, a quite large number of empirical model parameters are required, so the extraction of these is not an easy task. The model has been implemented into SPICE.

The model of McCamant et. al. [48] improves upon the Statz model by making the threshold voltage a function of $V_{DS}$, which improves the drain conductance fit at low currents. The way $I_{DS}$ decreases at higher values of current and voltage, possibly due to self-heating, is also taken into account, and the gate voltage control expression exponent has been made an input parameter to facilitate the modeling of devices which do not follow the square law $I_{DS}-V_{GS}$ dependence. These modifications lead to more accurate predictions of small-signal parameters over a large range of bias conditions. The model has been implemented into SPICE.
8.11 Subthreshold models

For many digital applications of GaAs MESFETs, it is desirable to have high levels of integration. This means that the power dissipations in the devices must be kept small, which leads to designs where the MESFETs are operated at gate voltages close to cutoff. Therefore, it is critical that the device model accurately describes the characteristics also in the subthreshold region where $V_{GS} < V_{TH}$. This is also important for circuits which are sensitive to leakage currents, such as static RAMs.

But subthreshold modeling is not only important for simulation accuracy, it can also reduce the simulation time by promoting convergence. FET models in which $I_{DS}$ goes abruptly to zero when $V_{GS}$ decrease below $V_{TH}$ essentially have discontinuous $I_{DS}$-$V_{GS}$ characteristics. This means that the Newton-Raphson iteration algorithm used in most circuit simulators may fail, and the DC convergence will be severely hampered. Usually the circuit simulator has the capability to recover from a convergence problem, but the simulation time will nonetheless be significantly increased. Sometimes the problem can be avoided by specifying an input voltage or setting initial conditions that avoid a bias point initially in cutoff, but a circuit can also ‘drift’ into a nonconvergent state during a simulation. A smooth transition of the drain-source current through the threshold voltage will promote convergence and reduce computation time in most cases. Models that include some kind of subthreshold behaviour, even just a rough exponential decrease of $I_{DS}$ as a function of $V_{GS}$ for voltages below $V_{TH}$, will therefore reduce the circuit simulation time.

The subthreshold drain current of a GaAs MESFET has an exponential-like dependence of $V_{GS}$ until the current decreases below the substrate leakage current, as shown in Figure 26.

![Figure 26. Typical GaAs MESFET drain current subthreshold characteristics. Data is for an 1 x 10 µm ion-implanted depletion device with a threshold voltage of about -0.7 V. $V_{DS}$ is swept from 0.1 V to 3.1 V with 0.5 V increments.](image-url)
The slight gradual increase of the current with more negative $V_{GS}$ values after this point is due to leakage through the reverse-biased gate junction. The diode models that normally are used to model the gate junction can not account for this behaviour properly, but it may not have much significance for most circuits. However, here the reverse-biased behaviour of the gate diodes is modeled by replacing them with a resistance $R_{rev}$ in the reverse-biased region of operation. This is a rather crude approximation, but it seems to work better than the usual diode current equation, at least concerning MESFET subthreshold characteristics.

The problem in modeling the channel subthreshold current is that the drain-source current and its derivatives must be kept continuous, otherwise the Newton-Raphson iteration may fail and the circuit will exhibit convergence problems. Thus it is not advisable to just ‘glue on’ a subthreshold current expression to the model for the normal operation region. Subthreshold models that can duplicate the MESFET behaviour extremely well have been proposed, for example by Chang et. al. [49]. However, it is not clear how these models should be applied to achieve current and derivative continuity. Therefore, in this work it was decided to investigate simpler, empirical models, of which two showed some potential to be useful.

In both models, a drain-source leakage conductance, $G_{leak}$, is added to the equivalent circuit of the MESFET. It is the inverse of the drain-source resistance $R_{DS}$, and it has the following effect on the drain-source current and conductance:

\begin{align}
I_{DS}(\text{new}) &= I_{DS}(\text{old}) + G_{leak} V_{DS} \\
g_{D}(\text{new}) &= g_{D}(\text{old}) + G_{leak}
\end{align}

The first subthreshold modeling technique has been suggested by Vogel [50] and used for GaAs MESFETs (however, in a more complicated way than shown below) by P. George et.al. [47]. A gate voltage control expression such as

\begin{equation}
V_C = V_{GS} - V_{TH} 
\end{equation}

is replaced by

\begin{equation}
V_C = \frac{\ln(1 + e^{\eta(V_{GS} - V_{TH})})}{\eta}
\end{equation}

where $\eta$ is a parameter that determines the subthreshold slope. The expression used in Eq. (94) is based on the fact that $\ln(1 + e^x) \approx x$ when $x \gg 0$, and $\ln(1 + e^x) \approx e^x$ when $x \ll 0$. This method is applicable not only to channel current models containing the expression in (93), but to all models for which the threshold voltage is known or can be calculated. It is always possible to define a new gate voltage

\begin{equation}
V_{GSnew} = \frac{\ln(1 + e^{\eta(V_{GS} - V_{TH})})}{\eta} + V_{TH}
\end{equation}
that can then be used instead of $V_{GS}$ in the channel current model equations. Figure 27. shows results obtained with this subthreshold model.

![Graph showing measured and simulated drain current curves of a 1 x 10 µm ion-implanted depletion MESFET. $V_{DS}$ is swept from 0.1 V to 3.1 V with 0.5 V increments. The simulation has been performed using the tanh channel current model and the first subthreshold model.]

The model certainly improves circuit convergence, but does not produce very accurate subthreshold characteristics. The dependence of the drain current curves on $V_{DS}$ in the subthreshold region is determined only by the shape of the curves before the cutoff point. As can be seen from Figure 27., the subthreshold characteristics as a function of $V_{DS}$ is not very accurate.

The second model is a modified version of a subthreshold model proposed by Golio et. al. [45]: A subthreshold gate voltage, $V_{sub}$, is defined. $V_{sub}$ is given a slightly more positive value than $V_{TH}$. For $V_{GS}$ values larger than $V_{sub}$, the normal drain-source current equations are used, but for values below $V_{sub}$ the following equations are used:

$$I_{DS}(V_{GS}, V_{DS}) = I_{DS}(V_{sub}, V_{DS})e^{\frac{g_m(V_{sub}, V_{DS})}{I_{DS}(V_{sub}, V_{DS})}(V_{sub}-V_{GS})}$$  \hspace{1cm} (96)

$$g_m(V_{GS}, V_{DS}) = g_m(V_{sub}, V_{DS})e^{\frac{g_{m1}(V_{sub}, V_{DS})}{I_{DS}(V_{sub}, V_{DS})}(V_{sub}-V_{GS})}$$  \hspace{1cm} (97)

$$g_D(V_{GS}, V_{DS}) = g_D(V_{sub}, V_{DS})e^{\frac{g_{D1}(V_{sub}, V_{DS})}{I_{DS}(V_{sub}, V_{DS})}(V_{sub}-V_{GS})}$$  \hspace{1cm} (98)

As can be seen, both the drain-source current and it’s derivatives with respect to $V_{GS}$ and $V_{DS}$ are continuous at $V_{GS} = V_{sub}$.

**Parameter values:**

- $V_{TH}$: -0.7 V
- $\beta$: 9.38 $\cdot$ 10$^{-4}$ A/V$^2$
- $\alpha$: 4.57 1/N
- $\lambda$: 22.63 $\cdot$ 10$^{-2}$ 1/N
- $R_s$: 100.08 Ω
- $R_n$: 100.08 Ω
- $\eta$: 13.12 1/N
- $G_{m0}$: 1.14 $\cdot$ 10$^{-6}$ S
- $R_{rev}$: 35.87 $\cdot$ 10$^{12}$ Ω

Average absolute log($I_D$) error 0.0879
In order to model the shift in the starting gate voltage for the subthreshold region, two additional parameters $V_{\text{incr}}$ and $\eta$ are used. The effect of these parameters on the used value of $V_{\text{sub}}$ is as follows:

$$V_{\text{sub}}(\text{used}) = V_{\text{sub}}(\text{given}) + V_{\text{incr}} \tanh (\eta V_{DS})$$  \hspace{1cm} (99)

Figure 28. shows typical results from this subthreshold model. The simulation curves exhibit a much better fit than for the first model.

These subthreshold models were implemented in the program MESFETOPT and in SPICE, and they work with all drain current models. To summarize, the parameters are:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\eta$</td>
<td>ETA</td>
<td>subthreshold slope</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$G_{\text{leak}}$</td>
<td>GDLEAK</td>
<td>minimum drain-source conductance</td>
<td>S</td>
<td>W</td>
</tr>
<tr>
<td>$V_{\text{sub}}$</td>
<td>VSUB</td>
<td>subthreshold start gate voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{incr}}$</td>
<td>VINCR</td>
<td>subthreshold start voltage increment</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$\eta$</td>
<td>ETA</td>
<td>subthreshold slope</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>$G_{\text{leak}}$</td>
<td>GDLEAK</td>
<td>minimum drain-source conductance</td>
<td>S</td>
<td>W</td>
</tr>
</tbody>
</table>

Parameter values:

- $V_{TH} = -0.7$ V
- $\exp = 2.2$
- $\beta = 9.38 \times 10^{-4}$ A/V²
- $\alpha = 4.57$ 1/V
- $\lambda = 22.63 \times 10^{-2}$ 1/V
- $R_s = 100.08$ Ω
- $R_d = 100.08$ Ω
- $V_{\text{sub}} = -0.62$ V
- $V_{\text{incr}} = 0.097$ V
- $\eta = 0.081$ 1/V
- $G_{\text{leak}} = 1.14 \times 10^{-10}$ S
- $R_{rev} = 35.87 \times 10^{12}$ Ω

Average absolute log($I_D$) error = 0.0675
8.12 Schottky barrier diode models

The Schottky barrier diode is used in GaAs circuits both as the gate electrode in the MESFET and also by itself for both level-shifting and logic applications. The current of this type of diode, $I_D$, can be described as a function of the voltage over the diode, $V_D$, by an equation similar to that for a pn junction diode [51]:

$$I_D = I_S \left( e^{\frac{qV_D}{nkT}} - 1 \right)$$

(100)

where $q$ is the elementary charge, $n$ the ideality parameter, $k$ Boltzmann’s constant, $T$ the temperature and $I_S$ the diode saturation current. $I_S$ can be expressed as

$$I_S = WLA^*T^2e^{-\frac{q\phi_{BI}}{kT}}$$

(101)

where $W$ and $L$ the gate width and length, $A^*$ the effective Richardson constant and $\phi_{BI}$ the Schottky junction barrier height, which is not equal to the Schottky barrier voltage, $V_{BI}$, but is a function of it. This thermionic emission model adequately represents the I-V characteristics of GaAs Schottky diodes with doping levels up to about $5 \cdot 10^{17}$ 1/cm$^3$. For circuit simulation purposes, it sufficient to use Eq. (100) and treat $I_S$ as a model parameter.

The MESFET gate junction is modeled by two diodes with identical parameters, one connected to the gate and drain, the other one connected to the gate and source, as explained previously in chapter 8.2. This is shown in Figure 29.

![Figure 29. Simplified MESFET DC equivalent circuit showing gate diodes.](image)

Of course, this arrangement is not exactly valid at all bias values, which makes it difficult to get a good fit of simulation data to measurement data for high (> 1 V) $V_{GS}$ or $V_{GD}$ values, while limiting the diode parameters to physically sensible values. This is not due to any faults in the diode models or the extraction program, but rather to how the models are used. There is only one gate in reality, and the current through it is divided into $I_{GS}$ and $I_{GD}$ according to the corresponding voltages, $V_{GS}$ and $V_{GD}$. However, this problem is not easy to solve while maintaining a model simplicity necessary for circuit simulation.
One approximation that is usually employed in Schottky diode modeling is the assumption that the gate series resistance $R_G$ is a constant, independent of the forward gate current. In reality, the current distribution over the anode of a planar Schottky-barrier diode varies with the magnitude of the forward current, unlike the behaviour of a pn-diode. Because of current crowding toward that edge of the anode which is nearest to the cathode, there will be a current-dependent component in the series resistance. This so-called *Schottky spreading resistance*, denoted by $R_{SS}$, will have a maximum value at small diode currents, and decrease towards zero at larger currents. This behaviour can be expressed in closed form as [52]

$$\frac{R_{SS}}{R_{SS\text{max}}} = \frac{1}{2} \left( 1 - \tanh \left( \log_{10} \left( \frac{I_D}{I_{\text{inf}}} \right) \right) \right)$$

where $I_D$ is the diode forward current and $I_{\text{inf}}$ is the inflection current, at which the Schottky spreading resistance is equal to half its maximum value, $R_{SS\text{max}}$. Figure 30. shows $R_{SS}/R_{SS\text{max}}$ as a function of $I_D$.

![Normalized Schottky spreading resistance as a function of the ratio of diode forward current to inflection current, $I_{\text{inf}}$ [52].](image)

**Figure 30.** Normalized Schottky spreading resistance as a function of the ratio of diode forward current to inflection current, $I_{\text{inf}}$ [52].

One possible way to model the Schottky diode accurately is by using two diodes, with different values for the $I_S$ and $n$ parameters, instead of one [52]. Figure 31. shows the difference between this model and the ‘normal’ diode model.
Figure 31. Schottky diode modeling through the use of an auxiliary diode.

This strategy can be used in SPICE simulations to add the necessary elements to a MESFET subcircuit. The values of \( I_S \) and \( n \) for the auxiliary diode are calculated as:

\[
\begin{align*}
n_{aux} &= \frac{I_{inf}R_{SSmax} q}{6.435 \, kT} \\
I_{Saux} &= \frac{I_{inf}}{50}
\end{align*}
\]  

(103)  

(104)

This choice of values for \( I_{Saux} \) and \( n_{aux} \) has been empirically found to give a good fit to Eq. (102) [52].

Figure 32. MESFET DC equivalent circuit with accurate Schottky diodes.
However, when developing a new simulation model, it is more convenient to directly use a resistor with nonlinear I/V-characteristics like those described in Eq. (102). This method is used in the program MESFETOPT, and the resulting MESFET equivalent circuit is shown in Figure 32. Because of the complicated nature of Eq. (102), the simulation slows down a bit. If it is not desired to include the Schottky spreading resistance in the simulation, $R_{SS\text{max}}$ can be set to zero. This makes the program use the standard equivalent circuit. Due to the numerical difficulties, this model has not been implemented into SPICE yet.

The reverse-bias characteristics produced by Eq. (100) were found to be inadequate for simulating the MESFET subthreshold characteristics. Therefore, a reverse-bias leakage resistance, $R_{rev}$, was added. When the voltage over the diode becomes negative, the current is simply calculated from this resistance. Thus, the current will be continuous, but its derivative will have a discontinuity at the zero bias point. However, this discontinuity is small enough not to cause problems for the circuit simulator, and so convergence will not be slowed down appreciably. If the value of $R_{rev}$ is less than 1 kΩ, Eq. (100) will be used for all voltages.

In summary, the parameters for the gate Schottky diode model are:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>IS</td>
<td>saturation current</td>
<td>A</td>
<td>WL</td>
</tr>
<tr>
<td>$n$</td>
<td>N</td>
<td>ideality parameter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{rev}$</td>
<td>RREV</td>
<td>reverse-bias leakage resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
<tr>
<td>$R_{SS\text{max}}$</td>
<td></td>
<td>max. Schottky spreading resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
<tr>
<td>$I_{inf}$</td>
<td></td>
<td>Inflection current</td>
<td>A</td>
<td>WL</td>
</tr>
<tr>
<td>$R_G$</td>
<td>RG</td>
<td>gate resistance</td>
<td>Ω</td>
<td>1/W</td>
</tr>
</tbody>
</table>
8.13 Gate-source and gate-drain capacitance models

This chapter deals with the modeling of the depletion layer capacitances of the MESFET. The device exhibits also parasitic gate-source, gate-drain and drain-source capacitances that have two main causes: The fringing capacitance that arises from the lateral extension of the depletion layer beyond the edge of the gate electrode, and the geometric fringing capacitances between the coplanar gate, drain and source metal strips on the GaAs surface. However, these capacitances are essentially constant, and can thus be added directly to the equivalent circuit as shown in Figure 33.

Figure 33. Schematic cross-section of a MESFET showing the origins of the parasitic capacitances.

The simplest, and perhaps still most often used depletion layer capacitance model is the diode model, which is a charge nonconserving capacitance model. The gate-source and gate-drain capacitances of the MESFET are modeled as Schottky diode capacitances:

\[
V_{GS} \leq FC \cdot V_{BI}
\]

\[
C_{GS} = \frac{C_{GS0}}{M} \left(1 - \frac{V_{GS}}{V_{BI}}\right)
\]

\(105\)

\[
V_{GS} > FC \cdot V_{BI}
\]

\[
C_{GS} = \frac{C_{GS0}}{(1 - FC) (1 + M)} \left(1 - FC (1 + M) + M \frac{V_{GS}}{V_{BI}}\right)
\]

\(106\)

and

\[
V_{GD} \leq FC \cdot V_{BI}
\]

\[
C_{GD} = \frac{C_{GD0}}{M} \left(1 - \frac{V_{GD}}{V_{BI}}\right)
\]

\(107\)
\[ V_{GD} > FC \cdot V_{BI} \]

\[ C_{GD} = \frac{C_{GD0}}{(1 - FC) (1 + M)} \left( 1 - FC \left( 1 + M \right) + M \frac{V_{GD}}{V_{BI}} \right) \tag{108} \]

The capacitance equations have a singularity at the voltage \( V_{BI} \). To avoid this, the capacitances are approximated by a straight line for voltages exceeding \( FC \cdot V_{BI} \), where \( FC \) is a model parameter that is usually given the value 0.5.

The parameters for this model are:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{GS0} )</td>
<td>CGSO</td>
<td>zero bias gate-source capacitance</td>
<td>F/m²</td>
<td>WL</td>
</tr>
<tr>
<td>( C_{GD0} )</td>
<td>CGDO</td>
<td>zero bias gate-drain capacitance</td>
<td>F/m²</td>
<td>WL</td>
</tr>
<tr>
<td>( V_{BI} )</td>
<td>VBI</td>
<td>gate Schottky barrier</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( M )</td>
<td>M</td>
<td>gate junction grading coefficient</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FC</td>
<td>FC</td>
<td>forward bias depletion capacitance coefficient</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unfortunately, aside from being charge nonconserving, this model has some serious shortcomings. It is completely inadequate for gate voltages smaller than the threshold voltage, because it yields a nonzero capacitance at these voltages. The capacitance should be equal to zero because the total charge in the section of the channel under the gate does not change after cutoff. Carrier velocity saturation is also not taken into account. Due to this effect, \( C_{GS} \) increases in the saturation region and \( C_{GD} \) drops rapidly as the device enters saturation. And finally, the model is not symmetric with respect to \( V_{DS} \), i.e. in the inverse region the capacitances will be calculated wrongly.

![Figure 34](image.png)

**Figure 34.** Gate-source capacitance of a 1 x 20 \( \mu \)m DMESFET according to the diode capacitance model. The drain-source current has been calculated with the Statz model, but as the parasitic resistances have zero values, this has no effect on the capacitance values.
The Statz capacitance model [37,53,54] is a charge-based model that corrects the deficiencies of the diode capacitance model. As the theory behind this model is quite complex, only the resulting capacitance equations are shown here:

\[
C_{GSD} = C_{GSO} \frac{K_1K_2}{\sqrt{1 - \frac{V_{new}}{V_{BL}}}} + C_{GD0}K_3 
\]

(109)

\[
C_{GDD} = C_{GSO} \frac{K_1K_3}{\sqrt{1 - \frac{V_{new}}{V_{BL}}}} + C_{GD0}K_2 
\]

(110)

where

\[
K_1 = \frac{1}{2} \left( 1 + \frac{V_{eff} - V_{TH}}{\sqrt{(V_{eff} - V_{TH})^2 + \delta^2}} \right) 
\]

(111)

\[
K_2 = \frac{1}{2} \left( 1 + \frac{V_{GS} - V_{GD}}{\sqrt{(V_{GS} - V_{GD})^2 + \Delta^2}} \right) 
\]

(112)

\[
K_3 = \frac{1}{2} \left( 1 - \frac{V_{GS} - V_{GD}}{\sqrt{(V_{GS} - V_{GD})^2 + \Delta^2}} \right) 
\]

(113)

\[
V_{eff} = \frac{1}{2} (V_{GS} + V_{GD} + \sqrt{(V_{GS} - V_{GD})^2 + \Delta^2}) 
\]

(114)

\[
V_{new} = \min\left(V_{max}, \frac{1}{2} (V_{eff} + V_{TH} + \sqrt{(V_{eff} - V_{TH})^2 + \delta^2}) \right) 
\]

(115)

The parameters for this model are:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE name</th>
<th>Parameter</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{GSO}$</td>
<td>CGSO</td>
<td>asymptotic gate-source capacitance</td>
<td>F</td>
<td>WL</td>
</tr>
<tr>
<td>$C_{GD0}$</td>
<td>CGDO</td>
<td>asymptotic gate-drain capacitance</td>
<td>F</td>
<td>WL</td>
</tr>
<tr>
<td>$V_{BL}$</td>
<td>VBI</td>
<td>gate Schottky barrier</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>VTO</td>
<td>threshold (turn-off) voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{max}$</td>
<td></td>
<td>maximum forward bias</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$\delta$</td>
<td></td>
<td>beyond-pinchoff capacitance interpolation voltage range</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$\Delta$</td>
<td></td>
<td>transition width parameter</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

The transition width parameter $\Delta$ is not a user-definable parameter but is derived from the drain current saturation voltage, $V_{DSat}$, of the channel current model in use. For the JFET model used in the program MESFETOPT, $\Delta$ will equal $E_{VGS}V_{GS} - V_{TH}$, and for the tanh, Statz and cubic models $1/\alpha$. The VTT model automatically calculates a new $V_{DSat}$ value for each new gate voltage, and $\Delta$ is given this value. In the cubic model, the threshold voltage $V_{TH}$ is a function of the drain voltage, and this is also taken into account in this capacitance model. Also note that the parameter $V_{max}$ should have a value smaller than $V_{BL}$, otherwise the results of Eqs. (109) and (110) can become imaginary. However, this error is prevented in the program code, and in
SPICE $V_{\text{max}}$ has a constant value of 0.5. Figure 35. shows the behaviour of $C_{GS}$ according to this capacitance model.

![Graph of C GS vs V GS and V DS](image)

**Figure 35.** The behaviour of $C_{GS}$ as a function of a) $V_{GS}$ and b) $V_{DS}$ according to the Statz capacitance model.

Finally, the delay that is observed between the change in the gate-source voltage and the corresponding change in the drain-source current can be modeled as stored charge

$$Q_{DS} = \tau I_{DS}$$ (116)

and

$$Q_D = Q_{DS}, Q_S = -Q_{DS}$$ (117)

where $\tau$ represents the transit time for electrons in the section of the channel under the gate. The corresponding transit time capacitance can then be expressed as

$$C_{\tau} = \tau \frac{dI_{DS}}{dV_{GS}} = \tau g_m$$ (118)

This effect is also included in the capacitance models of MESFETOPT.
9. Parameter extraction

9.1 Extraction methods

Parameter extraction methods may be divided into two classes: Direct methods and indirect methods. In direct methods, parameters are usually obtained sequentially, from measurements of test devices or circuits. Typically, each parameter requires a specific test circuit or a transistor of suitable size. For example, the drift mobility of the GaAs MESFET channel may be measured using a so-called FATFET (a MESFET with a very long gate, typically 20 - 250 µm). The calculations required in direct methods are usually not too complicated, which makes it possible (though not desirable) to perform the extraction manually, without the use of a computer. In indirect methods, the values of all parameters are extracted simultaneously by a computer. Programs for this purpose use nonlinear optimization techniques to find a minimum for the difference between the simulated and measured transistor characteristics.

The main advantage of direct methods is that they are fast, and thus potentially suitable for real time process control. Unfortunately, direct methods have several disadvantages. First, they ignore interactions between parameters, making it difficult to get a good fit for a group of transistors with large variations in the W and L values. This is a direct consequence of the fact that typically the value of each parameter has been measured from a single transistor at a particular operating point. Second, direct methods are model specific, i.e. each model requires a parameter extraction method of its own. In fact, each parameter requires an extraction method of its own. Often the parameters are deeply embedded in the model equations, so that it becomes very difficult to devise a suitable measurement method which would yield the required parameter value directly. To be really useful, direct parameter extraction methods require test structures containing a large number of devices of different sizes, which should be selected to form a reasonably dense grid over the region in the WL plane to be used in design work. Each node in this grid would be characterized by a unique set of model parameters, and the designer should choose the parameter set of the node closest to the transistor he wishes to use. Obviously, this method is thorough, but inconvenient, and therefore less desirable.

The manual extraction of SPICE MESFET model parameters from a set of $I_{DS}$-$V_{DS}$ curves may also be considered a direct method. It’s possible to get a rough fit quite fast, at least for models that are relatively simple and have some physical meaning, like the tanh and Statz models. However, there are some problems, like taking the parasitic resistances into account, which may demand the use of a computer for evaluating the equations. Therefore, to get a really good fit in a reasonable time, indirect computer extraction methods must be used.

Indirect parameter extraction methods are inherently free of the problems associated with direct methods. By definition, they find an optimal parameter set for a given model, and this parameter set gives the best possible fit (in some sense) to the measured data, which may include the characteristics of several devices. In principle,
only some type of transistor curve tracer is needed to obtain this data. Indirect methods are also model independent. The programmer only needs to write a subroutine for calculating the transistor currents for a certain model, and the actual extraction algorithm is the same for all models. The main disadvantage of indirect methods is their relative slowness. For example, it may take several hours to find a good parameter set for some of the SPICE MESFET models, using a desktop computer. Naturally, using a large mainframe computer will speed up the process considerably, but one might not always be available, and it’s very convenient to be able to control the measurements and perform the extraction on the same computer. Besides, microcomputer CPU time costs virtually nothing, and the machine may be left running overnight. In any case, the goodness of the fit obtained with these methods is likely to be superior over those obtained by direct measurements or manual extraction methods. Indirect parameter extraction methods will be discussed further in chapter 9.3.

9.2 Manual extraction

There is not much to be said generally about manual extraction, because the extraction method must be tailored to a specific model, i.e. every model has its own extraction method. Some similarities do exist, for example, models containing the expression

\[ \beta (V_{GS} - V_{TH})^n \]  

(119)

can be treated by plotting \( I_{DS}^{1/n} \) as a function of \( V_{GSI} = V_{GS} - R_S I_{DS} \). The effect of the channel length modulation parameter \( \lambda \) can be removed by extrapolating the saturation slope to \( V_{DS} = 0 \), as shown in the figure below.

![Figure 36. Extraction of \( \beta \) and \( V_{TH} \) from the MESFET I-V characteristics.](image)
RS is selected in such a way that the plot is a straight line. The slope of the line will be \( \beta^{1/n} \) and the intercept with the \( V_{GS} \) axis provides \( V_{TH} \). However, this method can give ambiguous results, so ideally the values of \( R_S \) and \( R_D \) should be known from a separate measurement. If this is the case, it is possible to use the *intrinsic* voltages in all extraction calculations. A great number of methods for the measurement of the MESFET parasitic resistances have been published [55-59]. The method described in [59] has been coded as part of a measurement program and used in this work.

The channel length modification coefficient \( \lambda \) present in many models is simply calculated from the slope of a \( I_{DS}-V_{DS} \) curve in the saturation region, and the tanh constant \( \alpha \) in the Curtice models and the Statz model is calculated from the slope of the same curve, but in the linear region. This can be expressed as

\[
\alpha, \lambda = \frac{I_{DS2} - I_{DS1}}{V_{DS2}I_{DS1} - V_{DS1}I_{DS2}}
\]

(120)

Calculating the average value over a couple of different \( V_{GS} \) points may also yield more consistent results for these parameters.

An important point to keep in mind is to avoid using large \( I_{DS} \) values for the extraction, because in that case thermal effects (i.e. electron mobility and saturation velocity degradation) may influence the results. The gate-source voltage must also be small enough (< 0.5 - 0.7 V) to ensure that gate forward conduction does not have to be taken into account. The gate diode parameters can be extracted separately from a gate current measurement with the source and drain grounded. The method for this can be found in [55], and it is also quite easy to implement in a computer program.

In the program MESFETOPT algorithms that use these techniques together with linear regression and polynomial fitting have been developed. The purpose of these algorithms is to extract starting values for the model parameters, so that the actual nonlinear optimization will result in an accurate fit faster. In some cases, the results produced by these algorithms can be amazingly accurate, especially for the simpler models.

### 9.3 Computer extraction methods

In indirect computer extraction methods an objective function describing the “goodness” of the fit is minimized using nonlinear optimization techniques. The objective function is usually a suitably weighted sum of the squares of the differences between simulated and measured data. Mathematically this can be described as follows:

\[
S = \tilde{f}^T \cdot \tilde{f}
\]

(121)

where \( \tilde{f}^T \) stands for the transpose, or corresponding row vector of \( \tilde{f} \), which can be expressed as

\[
f(i) = w(i) (D_{calc}(i) - D_{meas}(i))
\]

(122)
Here $S$ is the objective function, $\overline{f}$ is the error or residual vector, $\overline{w}$ is a suitable weight vector and $i$ is the vector index. $D_{\text{calc}}$ and $D_{\text{meas}}$ are the calculated and measured data points, respectively. Typically, $w(i)$ is the inverse of $D_{\text{meas}}(i)$, in which case we get the relative error, but it may be a function of, for example, gate width and/or length, $V_{GS}$, $V_{DS}$, and $D_{\text{meas}}(i)$. Another way of calculating the error vector is to simply take either the absolute or relative differences between measured and simulated data as positive values:

$$f_{\text{abs}}(i) = w(i)|D_{\text{calc}}(i) - D_{\text{meas}}(i)| \quad (123)$$
$$f_{\text{rel}}(i) = w(i)\left|\frac{D_{\text{calc}}(i) - D_{\text{meas}}(i)}{D_{\text{meas}}(i)}\right| \quad (124)$$

From these the objective function can be calculated in many different ways, but the best measure of the fit is perhaps given by either the error sum, the average error, or the maximum error:

$$S_{\text{sum}} = \sum_{i=1}^{N} f(i) \quad (125)$$
$$S_{\text{ave}} = \frac{S_{\text{sum}}}{N} \quad (126)$$
$$S_{\text{max}} = \text{MAX}(f(i)) \quad (127)$$

Here, $N$ is the number of data points, and $f(i)$ is either $f_{\text{abs}}(i)$ or $f_{\text{rel}}(i)$. When one of these values reaches the specified limit, the optimization can be halted. These objective functions are used in the program MESFETOPT.

However, suppose this does not occur in a reasonable time, or in the worst case, never. The used model may be too simple, and so the wanted fit will never be reached. Clearly, we need to have some way of determining the point of diminishing returns for the optimization. One way to do this is to look at the variance of the fits for the different parameter value groups in the optimization. Usually, regardless of the optimization method used, a number $n+1$ of parameter groups will exist simultaneously during the optimization, where $n$ is the number of parameters to be optimized. The variance $V$ of the different fits that these groups give can then be calculated as

$$V = \frac{1}{n} \left( \frac{1}{n+1} \sum_{j=1}^{n} S(j)^2 - \frac{1}{n+1} \left( \sum_{j=1}^{n} S(j) \right)^2 \right) \quad (128)$$

where $S$ is calculated using either Eq. (125), (126) or (127). Now, as the optimization proceeds, the variance of the fit for the different parameter groups will decrease as the parameter values converge in the direction of the minimum of the objective function. Consequently, a minimum allowed variance can be set as a second halting criterion for the optimization. Of course, other criterions such as the number of evaluations of the semiconductor equations or CPU time can also be used.
The data used for optimization is usually the drain current, \( I_D \), or capacitance data for optimization of the capacitance model parameters. However, for some channel current models it may be necessary to use a combination of, for example \( I_D \) and \( G_D \), to ensure that the slope of the \( I_D-S-V_D \) characteristics is reproduced correctly. In the program MESFETOPT any one of the quantities \( I_D \), \( I_S \), \( I_G \), \( G_D \), or \( G_m \) can be used as optimization data, and the first three currents can be used together with either \( G_D \) or \( G_m \). For the optimization of capacitance model parameters, \( C_{GS} \) or \( C_{GD} \) can be used.

Typically, in semiconductor device parameter extraction, the global minimum of the objective function lies outside the space of physically sensible values. The easiest way to introduce constraints is via a suitable transformation of variables. Generally, each parameter \( x_i \) is subject to a constraint

\[
I_i \leq x_i \leq u_i
\]

where \( I_i \) and \( u_i \) are the smallest and largest allowed values of \( x_i \). The transformation can be performed as follows [63]:

\[
x_i = \frac{I_i + u_i + (I_i - u_i) \sin (y_i)}{2}
\]

It is readily seen that this equation transforms the constrained parameter domain \( x \) to an unconstrained parameter domain \( y \), and now the minimization of the objective function may be carried out with respect to the parameter set \( y \) using unconstrained optimization techniques.

Over the years quite a large number of optimization algorithms have been developed [60,61]. They can roughly be divided into two groups: Direct methods which only require the function value and not the first derivatives, and gradient methods which do require the first derivatives of the function to be computed, as well as the function itself. Gradient methods are potentially more efficient than direct methods, but they are also generally much more complicated than direct methods. The NMS (Nelder and Mead Simplex) method [62] is a direct method which the author has found to perform quite satisfactorily, at least for problems with no more than 20 variables. Therefore, this method has been used in MESFETOPT. An excellent review of optimization algorithms for semiconductor device parameter optimization can be found in [63].
10. SPICE model implementation

The models described in this work have been implemented into a widely used commercial SPICE version, *PSpice* from MicroSim Corporation. This program can be installed on many different computers, but the implementation was done on a personal computer (PC) version of the program, release 4.3. As the program is written in the C programming language, however, there should not be any problems in moving the new program code to other PSpice versions.

By purchasing a special option with PSpice, *Device Equations*, the user gets the source code for the semiconductor models and the rest of the program as object code files. The source code can be modified, and then by compiling and linking it with the rest of the object files, a new, customized PSpice version can be created.

The available semiconductor devices in PSpice actually include the GaAs MESFET, and in version 4.3 two models can be used for this device; the hyperbolic tangent model or the Statz model [64]. In this work the program code has been modified so that all the five GaAs channel current models described earlier in the text can be used in PSpice. The two subthreshold models have also been implemented, and either the diode or Statz capacitance model can be used with any one of the channel current models. This is not possible in the original code. The modification of the diode model to include the Schottky spreading resistance has not been carried out so far, due to the inherent non-analytical nature of the equations for this effect.

The wanted channel current model is chosen by giving the model parameter LEVEL the appropriate value, in the range 1 - 5. The new parameters CAPOP and SUBOP control the capacitance and subthreshold models, respectively. CAPOP can be given a value of 1 or 2, and for SUBOP the allowed values are 0, 1, and 2.

For completeness, all the possible parameters for the MESFET in the modified PSpice version are listed below. PSpice uses a scaling factor called AREA, which is equivalent to the device width in micrometers, for GaAs MESFETs. The scaling of the parameters by this factor is also shown.

<table>
<thead>
<tr>
<th>Name</th>
<th>Parameter</th>
<th>Default value</th>
<th>Units</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>polynomial coefficient 0</td>
<td>0.0</td>
<td>A</td>
<td>AREA</td>
</tr>
<tr>
<td>A1</td>
<td>polynomial coefficient 1</td>
<td>0.0</td>
<td>A/V</td>
<td>AREA</td>
</tr>
<tr>
<td>A2</td>
<td>polynomial coefficient 2</td>
<td>1.0</td>
<td>A/V^2</td>
<td>AREA</td>
</tr>
<tr>
<td>A3</td>
<td>polynomial coefficient 3</td>
<td>0.0</td>
<td>A/V^3</td>
<td>AREA</td>
</tr>
<tr>
<td>ALPHA</td>
<td>saturation voltage parameter</td>
<td>2.0</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>AF</td>
<td>flicker noise exponent</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>doping tail extending parameter</td>
<td>0.3</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>BETA</td>
<td>transconductance coefficient</td>
<td>0.1</td>
<td>A/V^2</td>
<td>AREA</td>
</tr>
<tr>
<td>BETATCE</td>
<td>BETA exponential temp. coeff.</td>
<td>0.0</td>
<td>%/°C</td>
<td></td>
</tr>
<tr>
<td>CAPOP</td>
<td>capacitance model selector</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDS</td>
<td>drain-source capacitance</td>
<td>0.0</td>
<td>F</td>
<td>AREA</td>
</tr>
<tr>
<td>CGD</td>
<td>zero-bias gate-drain capacitance</td>
<td>0.0</td>
<td>F</td>
<td>AREA</td>
</tr>
<tr>
<td>CGS</td>
<td>zero-bias gate-source capacitance</td>
<td>0.0</td>
<td>F</td>
<td>AREA</td>
</tr>
</tbody>
</table>
Some details remain before the models are complete. The temperature behaviour of BETA and VTO has not so far been extended to affect the parameters A0 - A3, U0, IDSAT and VP. The Schottky spreading resistance model should also be added to both the MESFET and diode model in PSpice. However, these are minor additions, so at this stage the implemented GaAs models can be considered fully functional.
11. Simulation results

11.1 DC analysis speed

The implemented models were compared in terms of the time required to simulate the DC I-V characteristics of the 1 x 20 µm DMESFET that was used as an example device in chapter 8. However, a lot more data points were used in order to emphasize speed differences between the models, and the $V_{GS}$ range was -0.7 ... 0.5 V. The simulation times are shown relative to that of the plain JFET model.

Results from MESFETOPT (403 data points):

<table>
<thead>
<tr>
<th>Model</th>
<th>Relative simulation time</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFET</td>
<td>1.0</td>
</tr>
<tr>
<td>JFET with extra voltage source</td>
<td>1.05</td>
</tr>
<tr>
<td>Hyperbolic tangent</td>
<td>1.08</td>
</tr>
<tr>
<td>Hyperbolic tangent with variable gate exponent</td>
<td>1.12</td>
</tr>
<tr>
<td>Statz</td>
<td>2.12</td>
</tr>
<tr>
<td>Cubic</td>
<td>1.13</td>
</tr>
<tr>
<td>VTT</td>
<td>2.89</td>
</tr>
</tbody>
</table>

Results from PSpice (3751 data points):

<table>
<thead>
<tr>
<th>Model</th>
<th>Relative simulation time</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFET</td>
<td>1.0</td>
</tr>
<tr>
<td>JFET with extra voltage source</td>
<td>1.0</td>
</tr>
<tr>
<td>Hyperbolic tangent</td>
<td>1.05</td>
</tr>
<tr>
<td>Hyperbolic tangent with variable gate exponent</td>
<td>1.05</td>
</tr>
<tr>
<td>Statz</td>
<td>1.06</td>
</tr>
<tr>
<td>Cubic</td>
<td>1.06</td>
</tr>
<tr>
<td>VTT</td>
<td>1.15</td>
</tr>
</tbody>
</table>

The trend is the same for both comparisons, i.e. the simulation time increases for more complicated models, but the differences are much smaller for the PSpice test. This may be due to programming language differences and the undoubtedly superior circuit solving algorithms of PSpice. So, at least for DC analysis, the time penalty for more accurate models does not seem to be very hard.

In Figure 37. the same I-V characteristics as in chapter 8. are shown, but now generated using the new PSpice version.
Figure 37. I-V characteristics of the example 1 x 20 µm DMESFET simulated with PSpice. a) JFET model, b) JFET model with extra voltage source, c) tanh model, d) tanh model with variable gate exponent, e) Statz model, f) cubic model and g) VTT model.
11.2 Transient analysis example

The new PSpice version was used to simulate a fabricated and measured DCFL logic divide-by-two circuit. This circuit is simply a feedback flipflop gate that consists of 6 1 x 11 \( \mu \)m DMESFETs and 16 1 x 29 \( \mu \)m EMESFETs. The circuit was not equipped with output buffers, which meant that the operational frequency was limited to about 100 MHz because of capacitive and resistive oscilloscope probe loading during the on-wafer measurement. Figure 38. shows the simplified layout of the chip and the measurement arrangement.

![Figure 38. Measurement arrangement for a GaAs E/D DCFL logic divide-by-two circuit with no buffering.](image)

Figure 39. shows the measured input clock waveform and the output waveform.

![Figure 39. Measured input and output waveforms of DCFL divider](image)
As the basis for the simulation the standard modeling technique of the foundry was used. This involves using a subcircuit containing resistors, capacitors, diodes and a JFET with a voltage-controlled voltage source connected to the gate, as mentioned in chapter 8.5. The circuit was first simulated using this technique, and then the voltage source and the JFET were substituted by the modified GaAs MESFET device using the different models. The model parameters were optimized with the standard technique JFET I-V characteristics as the goal. This was done in order to be able to compare the models in terms of functionality and speed as fairly as possible. For the cubic model, it was not possible to get an acceptable fit, so this model was left out of the comparison. The input file containing the circuit description and all the models is listed in Appendix 1.

The speed comparison results are now shown relative to that of the standard modeling technique:

<table>
<thead>
<tr>
<th>Model</th>
<th>Relative simulation time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard JFET subcircuit</td>
<td>1.0</td>
</tr>
<tr>
<td>Modified GASFET - JFET</td>
<td>1.0</td>
</tr>
<tr>
<td>Modified GASFET - tanh</td>
<td>1.08</td>
</tr>
<tr>
<td>Modified GASFET - tanh &amp; subthreshold model 1</td>
<td>1.03</td>
</tr>
<tr>
<td>Modified GASFET - tanh &amp; subthreshold model 2</td>
<td>1.04</td>
</tr>
<tr>
<td>Modified GASFET - Statz</td>
<td>1.01</td>
</tr>
<tr>
<td>Modified GASFET - VTT</td>
<td>1.04</td>
</tr>
</tbody>
</table>

These results are quite interesting. Firstly, the penalty of the tanh function can be seen clearly as the 8 percent increase in simulation time for the hyperbolic tangent model. However, the use of the subthreshold models clearly make the simulation converge faster by a factor of 5 and 4 percent, respectively. As this circuit is not an especially difficult one to simulate, larger gains are to be expected for more difficult cases.

As the VTT model involves quite a lot of time-consuming calculations, one would have expected it to perform worst of all the models, but this is clearly not the case. This phenomena has been investigated thoroughly, but no explanation has been found.

As the model parameters were all optimized using the same goal, the simulation results for all the models are very similar, as shown in Figure 40. of the next page. The simulated results are somewhat too optimistic, which probably reflects the fact that the probe loading was underestimated.

It may be that the test circuit used in this work is too small to clearly show differences in simulation speed for the models. However, the tests conducted here show that it is feasible to simulate small ‘building blocks’ of large digital circuits using more accurate models without unreasonable time penalties.
Figure 40. Results from PSpice transient analysis. a) standard modeling technique, b) JFET, c) tanh, d) Statz and e) new VTT model.
12. Conclusions

The rapid developments in GaAs processing technology of today place increasingly stronger demands on device model accuracy and speed. Model development is one of the key factors in the efforts to increase the integration level of existing GaAs technologies.

In this work the most popular GaAs MESFET models for digital IC simulation of today were presented and discussed. A new model was described, and also two ways of modeling the subthreshold region of the device. Model parameter extraction and optimization was also discussed. All the reviewed models were implemented into a SPICE circuit simulator version.

Having access to several models in the same simulator can be very useful, because different simulation tasks often place varying emphasis on accuracy and speed. The differences in simulation time for the implemented models were found to be almost insignificant, at least for a comparatively small circuit, like a flipflop. This means that more accurate models can be used successfully for analyzing small ‘building blocks’ of larger circuits. It was also found that the subthreshold models improve circuit convergence significantly.
13. References

1. D. Kiefer, J. Heightley
   CRAY-3: A GaAs Implemented Supercomputer System
   Proceedings of the IEEE GaAs IC Symposium
   Portland, Oregon, 13 - 16 October 1987, pp. 3 - 6

2. D.L. Harrington et. al.
   A GaAs 32-Bit RISC Microprocessor
   Proceedings of the IEEE GaAs IC Symposium
   Nashville, Tennessee, 6 - 9 November 1988, pp. 87 - 90

3. B. Travis
   Large-scale GaAs ICs Challenge Bipolar ICs in Speed, Power, Cost
   EDN magazine
   vol. 35, no. 14, 1990, pp. 80 - 86

4. M. Andersson, M. Åberg, H. Pohjonen
   Simultaneous Extraction of GaAs MESFET Channel and Gate Diode Parameters and its Application to Circuit Simulation
   Proceedings of IEEE Int. Symp. on Circuits and Systems
   Espoo, Finland, 7 - 9 June 1988, pp. 2601 - 2604

5. J. Ahopelto, H.P. Kattelus, J. Saarilahti, I. Suni
   GaAs/InAs Heterostructures Grown by Atomic Layer Epitaxy
   Springer-Verlag, pp 169 - 172

6. H. Kroemer
   Heterostructure Bipolar Transistors and Integrated Circuits
   Proceedings of the IEEE
   vol. 70, no. 1, 1982, pp. 13 - 25

7. M.F. Chang
   Self-aligned AlGaAs/GaAs Heterostructure Bipolar Transistors with Improved High-Speed Performance
   Abstract for the 45th Annual Device Research Conf.
   Santa Barbara, California, 22 - 24 June 1987
   IEEE Trans. on Electron Devices
   vol 34, no. 11, 1987, pp. 2369

8. W. Shockley
   A Unipolar Field-Effect Transistor
   Proceedings of the IRE
   vol. 40, 1962, pp. 1365 - 1376

   General Theory for Pinched Operation of the Junction-Gate FET
   Solid-State Electronics
   vol. 12, no. 7, 1969, pp. 573 - 589
<table>
<thead>
<tr>
<th></th>
<th>Authors</th>
<th>Title</th>
<th>Publisher</th>
<th>Volume/Issue</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>C. Kocot, C.A. Stolte</td>
<td>Backgating in GaAs MESFET’s</td>
<td>IEEE Trans. on Microwave Theory and Techniques</td>
<td>vol. 30, no. 7</td>
<td>pp. 963 - 968</td>
</tr>
<tr>
<td>12</td>
<td>S. Sriram, M.B. Das</td>
<td>An Experimental Study of Backgating Effects in GaAs MESFETs</td>
<td>Solid-State Electronics</td>
<td>vol. 28, no. 10</td>
<td>pp. 979 - 989</td>
</tr>
<tr>
<td>13</td>
<td>E. Siren</td>
<td>Galliumarsenidi-MESFET:n Valmistus ja Ominaisuuksiens Tutkiminen</td>
<td>Master’s Thesis, Electron Physics Laboratory, Department of Electrical Engineering Helsinki University of Technology Otaniemi, Finland, 1990, 102 pages</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>A.M. Pavio</td>
<td>Design and Application of Monolithic Microwave GaAs ICs: Lecture 3 - Non-linear and Special Purpose Circuit Design</td>
<td>IEEE GaAs IC Symposium Short Course</td>
<td>Portland, Oregon, 13 - 16 October 1987</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>L.E. Larson</td>
<td>An Improved GaAs MESFET Equivalent Circuit Model for Analog Integrated Circuit Applications</td>
<td>IEEE Journal of Solid-State Circuits</td>
<td>vol. 22, no. 4</td>
<td>pp. 567 - 574</td>
</tr>
</tbody>
</table>
19. P.C. Canfield, J. Medinger, L. Forbes

**Buried-Channel GaAs MESFET’s with Frequency-Independent Output Conductance**
*IEEE Electron Device Letters*
vol. 8, no. 3, 1987, pp. 88 - 89

20. W.S. Lee, J. Mun

**Improved Negative Feedback Technique to Reduce Drain Conductance of GaAs MESFETs for Precision Analogue ICs**
*Electronics Letters*
vol. 23, no. 13, 1987, pp. 705 - 707

21. M. Rocchi, B. Gabillard

**GaAs Digital Dynamic IC’s for Applications up to 10 GHz**
*IEEE Journal of Solid-State Circuits*
vol. 18, no. 3, 1985, pp. 369 - 376

22. J. Jensen, L.G. Salmon, D.S. Deakin, M.J. Delaney

**26 GHz GaAs Room-Temperature Dynamic Divider Circuit**
*Proceedings of the IEEE GaAs IC Symposium*
Portland, Oregon, 13 - 16 October 1987, pp. 201 - 204

23. S.I. Long, S.E. Butner

**Gallium Arsenide Digital Integrated Circuit Design**
*McGraw-Hill, 1990*
chapter 4.3, pp. 231 - 239

24. R.L. Van Tuyl, C.A. Liechti

**High Speed Integrated Logic with GaAs MESFETs**
*IEEE Journal of Solid-State Circuits*
vol. 9, no. 5, 1974

25. R.L. Van Tuyl, C.A. Liechti, R.E. Lee, E. Gowen

**GaAs MESFET Logic with 4-GHz Clock Rate**
*IEEE Journal of Solid-State Circuits*
vol. 12, no. 5, 1977, pp. 485 - 496

26. L.W. Nagel, D.O. Pederson

**Simulation Program with Integrated Circuit Emphasis (SPICE)**
*Electronics Research Laboratory Rep. No. ERL-M382*  
University of California, Berkeley, 1973

27. G. Bischoff, P. Krusius

**Technology Independent Device Modeling for Simulation of Integrated Circuits for FET Technologies**
*IEEE Trans. on Computer-Aided Design*
vol. 4, no. 1, 1985, pp. 99 - 110

28. R. Goyal, N. Scheinberg

**GaAs MESFET Model for Precision Analog IC Design**
*VLSI Systems Design*
vol. 8, no. 5, 1987, pp. 52 - 55
<table>
<thead>
<tr>
<th>No.</th>
<th>Author(s)</th>
<th>Title</th>
<th>Publisher</th>
<th>Edition</th>
<th>Chapter</th>
<th>Page(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>M. Shur</td>
<td>GaAs Devices and Circuits</td>
<td>Plenum Press, 1987</td>
<td></td>
<td>chapter 7, pp. 313</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>A. Rode</td>
<td>TriQuint GaAs 1A/1D Design Manual</td>
<td>TriQuint Semiconductor</td>
<td>Ver. 2.0, Rev. A, January 1987, pp. 14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No.</td>
<td>Authors</td>
<td>Title</td>
<td>Journal/Conference Details</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----</td>
<td>---------</td>
<td>-------</td>
<td>---------------------------</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>43.</td>
<td>J. Sone, Y. Takayama</td>
<td>Analysis of Field Distributions in a GaAs MESFET at Large Drain Voltages</td>
<td>Electronics Letters, vol. 12, no. 23, 1976, pp. 622 - 624</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
49. C.T.M. Chang, T. Vrotsos, M.T. Frizell, R. Carroll
   A Subthreshold Current Model for GaAs MESFET’s
   IEEE Electron Device Letters
   vol. 8, no. 2, 1987, pp. 69 - 72

50. R.F. Vogel
   Analytical MOSFET Model with Easily Extracted Parameters
   IEEE Trans. on Computer-Aided Design
   vol. 4, no. 2, 1985, pp. 127 - 134

51. S.M. Sze
   Physics of Semiconductor Devices
   John Wiley & Sons, 1981
   chapter 5, pp. 262

52. D.B. Estreich
   A Simulation Model for Schottky Diodes in GaAs Integrated Circuits
   IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems
   vol. 2, no. 2, 1983, pp. 106 - 111

53. D.A. Divekar
   Comments on "GaAs FET Device and Circuit Simulation in SPICE"
   IEEE Trans. on Electron Devices
   vol. 34, no. 12, 1987, pp. 2564 - 2565

54. I.W. Smith, H. Statz, H.A. Haus, R.A. Pucel
   On Charge Nonconservation in FET’s
   IEEE Trans. on Electron Devices
   vol. 34, no. 12, 1987, pp. 2565 - 2568

55. H. Fukui
   Determination of the Basic Device Parameters of a GaAs MESFET
   The Bell System Technical Journal
   vol. 58, no. 3, 1979, pp. 771 - 797

56. P. Urien, D. Delagebeaudeuf
   New Method for Determining the Series Resistances in a MESFET or TEGFET
   Electronics Letters
   vol. 19, no. 17, 1983, pp. 702 - 703

   Source, Drain, and Gate Series Resistances and Electron Saturation Velocity in Ion-Implanted GaAs FET’s
   IEEE Trans. on Electron Devices
   vol. 32, no. 5, 1985, pp. 987 - 992
58. L. Yang, S.I. Long
   New Method to Measure the Source and Drain
   Resistances of the GaAs MESFET
   IEEE Electron Device Letters
   vol. 7, no. 2, 1986, pp. 75 - 77

59. R.P. Holmstrom, W.L. Bloss, J.Y. Chi
   A Gate Probe Method of Determining Parasitic
   Resistances in MESFET’s
   IEEE Electron Device Letters
   vol. 7, no. 7, 1986, pp. 410 - 412

60. M.J. Box
   A Comparison of Several Current Optimization
   Methods, and the Use of Transformations
   in Constrained Problems
   The Computer Journal
   vol. 9, no. 1, 1966, pp. 67 - 77

61. K. Doganis, D.L. Scharfetter
   General Optimization and Extraction of IC Device
   Model Parameters
   IEEE Trans. on Electron Devices
   vol. 30, no. 9, 1983, pp. 1219 - 1228

62. J.A. Nelder, R. Mead
   A Simplex Method for Function Minimization
   The Computer Journal
   vol. 7, 1965, pp. 308 - 313

63. J. Salonen
   The Extraction of Transistor Model Parameters
   Using Nonlinear Optimization Techniques
   Licentiate’s Thesis, Electron Physics Laboratory,
   Department of Electrical Engineering
   Helsinki University of Technology
   Otaniemi, Finland, 1987, 66 pages

64. PSpice User’s Manual
   MicroSim Corporation, 1989
   version 4.03, January 1990, pp. 82 - 86
SPICE input file for the circuit simulation described in chapter 11.2:

GaAs ED-DCFL 2-Divider 23.01.91

* .OPTIONS LIMPTS=10000 ITI1=100 ITL2=100 ITL4=100 ITL5=0
+ NOMOD NOPAGE NOECHO
*
* Voltages:
VDD      1  0  PWL(0.0 0.0 1.0N 2.0 100N 2.0)
VCLK     2  0  SIN(0.45 0.68 101.0E+6)
VRESET   5  0  0.0
*
* Circuit description:
* Node 2 = CLK
*      5 = RESET
*      6 = Q
*      7 = NQ
* 3 - input NOR
X1    1  8  8  DFET111
X2    8  6  0  EFET129
X3    8  9  0  EFET129
X4    8  5  0  EFET129
* 3 - input NOR
X5    1  9  9  DFET111
X6    9  2  0  EFET129
X7    9  8  0  EFET129
X8    9 10  0  EFET129
* 2 - input NOR
X9    1 10 10  DFET111
X10   10  2  0  EFET129
X11   10 11  0  EFET129
X12   10  9  0  EFET129
* 2 - input NOR
X13   1 11 11  DFET111
X14   11  7  0  EFET129
X15   11 10  0  EFET129
* 3 - input NOR
X16   1  6  6  DFET111
X17   6  5  0  EFET129
X18   6  9  0  EFET129
X19   6  7  0  EFET129
* 2 - input NOR
X20   1  7  7  DFET111
X21   7 10  0  EFET129
X22   7  6  0  EFET129
* Parasitic interconnection capacitances
C1       2  0  7.0F
C4       5  0 38.0F
C5       6  0 30.0F
C6       7  0 30.0F
C7       8  0 15.0F
C8       9  0 35.0F
C9      10  0 35.0F
C10     11  0 18.0F
* Oscilloscope loading = 10 kohm, 6 pF
CL       6  0 6P
* Transient analysis:
.TRAN 0.25N 60.0N 0.0N 0.25N
* .PROBE V(2) V(6)
* 1 x 11 um, 1-fingered DMESFET (standard model):
.SUBCKT DFET111 1 2 3
RD  1 11 124.909
J1  11 22 33 FET 11.0
RS  3 33 124.909
E1  22 33 2 33 0.5
CDS 11 33 1.4E-15
DGD 2 11 DD 4.32
DGS 2 33 DD 7.68
.MODEL DD D (IS=2.63E-15 N=1.13 CJO=2.2E-15 VJ=0.4 M=0.5 FC=0.0)
.MODEL FET NJF (LAMBDA=0.3 VTO=-0.3334 BETA=3.75E-4 IS=1.0E-30)
.ENDS DFET111
* 1 x 29 um, 1-fingered EMESFET (standard model):
.SUBCKT EFET129 1 2 3
RD  1 11 54.621
J1  11 22 33 FET 29.0
RS  3 33 54.621
E1  22 33 2 33 0.6
CDS 11 33 3.2E-15
DGD 2 11 DE 14.28
DGS 2 33 DE 15.72
.MODEL DE D (IS=1.88E-15 N=1.13 CJO=0.68E-15 VJ=0.33 M=0.5 FC=0.0)
.MODEL FET NJF (LAMBDA=0.8 VTO=0.0533 BETA=3.32E-4 IS=1.0E-30)
.ENDS EFET129
* 1 x 11 um, 1-fingered DMESFET (JFET model):
.SUBCKT DFET211 1 2 3
RD  1 11 124.909
B1  11 2 33 FET 11.0
RS  3 33 124.909
DGD 2 11 DD 4.32
DGS 2 33 DD 7.68
.MODEL DD D (IS=2.63E-15 N=1.13 CJO=2.2E-15 VJ=0.4 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=1 EVGS=0.5 LAMBDA=0.3 VTO=-0.3334 + BETA=3.75E-4 CDS=1.273E-16 IS=1.0E-30)
.ENDS DFET211
* 1 x 29 um, 1-fingered EMESFET (JFET model):
.SUBCKT EFET229 1 2 3
RD  1 11 54.621
B1  11 2 33 FET 29.0
RS  3 33 54.621
DGD 2 11 DE 14.28
DGS 2 33 DE 15.72
.MODEL DE D (IS=1.88E-15 N=1.13 CJO=0.68E-15 VJ=0.33 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=1 EVGS=0.6 LAMBDA=0.8 VTO=0.0533 + BETA=3.32E-4 CDS=1.1E-16 IS=1.0E-30)
.ENDS EFET229
*
* 1 x 11 um, 1-fingered DMESFET (tanh model):

```
.SUBCKT DFET311 1 2 3
RD  1 11  124.909
B1  11  2 33 FET 1.0
RS  3 33  124.909
DGD 2 11 DD 4.32
DGS 2 33 DD 7.68
.MODEL DD D (IS=2.63E-15 N=1.13 CJO=2.2E-15 VJ=0.4 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=2 ALPHA=6.0 LAMBDA=0.3 VTO=-0.6667 +
  BETA=1.0314E-3 CDS=1.273E-16 IS=1.0E-30)
* Subthreshold model 1:
  .MODEL FET GASFET (LEVEL=2 ALPHA=6.0 LAMBDA=0.3 VTO=-0.6667
  +
  BETA=1.0314E-3 SUBOP=1 ETA=13.12 GDLEAK=1.254E-10 +
  CDS=1.273E-16 IS=1.0E-30)
* Subthreshold model 2:
  .MODEL FET GASFET (LEVEL=2 ALPHA=6.0 LAMBDA=0.3 VTO=-0.6667
  +
  BETA=1.0314E-3 SUBOP=2 ETA=0.081 GDLEAK=1.254E-10 +
  VSUB=0.16887 VINCR=0.097 CDS=1.273E-16 IS=1.0E-30)
.ENDS DFET311
* 1 x 29 um, 1-fingered EMESFET (tanh model):

```}

```
.SUBCKT EFET329 1 2 3
RD  1 11  54.621
B1  11  2 33 FET 1.0
RS  3 33  54.621
DGD 2 11 DE 14.28
DGS 2 33 DE 15.72
.MODEL DE D (IS=1.88E-15 N=1.13 CJO=0.68E-15 VJ=0.33 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=2 ALPHA=6.0 LAMBDA=0.6 VTO=0.08887 +
  BETA=3.989E-3 CDS=1.1E-16 IS=1.0E-30)
* Subthreshold model 1:
  .MODEL FET GASFET (LEVEL=2 ALPHA=6.0 LAMBDA=0.6 VTO=0.08887
  +
  BETA=3.989E-3 SUBOP=1 ETA=13.12 GDLEAK=3.306E-10 +
  CDS=1.1E-16 IS=1.0E-30)
* Subthreshold model 2:
  .MODEL FET GASFET (LEVEL=2 ALPHA=6.0 LAMBDA=0.6 VTO=0.08887
  +
  BETA=3.989E-3 SUBOP=2 ETA=0.081 GDLEAK=3.306E-10 +
  VSUB=0.16887 VINCR=0.097 CDS=1.1E-16 IS=1.0E-30)
.ENDS EFET329
* 1 x 11 um, 1-fingered DMESFET (Statz model):

```}

```
.SUBCKT DFET411 1 2 3
RD  1 11  124.909
B1  11  2 33 FET 1.0
RS  3 33  124.909
DGD 2 11 DD 4.32
DGS 2 33 DD 7.68
.MODEL DD D (IS=2.63E-15 N=1.13 CJO=2.2E-15 VJ=0.4 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=3 ALPHA=5.85 LAMBDA=0.291 VTO=-0.6594 +
  BETA=1.106E-3 B=0.062 CDS=1.273E-16 IS=1.0E-30)
.ENDS DFET411
* 1 x 29 um, 1-fingered EMESFET (Statz model):

```}

``` SUBCKT EFET429 1 2 3
RD  1 11  54.621
B1  11  2 33 FET 1.0
RS  3 33  54.621
```
DGD  2 11  DE  14.28
DGS  2 33  DE  15.72
.MODEL DE D (IS=1.88E-15 N=1.13 CJO=0.68E-15 VJ=0.33 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=3 ALPHA=5.665 LAMBDA=0.6 VTO=0.08908
+ BETA=4.134E-3 B=0.1432 CDS=1.1E-16 IS=1.0E-30)
.ENDS EFET429

* Cubic model not used
*
* 1 x 11 um, 1-fingered DMESFET (new VTT model):
.SUBCKT DFET611 1 2 3
RD  1 11  124.909
B1  11  2 33 FET 11.0
RS  3 33  124.909
DGD  2 11  DD  4.32
DGS  2 33  DD  7.68
.MODEL DD D (IS=2.63E-15 N=1.13 CJO=2.2E-15 VJ=0.4 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=5 LG=1.0E-6 CH=1.382E-7 ND=1.04E23 U0=0.33567
+ ES=3.94E5 VBI=0.8 LAMBDA=0.188 CDS=1.1E-16 IS=1.0E-30)
.ENDS DFET611

* 1 x 29 um, 1-fingered EMESFET (new VTT model):
.SUBCKT EFET629 1 2 3
RD  1 11  54.621
B1  11  2 33 FET 29.0
RS  3 33  54.621
DGD  2 11  DE 14.28
DGS  2 33  DE 15.72
.MODEL DE D (IS=1.88E-15 N=1.13 CJO=0.68E-15 VJ=0.33 M=0.5 FC=0.0)
.MODEL FET GASFET (LEVEL=5 LG=1.0E-6 CH=1.0923E-7 ND=7.37E22 U0=0.428
+ ES=4.61E5 VBI=0.8 LAMBDA=0.583 CDS=1.1E-16 IS=1.0E-30)
.ENDS EFET629

.*
.END