Modeling, Control, and Design of Input-Series–Output-Parallel-Connected Converter for High-Speed-Train Power System

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Abstract—In this paper, a charge control with an input voltage feedforward is proposed for an input-series–output-parallel-connected converter configuration for the high-speed-train power system application. This control scheme accomplishes the output current sharing for the output-parallel-connected modules as well as the input voltage sharing for the input-series-connected modules for all operating conditions including the transients. It also offers the robustness for the input voltage sharing control according to the component value mismatches among the modules. This configuration enables the usage of a MOSFET for a high-voltage system allowing a higher switching frequency for a lighter system weight and smaller size. The performance of the proposed scheme is verified through the experimental results.

Index Terms—Charge control, input-series–output-parallel-connected converter.

I. INTRODUCTION

In the high-speed train power system, the input voltage of the auxiliary power supply is about 700 V. Therefore, an insulated gate bipolar transistor (IGBT) should be used instead of a MOSFET because of the high input voltage. Even though a soft-switching technique is employed for an IGBT, the switching frequency must be limited around 30 kHz for good efficiency because of the tail current. To increase the switching frequency for reduction of the system size while maintaining the efficiency requirement, a MOSFET should be considered for the switching device. However, due to the high input voltage, a MOSFET cannot be used in a conventional bridge topology unless the device is series connected to sustain the high voltage. Several papers in the literature address the issue of the device turn-off [1]–[4]. To achieve the voltage balancing a passive and active balancing method is used. The passive method requires a snubber circuit and this causes additional loss and restricts the switching frequency.

The active methods require complicated control circuits to achieve the voltage balancing, and the control delay of the voltage-balancing controller can increase the device stress, so that the switching speed is restricted. Moreover, perfect balancing is hard to accomplish during the switching transients.

The problems of the device series connection can be solved by the input-series–output-parallel (ISOP)-connected converter configuration [5]. Fig. 1 shows the ISOP zero-voltage switching (ZVS) full-bridge converter. In this configuration, the input voltage is divided by the series-connected input capacitors, and the outputs are paralleled. The series-connected converter experiences only the divided input voltage so that the lower voltage rating device MOSFET can be used for higher switching frequency operation.

In this paper, control of the ISOP-connected scheme is presented, in which lower voltage rating devices (MOSFETs) can be used for a high input voltage and the benefits of a parallel scheme can be achieved as well. In order to ensure the input voltage balancing and the output current sharing for all operation conditions including the transients, the charge control with the input voltage feedforward scheme is presented. A 5-kW piece of hardware employing an ISOP ZVS full-bridge scheme is built and the performance of the proposed control...
scheme is verified through the hardware experiments. Also, a comparison between the proposed scheme and the developed zero-voltage ZCS (ZVZCS) full-bridge converter system using IGBTs is given.

II. ISOP-CONNECTED CONVERTER CONFIGURATION
EMPLOYING CHARGE CONTROL WITH THE INPUT VOLTAGE FEEDFORWARD

A. ISOP System

1) One Voltage Controller Case: The components of the two converters in the ISOP converter system cannot be perfectly matched. If each converter has its own output voltage controller, output currents cannot be equally distributed because of the components mismatches. If one voltage controller controls the two converters, transformer turns ratio mismatch can cause output current and input capacitor voltage imbalances. Fig. 2 shows the simulation circuit to check this phenomenon and Fig. 3 shows the simulation result. There is a 10% mismatch in the transformer turns ratio. The duty ratios of the two modules are the same but the output currents become unbalanced due to the transformer mismatch and this causes input currents imbalance and input capacitor voltage imbalance. This results in power imbalance between modules and makes the system unreliable. One module, which supplies more power than the other, suffers more stress so the probability of failure is increased.

2) Charge Control Case: If the output currents are controlled to be balanced to solve the problems mentioned above, then even a slight mismatch in the transformer can cause the
Fig. 6. Input-capacitor mismatch case simulation result.

Fig. 7. ISOP ZVS full-bridge converter with the proposed method.

Fig. 8. Balancing mechanism of the proposed method.

Fig. 9. Simulation result with the proposed method.

input current imbalance. The input capacitor voltage of one module which draws more current than the other becomes higher and that of the other module becomes lower. Therefore, the average input current must be controlled instead of the output current.

To control the average input current, charge control can be implemented. However, if the component mismatches in the switch current-sensing circuit and the charge capacitor $C_T$, the average input current can be mismatched, which eventually causes the input voltage imbalance and the input voltage of one module to exceed the device rating. Fig. 4 shows the simulation circuit to check this phenomenon and Fig. 5 shows the simulation result. The inductor currents and the input capacitor voltages are shown in the case of a 10% mismatch in the charge capacitor.

Also, the input capacitor mismatch can cause the input capacitor voltage imbalance even if the components in the switch current sensing circuit and the charge capacitor are perfectly balanced. Fig. 6 shows the simulation result when there is a 10% mismatch in the input capacitor. Input capacitor voltages are unbalanced because of the unbalanced input capacitor voltages.

B. Charge Control with the Input Voltage Feedforward

To solve the problems mentioned above, charge control with the input voltage feedforward is proposed. Fig. 7 shows the ISOP ZVS full-bridge converter employing charge control with the input voltage feedforward. In this scheme, the input current of each module is adjusted according to the input voltage difference to achieve the voltage balance between the modules for all operating conditions. The input voltage difference is then multiplied by a gain $k_C$ and this controls the offset voltage in the duty ratio modulator. Fig. 8 illustrates the balancing mechanism of the proposed method.
when the input voltage of module #1, \( V_{\text{cin}1} \), is higher than that of module #2, \( V_{\text{cin}2} \). Because of the lowered offset voltage, \(-k(V_{\text{cin}1} - V_{\text{cin}2})\), the input current of module #1 increases and this increased input current makes the input capacitor voltage decrease. On the other hand, the input current of module #2 decreases owing to the raised offset voltage, \(+k(V_{\text{cin}1} - V_{\text{cin}2})\), and this reduced input current makes the input capacitor voltage increase because the supply current from the source for the two modules are equal. In this way, \( V_{\text{cin}1} \) and \( V_{\text{cin}2} \) become equal and the power balance of two modules is accomplished.

Equation (1) is obtained in Fig. 8 and the amount of the difference in the average input current to balance the input voltage during the transient can be calculated by (2) under an assumption of \( DT_S \gg \Delta t_{\text{cen}} \)

\[
\frac{1}{C_T} \int_0^{DT_S} n_c i_{\text{in}} \, dt + \frac{k}{C_T} \Delta V_{\text{in}} = -\frac{1}{C_T} \int_0^{DT_S + \Delta t_{\text{cen}}} n_c (i_{\text{in}} + \Delta i_{\text{in}}) \, dt
\]

\[\Delta I_{\text{in max}} = \frac{k}{n_c} \cdot C_T \frac{\Delta V_{\text{in max}}}{DT_S} \]  

where \( \Delta V_{\text{in max}} \) is the maximum of the input capacitor voltage difference, \( C_T \) is the charge control capacitor, \( D \) is the duty ratio, \( T_S \) is the switching period, \( n_c \) is the turns ratio of the current transformer, and \( k \) is the gain of the differential amplifier of the input voltages. The higher the gain \( k \), the larger the \( \Delta I_{\text{in max}} \) is, and lower the gain \( k \) makes \( \Delta I_{\text{in max}} \) small but it takes a longer time to reach the balanced steady state of the input capacitor voltages. Therefore, there must be a design tradeoff for the gain \( k \) between the current rating of the converter and the settling time.

Fig. 9 shows the simulation result of the proposed scheme. There is a 10% mismatch in the charge capacitor and in the input capacitor. The initial input voltage is 540 V and steps up to 600 V at 10 ms. As shown in this figure, to achieve the balance of the input capacitor voltage the input average currents are controlled to be different at the transient. Through the proposed scheme, input voltage sharing and input currents balancing are accomplished in spite of the component mismatch.

**III. SMALL-SIGNAL ANALYSIS**

Fig. 10 shows the small-signal equivalent circuit of a two-module ISOP ZVS full-bridge converter system [6]. In this figure, all switches are replaced with its small-signal pulsedwidth modulation (PWM) model [7], [8]. The ISOP system uses the input capacitor voltage as the control information for input capacitor voltage balancing. The input capacitor voltages adds new states to the system model and the overall small-signal model can be completed adding these two input capacitor voltage feedback loops to the general two-loop-controlled parallel converter system. The overall small-signal block diagram of the ISOP system including this control loop is shown in
In Fig. 11, $R_i$ and $FM$ are the equivalent current gain and the modulator gain, respectively. $H_c(s)$ represents the sampled-and-hold effect in the current loop [9] and $k$ represents the sensing gain of the input voltage difference. In order to obtain design information of the control loop for stability, it is necessary to simplify the system model in Fig. 11. Since the system has additional input voltage feedback loops to the conventional current-mode-controlled parallel module system, the influence of the feedback loop is analyzed.

Fig. 12 shows the transfer function from the control voltage $v_c$ to the output voltage $v_o$ (point A) in Fig. 11 with and without the input capacitor voltage loop. As can be seen from this figure, the two plots are almost the same. This can be qualitatively interpreted as follows. Since the amount of the input voltage feedback for each module is the same but with opposite sign, there is a net canceling effect in the overall system. Thus, we can conclude that the input capacitor voltage feedback loop has little
Fig. 13. Current loop gain according to the variation of gain $k$.

Fig. 14. Circuit diagram of the equivalent single module.

Fig. 15. System block diagram of the equivalent single module.

Fig. 16. Small-signal model of the equivalent single module.

IV. ISOP SYSTEM DESIGN

A. Design of Input Voltage Feedforward Gain $k$

The higher the gain $k$, the larger the $\Delta I_{\text{in max}}$ is, and decreasing the gain $k$ makes $\Delta I_{\text{in max}}$ small but it takes a longer time to reach the balanced steady state of the input capacitor voltages. Therefore, there must be a design tradeoff for the gain $k$ between the current rating of the converter and the settling time. The input current difference according to the $k$ is determined by (1).

B. Design of Charge Control Parameter

The charge control capacitor $C_T$ and external ramp slope $S_e$ shown in Fig. 7, can be determined by [9]. External ramp is necessary to prevent subharmonic oscillation.

C. Design of Input Filter

Using the small-signal model of the equivalent single module in Fig. 16, the input filter can be designed with the conventional method [10] and the designed parameters can be converted into the parameters of the two-module system. In this paper, a simple LC filter and an RL damping branch are used, as shown in Fig. 2.
D. Design of Voltage Loop Compensator

If $C_T$ is designed, the current loop gain $T_i$ is determined by

$$T_i = FM \cdot Rf \cdot Hc(s) \cdot G_{di}. \quad (4)$$

Once the current loop is designed, the current loop closed power stage can be treated as a new power stage for the voltage loop design. The system loop gain defined at point A in Fig. 15 is

$$T_A = G_{ci} \cdot H_v = \frac{FM \cdot G_{do}}{1 + FM \cdot \frac{Rf}{2} \cdot Hc(s) \cdot G_{di}} \cdot H_v. \quad (5)$$

$G_{ci}$ is the transfer function from the control voltage $v_{ci}$ to the output voltage $v_o$ with the current loop closed for given operating conditions. Fig. 12 shows a Bode plot of $G_{Ci}$, from which the voltage loop compensator $H_v$ can be designed.

For $H_v$, an integrator plus one pole and one zero compensator is used

$$H_v(s) = \frac{K_i}{s} \frac{1 + s/\omega_{z1}}{1 + s/\omega_{p1}}. \quad (6)$$

Fig. 17 shows the designed loop gain $T_A$ which has a wide control bandwidth with plenty of phase margin.

V. EXPERIMENTAL RESULT

To verify the effectiveness of the proposed control scheme, a 5-kW piece of hardware consisting of two 2.5-kW ZVS full-bridge converters shown in Fig. 1 is built, and its component values are summarized in Table I. Table I also includes the design results of a previously developed piece of hardware of the ZVZCS full-bridge scheme using an IGBT [11]. The switching frequencies of the two converters are selected to meet the efficiency specification at full load, 95%. Table I compares the two converters with respect to volume and weight, which shows that approximately 30% of weight and volume are reduced. Heat-sink size is reduced by parallel operation and the size of magnetic components is reduced by increased switching frequency [12]. Fig. 18 shows the measured efficiency of the two converters.

The experimental setup is the same as that of the previous simulations with the proposed method. Fig. 19 shows the transformer primary currents employing the proposed control scheme. The input voltage steps up at 5 ms from 540 to 600 V. The input capacitor of module #2 is 10% greater than that of module #1. Because the input capacitor of module #1 is smaller, the input capacitor voltage of module #1 varies faster than that of module #2. To balance the input capacitor voltage, the proposed charge controller increases the input current of module #1 and decreases the input current of module #2. The current waveforms in Fig. 19 verify the canceling effect for the output voltage control loop as discussed in Section III. There is about a 5-A difference between the input currents of the two modules to balance the input capacitor voltages. The experimental result coincides with the simulation result in Fig. 9.

Fig. 20 shows the input capacitor voltages of the two modules. In both the steady and transient states, a perfect balance of the input capacitor voltages is achieved by the proposed control scheme. Therefore, the power balance between the two modules

\begin{table}[h]
\centering
\caption{Comparison of ZVZSC full-bridge converter (IGBT) and ISOP ZVS full-bridge converter (MOSFET)}
\begin{tabular}{|c|c|c|}
\hline
 & ZVZCS full bridge converter & ISOP ZVS full bridge converter \\
\hline
Output power & 5kW & 2.5kW, 2EA \\
\hline
Switching frequency & 33.3kHz & 100kHz \\
\hline
Heat sink & 2920cm³ & 2040cm³ \\
\hline
Transformer & TDK EC90 & TDK PQ50/50, 2EA \\
\hline
Output inductor & TDK EC90 & TDK EI60, 2EA \\
\hline
Output capacitor & 1000uF & 1000uF \\
\hline
Switching device & IRGPH50KD2 & IRPC60 \\
\hline
Rectifier & RURU8060 & RURF3060 \\
\hline
Total system volume & 3742cm³ & 2554.7cm³(68.3%) \\
\hline
Total weight & 12kg & 8.1kg(67.5%) \\
\hline
\end{tabular}
\end{table}
is accomplished by the proposed control scheme and the voltage stress is equally divided between the two modules.

Fig. 21 shows the transformer primary currents employing the proposed method when load current steps down from full load to half load at 10 ms. The two currents are balanced due to the effect of charge control.

VI. CONCLUSION

In this paper, the charge control with the input voltage feed-forward has been proposed for the ISOP-connected converter configuration for high-voltage power conversion applications. This control scheme accomplishes the output current sharing for the output-parallel-connected modules as well as the input voltage sharing for the input-series-connected modules for all operating conditions including the transients. It also offers robustness for the component value mismatches among the modules.

The small-signal analysis shows that an equivalent single-module system can be used in the control loop design process in spite of input capacitor voltage feedback loop. The performance of the proposed scheme has been verified by the experimental results.

REFERENCES


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