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An organic-inorganic hybrid solar cell with a *p-i-n* stack structure has been investigated. The *p*-layer was a spin coated film of PEDOT:PSS [poly(3,4-ethylenedioxythiophene) poly (styrenesulfonate)]. The *i*-layer was hydrogenated amorphous silicon (*a*-Si:H), and the *n*-layer was microcrystalline silicon (μc-Si). The inorganic layers were deposited on top of the organic layer by the hot-wire chemical vapor deposition technique at 200 °C. These hybrid devices exhibited open circuit voltages (V_{OC}) as large as 0.88 V and solar conversion efficiencies as large as 2.1%. Comparison of these devices with those incorporating *a*-SiC:H:B *p*-layers indicates that the organic layer is acting as an electrically ideal *p*-layer. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2136409]

Organic materials have gained importance over the past several years for their potential in electronic devices such as organic light emitting diodes (OLEDs), solar cells, photodetectors, and thin film transistors. Among the most attractive characteristics of organics are the tailorability of their energy levels and the relatively simple, low-temperature processing techniques for device construction. Hydrogenated amorphous silicon (*a*-Si:H) is another material suitable for low-cost, large-area fabrication of potentially flexible devices. The combination of these two materials is very attractive for organic and inorganic hybrid device applications.

The solar cell structure that we investigated consists of a *p-i-n* stack that is also commonly used in conventional inorganic solar cells; in the present work, an organic film has replaced the typical *p*-type inorganic *a*-SiC:H:B layer used for *a*-Si:H based "superstrate" solar cells. The aim is to develop an efficient solar cell, fabricated at a low process temperature, which takes advantage of the photogeneration and charge transport properties of *a*-Si:H as well as the solution processing and potentially tunable energy levels of PEDOT:PSS [poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)]. Previously, Garnier has shown improved device performance (increased open circuit voltage and efficiency) for an *n*-type GaAs–Au Schottky diode upon insertion of a thiophene derivative film between the GaAs and the gold.[1] Organic-inorganic junctions have generated a great deal of interest for their potential in developing hybrid devices[2–9] and as a means to understand organic semiconductors and their interfacial properties.[10–13]

In the literature, it is most common to fabricate a device in which the organic layer has been thermally deposited onto an inorganic semiconductor substrate,[4,6] although there are some reports of electrodeposition of thiophene derivatives onto an inorganic substrate,[2,3] and even of spin coating organic solutions onto inorganic substrates.[8,9,13] However, solvent effects resulting from such procedures can have a dramatic effect on the interfacial characteristics. For this reason, it is beneficial to employ low temperature techniques, such as hot wire chemical vapor deposition (HWCVD)[7] or plasma-enhanced (PE) CVD[5] to allow for the growth of an inorganic layer onto an underlying polymer film.

The solar cells were fabricated according to the following procedure. The PEDOT:PSS suspension (Bayer, Inc. "Baytron P LS") was modified, to increase its conductivity, by mixing with glycerin, N-methylpyrrolidone, and isopropanol.[14] The modified PEDOT:PSS was spin cast at 800 rpm onto a 25 mm × 25 mm indium-tin-oxide (ITO) coated glass substrate (Applied Films, Inc., 15 Ω/sq). This process yielded a film approximately 110 nm thick with a sheet resistance of 2.5 kΩ/sq. The PEDOT:PSS coated ITO films were loaded into a HWCVD chamber[15] and heated to 200 °C before the thin film Si deposition. Pure silane (SiH_4) with a flow rate of 20 sccm and 10 mTorr was used for the *a*-Si:H layer deposition. A thin, microcrystalline Si (μc-Si) film was then deposited [SiH_4 (3 sccm), H_2 (40 sccm), 25 mTorr], and the *n*-layer was grown immediately after the μc-Si buffer layer using a mixture of SiH_4 (3 sccm), H_2 (40 sccm), and 3% PH_3 in H_2 (2.5 sccm) at 23 mTorr. The sample was cooled and transported to a metal deposition system where 0.05 cm^2, 800 Å thick Pd top contacts were grown by thermal evaporation. Each dot was isolated by removing the surrounding conducting μc-Si *n*-layer via reactive ion etching by SF_6. Figure 1 shows the device structure.

The solar cell characteristics were measured using a tungsten-halogen lamp with illumination adjusted to one-sun intensity (100 mW/cm^2); slight deviations between the spectrum of the tungsten-halogen lamp and the AM1.5 standard spectrum were not accounted for in this work. Figure 2 shows the current density as a function of voltage (*J-V*) of

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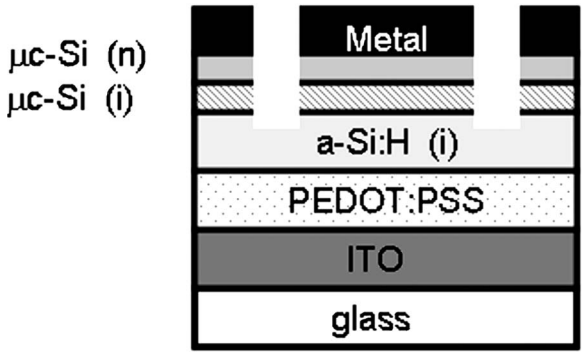

FIG. 1. Device structure (not to scale) of hybrid cell with a post-fabrication isolation etch. Devices without etch show a large leakage current in reverse bias.

the best hybrid solar cell. This cell has an efficiency of 2.1% with an open circuit voltage (V_{OC}) of 0.883 V, fill factor (FF) of 0.51, and short circuit current density (J_{SC}) of 4.55 mA/cm^2. 0.883 V is the highest reported V_{OC} for this type of *p-i-n*, thin film, organic-inorganic hybrid solar cell. The intersection of dark and light *J-V* curves in the forward bias can be attributed to the imperfect interface between the PEDOT:PSS and *i*-layers. For reference, one device was fabricated in which an *i-n* stack was grown directly on the ITO, without a PEDOT:PSS layer. This reference device displayed very poor solar cell characteristics: A V_{OC} of only 0.176 V, an efficiency of 0.21%, and a J_{SC} of 3 mA/cm^2. The high V_{OC} upon incorporation of PEDOT:PSS suggests that the conducting polymer is a potential replacement for traditional, inorganic, *a*-Si:H *p*-layers.

We examined the effects of varying (i) the substrate temperature during *a*-Si:H deposition, and (ii) the thicknesses of the PEDOT:PSS film, the *a*-Si:H *i*-layer, the μc-Si buffer layer, and the μc-Si *n*-layer. The substrate temperature was varied from 140 °C to 220 °C, and it was determined that devices performed better with increasing temperature since the quality of *a*-Si:H improves with temperature. However, devices fabricated with substrate temperatures above 200 °C showed reduced performance; presumably this effect was caused by damage to the PEDOT:PSS. A study on the thickness of the PEDOT:PSS layer revealed a trend with short circuit current: either too thin or too thick a layer led to a reduction in current density under illumination; the optimal thickness of 110 nm was used for all subsequent devices.

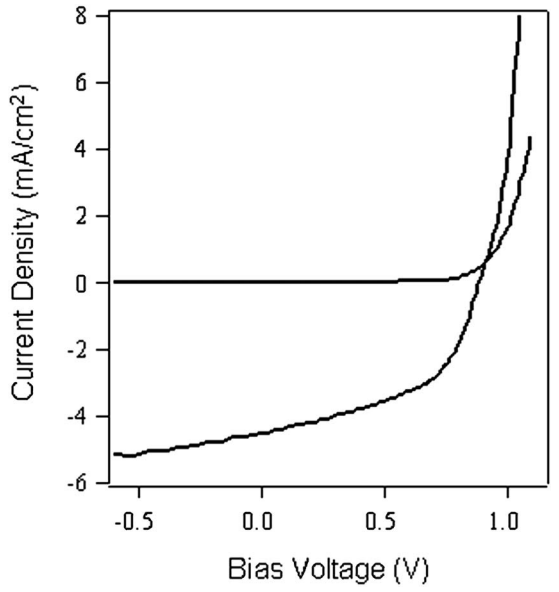

FIG. 2. Dark and illuminated (AM1.5) $J-V$ curves for solar cell structure of glass/ITO/PEDOT:PSS (110 nm)/*a*-Si:H (i) (130 nm)/μc-Si(*i*) (40 nm)/μc-Si(*n*) (20 nm)/Pd.

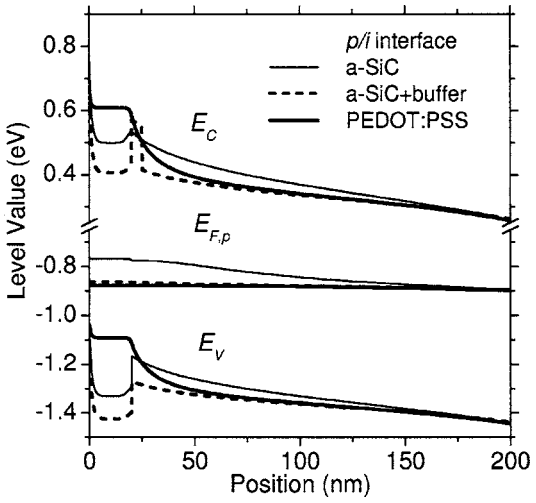

FIG. 3. The calculated profiles for the bandedge levels (valence E_V and conduction E_C) and for the hole quasi-Fermi level ($E_{F,p}$) for three different p/i interface configurations (open-circuit, AM1.5 illumination) of amorphous silicon based *pin* solar cells. Note: the p/i interface is located at $x=20$ nm, the full PEDOT:PSS film thickness not being shown.

In a previous effort to create a hybrid device using PEDOT:PSS and *a*-Si:H, in which the organic, aqueous suspension was painted onto an *a*-Si:H n/i structure, the solar cells displayed a V_{OC} of 0.72 V but very little photocurrent ($\sim$0.15 mA/cm^2).[8] In this case, it was suspected that the water in the suspension caused an insulating oxide layer to grow at the interface. In the current work, solar cells were fabricated using thin film Si deposition on top of spin coated PEDOT:PSS, to improve the interface at the junction and create a better device.

It is useful to compare our results using PEDOT:PSS with the characteristics of cells fabricated following the same procedures, but substituting *a*-SiC:H based *p*-layers for the organic layer. For an *a*-SiC:H *p*-layer (from SiH_4, H_2, and trimethylboron) the open-circuit voltage was 0.76 V. The insertion of a 5 nm wide-gap *a*-Si:H buffer layer (from SiH_4 and H_2) between the *a*-SiC:H:B *p*-layer and the *i*-layer increased this value to 0.88 V, essentially the same as that we achieved with PEDOT:PSS (without a buffer layer). We believe that this value $V_{OC}=0.88$ V is essentially the "intrinsic" value associated with our *a*-Si:H *i*-layers, and thus that the PEDOT:PSS is acting as a nearly ideal *p*-layer.

In Fig. 3 we present device simulations that illustrate and support this view. The figure shows calculated profiles for the two bandedges (valence, E_V, and conduction, E_C) and for the hole quasi-Fermi level ($E_{F,p}$) for three different p/i interface configurations; these are open-circuit simulations for AM1.5 illumination. Modeling was done using the computer program, AMPS;[16] the intrinsic-layer parameters for *a*-Si:H are those of Ref. 17, excepting the bandgap (1.70 eV) and the valence bandtail width (50 meV); we changed these parameters to accommodate the differences between the present HWCVD *a*-Si:H and typical PECVD *a*-Si:H.

The thin solid lines of the figure correspond to a calculation for an *a*-SiC:H:B *p*-layer. As can be read from the figure, for the *a*-SiC:H:B we used $E_G=1.85$ eV, a valence band offset of 0.15 eV, and a Fermi-level 0.57 eV above the bandedge. We used the same *n*-layer parameters for all three *p*/*i* configurations. For the *a*-SiC:H:B calculation, the Fermi level position in the *n*-layer (not shown) corresponds to a built-in potential $V_{BI}=1.05$ V.

In the figure, the open-circuit voltage V_{OC} may be read from the hole quasi-Fermi level $E_{F,p}$; in particular, $E_{F,p}$ at $x=0$ corresponds to the product eV_{OC} (e is the electron charge). By convention, the electron quasi-Fermi level at the right contact is set to $E_{F,n}=0.0$ eV. As can be seen, the simulation reproduces the experimental value $V_{OC}=0.76$ V. For this *a*-SiC:H:B *p*-layer calculation, the poor position of the Fermi level causes V_{OC} to be about 0.1 V below the intrinsic value. This decrement can be read from the figure as the rise in $E_{F,p}$ as the *p*/*i* interface is approached from the right.

It is worth noting that V_{OC} is significantly affected by the *p*-layer Fermi level even though V_{OC} is noticeably less (0.3 V) than V_{BI}. The failure of the "rule-of-thumb" that interface effects on V_{OC} are negligible for $V_{OC}<V_{BI}$ originates in the very low values ($\ll 1$ cm^2/V s) of the hole drift-mobility in *a*-Si:H.[18] On the other hand, calculations are relatively insensitive to the *n*-layer parameter choices; the insensitivity originates in the much larger values for electron drift-mobilities (≈ 1 cm^2/V s)

For the PEDOT:PSS calculation (bold, solid lines), $E_{F,p}$ is essentially flat near the *p*/*i* interface, and V_{OC} thus has its intrinsic value 0.88 V. For PEDOT:PSS we used $E_G=1.7$ eV, no band offsets with *a*-Si:H, and a Fermi level 0.2 eV above E_V; these are similar to PEDOT:PSS parameters proposed in recent work on PEDOT:PSS/crystalline silicon heterostructures,[9] and correspond to $V_{BI}=1.25$ V for this simulation.

Devices prepared with an *a*-SiC:H:B *p*-layer and a 5 nm buffer layer (*a*-Si:H made with strong H_2 dilution of SiH_4) also gave $V_{OC}=0.88$ V. In Fig. 3, we show this buffer layer as creating a barrier to thermionic emission[18] of electrons into the *a*-SiC:H:B *p*-layer, thus compensating for the poor location of E_F in *a*-SiC:H:B. As can be seen in the figure, such a barrier flattens the profile of $E_{F,p}$, and causes the device to yield essentially the intrinsic value for V_{OC}.

In summary, computer simulation was used to model this organic-inorganic hybrid interface, treating PEDOT:PSS as a semiconductor with *a*-Si:H properties modified such that the bandgap equals 1.7 eV. This modeling was done in attempt to explain the large V_{OC} displayed by the cell. It did not take into account interfacial considerations such as PSS anion coverage of the PEDOT:PSS surface, possible electrical passivation of the organic film due to electron transfer, nor does it attempt to explain the depletion width associated with this hybrid junction or the modest amount of photocurrent generated by the cell. Further work attempting to better understand and explain these interfacial dynamics and device parameters is under way.

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