Broadband Low-Noise CMOS Mixers for Wireless Communications

by

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Abstract

In this thesis, three broadband low-noise mixing circuits which use CMOS 130 nm technology are presented. As one of the first few stages in a receiving front-end, stringent requirements are posted on mixer performance. The Gilbert cell mixers have presented excellent properties and achieved wide applications. However, the noise of a conventional active Gilbert cell mixer is high. This thesis demonstrates both passive and active mixing circuits with improved noise performance while maintaining the advantages of the Gilbert cell-based mixing core. Furthermore, wide bandwidth and variable gain are implemented, making the designed mixers multi-functional, yet with compact sizes and low power consumptions.

The first circuit is a passive 2x subharmonic mixer that works from 4.5 GHz to 8.5 GHz. The subharmonic mixing core is a two-stage passive Gilbert cell driven by a quadrature LO signal. Together with a noise-cancelling transconductor and an inverter-based TIA, this subharmonic mixer possesses an excellent broadband conversion gain and a low noise figure. Measurement results show a high conversion gain of 16 dB and a low average DSB NF of 9 dB.

The second design is a broadband low-noise variable gain mixer which operates between 1 and 6 GHz. The transconductor stage is implemented with noise cancellation and current bleeding techniques. Series inductive peaking is used to extend the
bandwidth. Gain variation is achieved by a current-steering IF stage. Measurements show a wide gain control range of 13 dB and a low noise performance over the entire frequency and gain range. The lowest DSB NF is 3.8 dB and the highest DSB NF is 14.2 dB.

The Third design is a broadband low-noise mixer with linear-in-dB gain control scheme. Using the same transconductance stage with the second circuit, this design also works from 1 to 6 GHz. A 10 dB linear-in-dB gain control range is achieved using an R-r load network with a linear-in-dB error less than $\pm 0.5$ dB. Low noise performance is achieved. For different frequencies and conversion gains, the lowest DSB NF is 3.8 dB and the highest DSB NF is 12 dB.
Acknowledgments

First and foremost, I would like to thank Dr. Carlos Saavedra for his consistent guidance and support throughout my Master’s studies. He exposed me to the excitement of academic research and provided me with opportunities to sharpen my skills. I have been deeply impressed by his inspiring advice and timely feedback.

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# Nomenclature

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<th>Meaning</th>
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<tbody>
<tr>
<td>( A_v )</td>
<td>Voltage Gain [V/V]</td>
</tr>
<tr>
<td>( C_{gd} )</td>
<td>Gate to Drain Capacitance [F]</td>
</tr>
<tr>
<td>( C_{gs} )</td>
<td>Gate to Source capacitance [F]</td>
</tr>
<tr>
<td>( C_{ox} )</td>
<td>Gate Oxide Capacitance per Unit Area [F/mm(^2)]</td>
</tr>
<tr>
<td>( F )</td>
<td>Noise Factor</td>
</tr>
<tr>
<td>( f_c )</td>
<td>Flicker Noise Corner Frequency [Hz]</td>
</tr>
<tr>
<td>( f_{IF} )</td>
<td>Frequency of the IF Signal [Hz]</td>
</tr>
<tr>
<td>( f_{LO} )</td>
<td>Frequency of the LO Signal [Hz]</td>
</tr>
<tr>
<td>( f_{RF} )</td>
<td>Frequency of the RF Signal [Hz]</td>
</tr>
<tr>
<td>( g_m )</td>
<td>Transconductance [I/V]</td>
</tr>
<tr>
<td>( g_{mb} )</td>
<td>Back Gate Transconductance [I/V]</td>
</tr>
<tr>
<td>( i_{nd} )</td>
<td>Drain Current Noise Spectral Density [A/√Hz]</td>
</tr>
<tr>
<td>( k )</td>
<td>Boltzmann’s Constant [J/K]</td>
</tr>
<tr>
<td>( L )</td>
<td>Transistor Gate Length [µm]</td>
</tr>
<tr>
<td>( Q )</td>
<td>Quality Factor</td>
</tr>
<tr>
<td>( r_o )</td>
<td>Transistor Drain-Source Resistance at Saturation [Ω]</td>
</tr>
<tr>
<td>Symbol</td>
<td>Meaning</td>
</tr>
<tr>
<td>----------</td>
<td>----------------------------------------------</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>Input Reflection Coefficient [dB]</td>
</tr>
<tr>
<td>$S_{11}^{diff}$</td>
<td>Differential Input Reflection Coefficient [dB]</td>
</tr>
<tr>
<td>$T$</td>
<td>Absolute Temperature [K]</td>
</tr>
<tr>
<td>$V_{bd}$</td>
<td>Bleeding Circuit Bias Voltage [V]</td>
</tr>
<tr>
<td>$V_{ctrl}$</td>
<td>Control Voltage [V]</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>DC Supply Voltage [V]</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>DC Drain-Source Voltage [V]</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>DC Gate-Source Voltage [V]</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Transistor Threshold Voltage [V]</td>
</tr>
<tr>
<td>$W$</td>
<td>Transistor Width [$\mu$m]</td>
</tr>
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**Greek Symbols**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\gamma$</td>
<td>Transistor Noise Coefficient</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Angular Frequency [rad/s]</td>
</tr>
<tr>
<td>$\omega_{IF}$</td>
<td>Angular Frequency of the IF Signal [rad/s]</td>
</tr>
<tr>
<td>$\omega_{LO}$</td>
<td>Angular Frequency of the LO Signal [rad/s]</td>
</tr>
<tr>
<td>$\omega_{RF}$</td>
<td>Angular Frequency of the RF Signal [rad/s]</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Electron Mobility [cm$^2$/V·s]</td>
</tr>
</tbody>
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**Acronym**

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Meaning</th>
</tr>
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<tbody>
<tr>
<td>ACG</td>
<td>Automatic Gain Control</td>
</tr>
<tr>
<td>CG (CL)</td>
<td>Conversion Gain (Conversion Loss)</td>
</tr>
<tr>
<td>CG-CS</td>
<td>Common-gate Common-source</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
</tr>
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</table>

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<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>CPW</td>
<td>Coplanar Waveguide</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DSB</td>
<td>Double-Sideband</td>
</tr>
<tr>
<td>DUT</td>
<td>Device-under-test</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>GSGSG</td>
<td>Ground-Signal-Ground-Signal-Ground</td>
</tr>
<tr>
<td>HP</td>
<td>Hewlett-Packard company</td>
</tr>
<tr>
<td>IBM</td>
<td>International Business Machines Corporation</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuits</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IIP3</td>
<td>Input-referred Third-order Intercept Point</td>
</tr>
<tr>
<td>IM3</td>
<td>Third-order Intermodulation Products</td>
</tr>
<tr>
<td>IMD</td>
<td>Intermodulation Distortion</td>
</tr>
<tr>
<td>IP1dB</td>
<td>Input-referred 1 dB Interception Point</td>
</tr>
<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
</tr>
<tr>
<td>LNTA</td>
<td>Low Noise Transconductance Amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LTE</td>
<td>Long Term Evolution</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NMOS</td>
<td>n-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>NF(_{DSB})</td>
<td>Double-Sideband Noise Figure</td>
</tr>
<tr>
<td>NF(_{SSB})</td>
<td>Single-Sideband Noise Figure</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
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<tr>
<td>---------</td>
<td>------------</td>
</tr>
<tr>
<td>OIP3</td>
<td>Output-referred Third-Order Intercept Point</td>
</tr>
<tr>
<td>OP1dB</td>
<td>Output-referred 1 dB Intercept Point</td>
</tr>
<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
</tr>
<tr>
<td>P1dB</td>
<td>1 dB Compression Point</td>
</tr>
<tr>
<td>PMOS</td>
<td>p-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>PSA</td>
<td>Power Spectrum Analyzer</td>
</tr>
<tr>
<td>PSHM</td>
<td>Passive Subharmonic Mixer</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>S-E</td>
<td>Single-ended</td>
</tr>
<tr>
<td>SHM</td>
<td>Subharmonic Mixer</td>
</tr>
<tr>
<td>SMA</td>
<td>SubMiniature version A</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SSB</td>
<td>Single-Sideband</td>
</tr>
<tr>
<td>TIA</td>
<td>Transimpedance Amplifier</td>
</tr>
<tr>
<td>VCG</td>
<td>Variable Conversion Gain</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable Gain Amplifier</td>
</tr>
<tr>
<td>VGM</td>
<td>Variable Gain Mixer</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
</tr>
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Chapter 1

Introduction

1.1 General Introduction

Wireless communications have experienced tremendous growth over the last few decades. Various applications have been realized with wireless systems, such as radios, cellphones, satellite navigations and biomedical equipments. Taking the cellular industry as an example, it has grown from the first generation (1G) narrowband analog systems, to the second generation (2G) narrowband digital systems, to the currently thriving third generation (3G) and long-term evolution (4G LTE), which is featured by high-speed wideband multimedia systems [1]. Nowadays, the momentum of wireless telecommunication keeps increasing and the future generations are under active research and development worldwide. This fast-evolving wireless telecommunication industry has been benefited from the advances of the CMOS technology, which is characterized by low cost, high integration and low power consumption. As the featured minimum size scales down, CMOS stands out with great advantages in providing portable and affordable multi-functional wireless devices. As such, all the
1.1. GENERAL INTRODUCTION

The wireless signal propagating in open space is susceptible to electronic noise, interference and attenuation, therefore, in order to accurately retrieve the original information, high performance receivers are needed. The first downconversion stage of a very basic superheterodyne receiver is shown in Figure 1.1. The signal is collected by the antenna and then subject to a channel-selection filtering so that the adjacent channel interferers are suppressed. This is implemented with a band pass filter. Next, the signal within the interested channel is amplified by a low noise amplifier (LNA). Since the heterodyne configuration is vulnerable to the image effect, an image-reject filter might be used to suppress the image. Then the signal is subject to one or more down-conversions via down-converting mixers, yielding an intermediate frequency (IF) which is generally significantly lower than the carrier frequency. The down-converted signal is further processed by the succeeding IF stages and finally demodulated to restore the original information.

For a system of $n$ stages, the overall noise figure can be computed using Friis’
1.1. GENERAL INTRODUCTION

Equation [2]

\[ F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}}, \]  

(1.1)

where \( F_n \) and \( G_n \) are the noise factor and gain of the \( n \)th stage, respectively.

The noise factors of the first few stages are more critical in determining the overall noise factor of the cascade as the noises of the later stages are scaled down by the gains of previous stages. Therefore, LNAs with large gains are often found as the first stage in receivers. On the other hand, the image-reject filters after the LNAs are generally avoided in modern systems, because they are usually implemented with bulky, off-chip passive filters due to the high Q and linearity requirements. Another downside of using the off-chip filters is that they need 50 Ω input and output impedances. As a result, the preceding LNA is required to drive a 50 Ω load, which is power consuming. After the removal of the image-reject filter, the LNA and mixer interface can be designed to optimize the gain, linearity and so on. In fact, since the LNA and mixer designs are interdependent, they are often carefully designed as one entity. In either cases, as one of the first stages of the receiver, the design of the mixer is of great importance and is intensively studied in this thesis.

The mixers presented in this thesis are designed for low noise, high linearity, variable conversion gain, broadband matching and low power consumption. The interests in broadband circuit design originates from the current wideband multimedia wireless communication market. Variable conversion gain can extend the system’s dynamic range. Without deteriorating other parameters such as noise and linearity, the realization of variable conversion gain can further increase the system’s multifunctionality.

The following is a brief summary of the contributions of this thesis:
1.1. GENERAL INTRODUCTION

- A broadband, low-noise passive subharmonic mixer is designed in CMOS 130 nm technology. Measurement results show that compared to the current state-of-the-art subharmonic mixers, which are usually narrow-banded, the proposed passive subharmonic mixer achieves a wide 3-dB frequency range from 4.5 GHz to 8.5 GHz with a competitive low noise performance over the entire frequency range. The lowest DSB noise figure obtained is 8 dB and the average noise figure is 9 dB. Besides, a high conversion gain of 16 dB is achieved while maintaining an excellent linearity. The IP1dB and IIP3 are measured as -10.8 dBm and -3.7 dBm at 5 GHz. The corresponding OP1dB and OIP3 are as high as 6.5 dBm and 13.8 dBm respectively. The mixer has a compact size and occupies a core area of 0.49 mm$^2$.

- A broadband, low-noise variable gain mixer is implemented with CMOS 130 nm technology. By implementing gain control scheme at the IF stage, the proposed variable gain mixer achieves a low noise figure through the whole frequency and gain range. The noise performance is superior to the other recently reported variable gain mixers by a lowest noise figure measured as 3.8 dB. Moreover, the designed mixer achieves a broad operating frequency band from 1 GHz to 6 GHz and a highest gain of 25.3 dB. A 13 dB continuous conversion gain range is realized by tuning the control voltage from 0.7 V to 1.2 V. The circuit also presents a good linearity. At 5 GHz and highest gain setting, the measured input P1dB and IIP3 are -16.3 dBm and -7.9 dBm respectively. The core size of this mixer is only 0.44 mm$^2$.

- The linear-in-dB variable gain control scheme is utilised to the variable conversion gain mixer, in addition to the broadband, low-noise characters. The
proposed mixer achieves a 10 dB gain control range with a linearity error of less 
than ±0.5 dB. A superior low-noise performance is obtained that the lowest 
noise figure is measured as 3.8 dB and the low noise is maintained for different 
operating frequencies and conversion gains. The linearity of this mixer is also 
competitive. When the frequency is set at 5 GHz and the gain is set as the 
highest, the measured input P1dB is -13.8 dBm and the input IIP3 is -5.6 dBm. 
This mixer is very compact with a core size of 0.44 mm².

1.2 Thesis Organization

Chapter 2 provides some background on mixers, starting with a short description of 
the widely used parameters for characterizing mixer’s performance. Then the funda-
mental principles of both active and passive Gilbert cell based mixers are illustrated, 
with their pros and cons discussed. Models of resistor and transistor noise are pro-
vided for later noise analysis. Finally, a detailed description of the fully differential 
configuration that has been used for all the works in this thesis is given. The fo-
cus is on obtaining the differential $S_{11}$ and de-embedding the noise figure from the 
surrounding circuitry.

Chapter 3 starts with an overview of the subharmonic mixing circuit design and 
then gives a thorough explanation of the proposed passive subharmonic mixer. The 
designs of each individual part of the mixer are described in detail, with related 
theoretical analysis and mathematical calculations provided. The performance of the 
circuit is verified by measurements.

Chapter 4 begins with the introduction of the variable conversion gain mixer. 
Then the broadband transconductance with noise cancellation is discussed in detail.
The design considerations of current bleeding and inductive peaking implemented in the transconductance stage are also provided. Then two variable gain IF designs are discussed. The first one uses current steering method and the second one uses an \( R - r \) attenuation network to obtain the linear-in-dB gain variation. The measurement results of the two designs are given at the end of the chapter.

Chapter 5 concludes the thesis with a summary of the performances of the proposed designs. Possible improvements are also recommended as a reference for future works.
Chapter 2

Literature Review

2.1 Introduction

In this chapter, general ideas about mixers are presented, including the parameters that are typically used in characterizing mixer’s performance. Both passive and active mixers, specifically the Gilbert cell-based mixer, are analyzed. The advantages and disadvantages of each type of mixer are addressed. Next, resistor and transistor noise models are given. Finally, since all the designs in this thesis are doubly balanced, resulting in a fully differential configuration, components of the fully differential structure and approaches of de-embedding the effects from the surrounding circuitry are demonstrated. This provides guidelines in characterizing the performance of the proposed mixers.
2.2 Mixer Fundamentals

A frequency mixer is a 3-port device that takes two input signals and produces an output signal with a frequency that contains the sum or the difference of the input signals’ frequencies. This process can be expressed mathematically in time domain as

\[
\begin{align*}
Y_1 &= A_1 \cos(\omega_1 t) \\
Y_2 &= A_2 \cos(\omega_2 t)
\end{align*}
\]

\[
Y = Y_1 Y_2 = \frac{A_1 A_2}{2} \left\{ \cos[(\omega_1 + \omega_2)t] + \cos[(\omega_1 - \omega_2)t] \right\}.
\]

With one input being locally generated signal, which is typically a sinusoidal or a square wave signal generated by a local oscillator (LO), the other two ports, RF (radio frequency) and IF (intermediate frequency) ports, can be either used as the second input or the output, depending on whether the mixer is a downconverter or upconverter. In a transmitter, the input IF signal is up-converted to the RF signal \((\omega_{RF} = \omega_{IF} + \omega_{LO})\) for transmission purpose (Figure 2.1(a)). On the other hand, at the receiver side, the RF signal is down-converted to a baseband IF signal \((\omega_{IF} = \omega_{RF} - \omega_{LO})\), so that the original message can be extracted with further processes (Figure 2.1(b)).

In order to characterize the performance of a mixer, the following parameters are typically considered:

**Conversion Gain (Loss)** is defined as the power difference between the desired
2.2. MIXER FUNDAMENTALS

Figure 2.1: (a) Up-converting mixer and (b) down-converting mixer.

Output IF signal and the input RF signal in dB scale.

\[ CG(CL) = P_{IF}(\text{dBm}) - P_{RF}(\text{dBm}) = 10 \log \frac{\text{power of the output IF signal}}{\text{power of the input RF signal}} \]

Conversion gain (loss) is an important metric for mixers. An active mixer has conversion gain, meaning that it yields amplification along with frequency translation. On the other hand, a passive mixer has conversion loss. An advantage of using active mixer is that one of the IF amplifiers can be eliminated, and this may result in a reduced dc power consumption and a smaller chip area. However, having conversion gain does not necessarily indicate that active mixers are more favourable because passive mixers are more linear and generally produce less noise.

**Noise Figure (NF)** Noise is unavoidable in all electronic systems. It sets the floor of the system’s dynamic range, which is defined as the range between the 1 dB compression point and the minimum detectable signal level. A mixer’s noise performance is characterized by its noise factor \( F \) or noise figure NF (noise factor expressed in dB scale). The noise factor \( F \) is defined as the signal-to-noise ratio.
(SNR) at the input divided by the SNR at the output,

\[ F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} = 1 + \frac{N_{\text{added}}}{G N_{\text{in}}}, \]  

(2.2)

where \( N_{\text{added}} \) and \( G \) are the noise and gain of the device-under-test (DUT) respectively, and \( N_{\text{in}} \) is the input noise. Usually the input noise is thermal noise from the source and can be expressed as

\[ N_{\text{in}} = k T_0 B, \]  

(2.3)

where \( k \) is the Boltzmann constant, \( T_0 \) is the reference source temperature, and \( B \) is the total bandwidth for noise measurement. Assuming the DUT has an equivalent noise temperature \( T_e \) derived as [3]

\[ T_e = \frac{N_{\text{added}}}{G k B}, \]  

(2.4)

Equation (2.2) can be expressed as

\[ F = 1 + \frac{T_e}{T_0}. \]  

(2.5)

For mixers, the estimation of NF is more complicated due to the existence of the image signal, which has a frequency of \(|f_{\text{image}} - f_{\text{LO}}| = f_{\text{IF}}\). If it is assumed that all the noise output power comes from the RF channel, the NF obtained is called the single-sideband noise figure (SSB NF). On the other hand, if the noise output power is considered to come from both the RF and image channels, then the measured NF is the double-sideband noise figure (DSB NF). This mechanism can be illustrated by Figure 2.2 [4], where the mixer is considered as a noise-less component with its noise
2.2. MIXER FUNDAMENTALS

Figure 2.2: Representation of mixer NF (a) DSB NF and (b) SSB NF.

referred to the input and represented by the equivalent noise temperature \([4, 3]\), which is \(T_{SSB}\) in computing SSB NF (Figure 2.2 (a)) and \(T_{DSB}\) in the calculation of DSB NF (Figure 2.2 (b)). Assuming the equivalent noise temperature of the noise source is \(T_s\) and the conversion gain is \(G_{cr}\) from RF to IF and \(G_{ci}\) from the image channel to IF, the output equivalent noise temperature \(T_L\) can be derived as \([4]\)

\[
T_L = (T_s + T_{SSB})G_{cr} + T_sG_{ci} = (T_s + T_{DSB})G_{cr} + (T_s + T_{DSB})G_{ci}. \quad (2.6)
\]

Therefore, \(T_{SSB}\) and \(T_{DSB}\) can be obtained as \([4]\)

\[
T_{SSB} = \frac{T_L}{G_{cr}} - T_s - \frac{G_{ci}}{G_{cr}} T_s \quad (2.7)
\]

\[
T_{DSB} = \frac{T_L}{G_{cr} + G_{ci}} - T_s. \quad (2.8)
\]
Given the assumptions that $G_{cr} = G_{ci}$ and $T_s = T_0 = 290 K$, it can be seen that [4]

\begin{align*}
T_{SSB} &= 2T_{DSB} \\[2pt]
F_{SSB} &= \frac{(T_s + T_{SSB})G_{cr} + T_s G_{ci}}{G_{cr}T_0} = \frac{T_{SSB}}{T_0} + 2 \\[2pt]
F_{DSB} &= \frac{(T_s + T_{DSB})(G_{cr} + G_{ci})}{(G_{cr} + G_{ci})T_0} = \frac{T_{DSB}}{T_0} + 1.
\end{align*}

Thus, $F_{SSB} = 2F_{DSB}$ can be readily obtained. It is also interpreted as $NF_{SSB}$ is 3 dB higher than $NF_{DSB}$.

**1 dB Compression Point (P1dB)** It is defined as the point where the gain is compressed by an amount of 1dB. It can be characterized by either the input or output signal level, namely IP1dB and OP1dB. Together with the conversion gain, P1dB is an important parameter of a mixer, as it sets the ceiling of a mixer’s dynamic range. Mixers work beyond P1dB suffers from higher conversion loss, with the input RF power converted into heat and higher order intermodulation products instead of the desired IF output power [5].

**Intermodulation Distortion (IMD)** In most real-word scenarios, a multi-tone signal is present at the input of the mixer. These multiple tones intermodulate with each other and LO signal through the nonlinear mixing process, resulting in IMDs $f_{IMD} = m f_{RF1} \pm n f_{RF2}$, where $m$ and $n$ are integers. Among these IMDs, the two-tone third-order IMDs $(2f_{RF2} - f_{RF1})$ are of primary attention since they tend to fall within the IF bandwidth and ultimately degrade mixer’s performance. The two-tone third-order intercept point (IP3) is therefore widely used in characterizing the multi-tone performance of a mixer. It is defined as the extrapolated intersection of the fundamental output curve and the third-order IMD output curve, all versus
the input power.

**Isolation** In mixers, there is always some power leakage among ports due to the device parasitic capacitances and the finite substrate resistance. Isolation is an important parameter describing how much inter-port rejection is provided by the mixing circuit. Poor LO-to-RF isolation may result in the contamination of the RF signal. In even worse cases, the LO signal may radiate through the antenna and be received again, causing LO self-mixing, which is especially problematic in direct conversion systems. Poor LO-to-IF isolation may result in the desensitization of the IF mixer(s) and the saturation of the IF amplifier(s), and therefore requires low pass filter(s) to suppress it. Poor RF-to-IF isolation, on the other hand, yields poor conversion efficiency, which results in a poor conversion gain (loss). As such, balanced topology is widely used in mixer designs in order to achieve good isolations. The most representative double-balanced design is the Gilbert Cell mixer, which is going to be described in detail in the next section.

### 2.3 Mixer Topologies

Many mixer configurations have been proposed over time for various applications. For example, a mixer can be active or passive depending on whether dc power is dissipated and single-balanced or double-balanced depending on its configuration. An active mixer can provide conversion gain while usually suffer from low voltage headroom and poor noise performance. On the other hand, a passive mixer usually has conversion loss but presents good noise and linearity. In this section, only Gilbert cell-based active and passive field effect transistor (FET) mixers are discussed, whereas the discussion on diode mixers, single FET mixers and single balanced structures are
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not included for the reason that good summary can be found in various references [6, 7].

2.3.1 Gilbert Cell Mixer

General Concept The Gilbert cell [8] started as a low-frequency analog multiplier but as semiconductor transistors got faster over the decades, the Gilbert cell has reached the microwave region. Due to its double-balanced configuration, Gilbert cell mixer presents good port-to-port isolation, relative high gain and even-order distortion rejection. As a fully differential structure, it has a differential RF and LO input, as well as a differential IF output taken from cross-coupled connected drains, as shown in Figure 2.3. In order to understand how Gilbert cell mixer works, half of the circuit shown in Figure 2.4 (a) is analysed first. Assume the LO is an ideal

Figure 2.3: Gilbert cell mixer.
square wave and transistors $M_1$ and $M_2$ act as perfect switches, which turn on and off according to the LO swing. The current from the transconductance stage is then steered between the two branches, as shown in Figure 2.4 (b). From transistor $M_5$’s point of view, its output current is routed to a load $R_{\text{load}}$, either through $M_1$ or $M_2$. As such, when studying the transconductance stage $M_5$, the switching pair $M_1$ and $M_2$ can be equivalently viewed as a cascade transistor $M_{\text{equi}}$ as shown in Figure 2.4 (c), with its gate biased at a fixed value $V_B = V_{B,\text{LO}} + A_{\text{LO}}$, where $V_{B,\text{LO}}$ is the dc bias voltage at the gates of the switching transistors and $A_{\text{LO}}$ is the amplitude of the LO square wave. $V_B$ is chosen to ensure transistor $M_5$ and $M_{\text{equi}}$ work in saturation region. It can therefore be noticed that the node voltage $V_X$ manifests itself in corresponding to the input voltage $V_{RF}^+$ and as a result, the current $I_5$ is routed to the load $R_{\text{load}}$.

Figure 2.4: (a) Half circuit of the Gilbert cell mixer and (b) Illustration of the current steering functions by interpreting MOSFETs as switches and (c) Equivalent cascade structure.
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The transconductance current $I_5$ is composed of the dc bias current and the small-signal current generated by the small-signal input $v_{RF}^+ = V_{RF} \cos(\omega_{RF}t)$,

$$I_5 = \frac{I_{DC}}{2} + g_m V_{RF} \cos(\omega_{RF}t).$$  \hspace{1cm} (2.12)

Ideally, only one switch is on at a time and the transconductance current is steered from one branch to another 2.4 (b). The resulting effect is equivalent to multiply the transconductance current $I_5$ with a square wave, which swings from $+1$ to $-1$ at the LO frequency. This square wave can be expressed as the sum of the odd harmonics of its fundamental frequency $f_{LO}$. Therefore, the following equations are valid,

$$f_{\text{squareWave}}(t) = \frac{4}{\pi} \left[ \cos(\omega_{LO}t) - \frac{1}{3} \cos(3\omega_{LO}t) + \frac{1}{5} \cos(5\omega_{LO}t) + \ldots \right]$$ \hspace{1cm} (2.13)

$$I_1 - I_2 = I_5 \cdot f_{\text{squareWave}}(t)$$

$$= \frac{2}{\pi} I_{DC} \left[ \cos(\omega_{LO}t) - \frac{1}{3} \cos(3\omega_{LO}t) + \ldots \right] + \frac{2}{\pi} g_m V_{RF} \{ \cos(\omega_{RF} - \omega_{LO})t$$

$$+ \cos(\omega_{RF} + \omega_{LO})t - \frac{1}{3} [\cos(\omega_{RF} - 3\omega_{LO})t + \cos(\omega_{RF} + 3\omega_{LO})t] + \ldots \}.$$ \hspace{1cm} (2.14)

It can be seen in Equation (2.14) that the harmonics of the LO frequency are directly presented at the output. This indicates that the single-balanced configuration has a poor LO-to-IF isolation. In order to eliminate the LO harmonics, double-balanced structure is introduced, which is represented by the Gilbert cell shown in Figure 2.3. Due to the circuit symmetry, the other half circuit presents an output
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\[ I_4 - I_3 = I_6 \cdot f_{\text{squareWave}}(t) = \left[ \frac{I_{\text{DC}}}{2} - g_m V_{\text{RF}} \cos(\omega_{\text{RF}} t) \right] \cdot f_{\text{squareWave}}. \]  \hspace{1cm} (2.15)

Therefore, the output voltage is derived as

\[ v_{IF} = [V_{DD} - (I_1 + I_3) R_{load}] - [V_{DD} - (I_2 + I_4) R_{load}] \]
\[ = [(I_1 - I_2) - (I_4 - I_3)] R_{load} \]
\[ = \frac{4}{\pi} g_m R_{load} V_{RF} \{ \cos(\omega_{\text{RF}} - \omega_{\text{LO}}) t + \cos(\omega_{\text{RF}} + \omega_{\text{LO}}) t \}
\[ - \frac{1}{3} \{ \cos(\omega_{\text{RF}} - 3\omega_{\text{LO}}) t + \cos(\omega_{\text{RF}} + 3\omega_{\text{LO}}) t \} + \ldots \}. \]  \hspace{1cm} (2.16)

Note that the common-mode DC component is cancelled in this double-balanced structure, which ultimately eliminates the LO harmonics and achieves a good LO-to-IF isolation.

The conversion gain can also be readily obtained in the following equation,

\[ CG = \frac{|v_{IF}|}{|v_{RF}|} = \frac{2}{\pi} g_m R_{load}. \]  \hspace{1cm} (2.17)

2.3.2 Passive Mixers

It can been seen that active Gilbert cell mixers are current-commutating mixers with dc current component flowing through the switching pairs. It has been indicated in previous researches that flicker noise contributed by the FET switches at the output is proportional to the steered dc bias current [9]. Several approaches have been proposed to reduce the dc bias current [10, 11]. The dc current not only contributes to the flicker
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noise problem but also introduces a large dc voltage drop across the load, which results in a limited voltage swing and linearity degradation in low supply voltage designs. Thus, passive Gilbert cell mixers are implemented to improve the noise, linearity issues while maintaining the advantages such as high port isolations and even-mode distortion rejections provided by the double-balanced Gilbert cell topology. This section interprets the fundamentals of passive Gilbert cell mixers, which, differ from the active ones, can commutate both voltage and current. Passive mixers commutate voltage signals are referred to as voltage-driven passive mixers, while passive mixers commutate current signals are referred to as current-driven passive mixers.

Voltage-Driven Passive Mixers

The configuration of the double-balanced voltage driving passive mixer is plotted in Figure 2.5, where the voltage signal is commutated by the differential pairs in deep triode driven by LO and $C_L$ represents the capacitive load, for example the input capacitance of the subsequent stage. The I-V property for submicrometer devices in triode region using BSIM3V3.2 model is expressed as [12]

\[
I_{ds} = \mu_n C_{ox} \frac{W}{L} \frac{1}{1 + \frac{V_{gs}}{E_{sat}L}} (V_{gs} - V_{Th} - \frac{A_{bulk} V_{ds}}{2}) V_{ds},
\]

where $\mu_n$ is the electron mobility of the NMOS switch, $C_{ox}$ is the oxide capacitance per unit area, $W$ and $L$ stand for the width and length of the device, $E_{sat}$ is the saturated electrical field, $V_{TH}$ represents the threshold voltage, while $A_{bulk}$ corresponds to the bulk charge effect. Since the conductance of each switching transistor is controlled
by the gate voltage, which can be given in (2.19) as

\[
g(t) = \begin{cases} 
\frac{\partial I_{ds}}{\partial V_{ds}} \bigg|_{V_{ds}=0} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{TH}) & \text{when switch is ON} \\
0 & \text{when switch is OFF,}
\end{cases}
\]

in which \( V_{gs} = V_{LO}(t) + V_G - V_S - V_{TH} \), with \( V_{LO}(t) \) represents the LO waveform, \( V_S \) corresponds to the dc voltage at the drain and the source of the transistors, and \( V_G \) refers to the dc voltage at the gate of the transistors. Since \( LO^- \) is just the time-shifted version of \( LO^+ \), by replacing the conductances of the switches with \( g(t) \) and \( g(t - \frac{T_{LO}}{2}) \), a Thevenin equivalent circuit seeing from \( C_L \)'s point of view can be derived as shown in Figure 2.6 [13].

The open-circuit voltage and Thevenin impedance are derived as [13]
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![Thevenin equivalent circuit viewing from $C_L$.](image)

\[ v_T(t) = \frac{g(t - \frac{T_{LO}}{2}) - g(t)}{g(t) + g(t - \frac{T_{LO}}{2})} v_{RF}(t) = m(t)v_{RF}(t) \quad (2.20) \]

\[ g_T(t) = \frac{g(t) + g(t - \frac{T_{LO}}{2})}{2}, \quad (2.21) \]

where the mixing function $m(t)$ can be readily obtained as [13]

\[ m(t) = \frac{g(t - \frac{T_{LO}}{2}) - g(t)}{g(t) + g(t - \frac{T_{LO}}{2})}. \quad (2.22) \]

Since the terminal voltages of this passive mixer are determined by the external voltage biases, depending on the dc bias at the gate $V_G$ and the source $V_B$, the voltage-driven passive mixer can be operated in three different modes: ON overlap, zero overlap and OFF overlap [14, 15], where overlap refers to the time slot during which both transistors are in the same state. ON overlap and OFF overlap are also called as make-before-break and break-before-make respectively in [13, 16]. Square wave LO and sinusoidal LO signals that drive the passive mixer in three modes are investigated in [13] and depicted in Figure 2.7 (a), the resulting mixing function and equivalent Thevenin transconductance are shown in Figure 2.7 (b).
The derivation of conversion gain is different for two conditions: (1) $C_L = 0$ and (2) $C_L \neq 0$ [13]. For $C_L = 0$, $v_{IF}(t) = v_T(t)$ and the voltage conversion gain for the four LO drives stated above is listed in Reference [13], among which both square wave LO and sinusoidal LO for zero overlap mode yield a conversion gain of $2/\pi$. On the other hand, if $C_L \neq 0$, which is a more realistic case, superposition integral is employed after obtaining the network’s impulse response and the mixing function is modified to [13]

$$m'(t) = \frac{g_T(t)}{g_{T_{max}}} m(t), \quad (2.23)$$
### 2.3. MIXER TOPOLOGIES

If $\frac{g_T}{(2\omega_{LO}C_L)} \ll 1$ is satisfied, where $g_T$ represents the dc level of $g_T$. $g_{T\text{max}}$ corresponds to the peak conductance of $g_T(t)$ and is implemented to normalize $m'(t)$ to vary within the range of $[-1,1]$. The resulting $v_{IF}$ as a function of $v_{RF}$ is also given in [13] and expressed as

$$v_{IF} = \int_{-\infty}^{t} \frac{g_T}{C_L} e^{-\frac{g_T}{v_T}(t-\tau)} Am'(\tau)v_{RF}(\tau) d\tau,$$

where $A = \frac{g_{T\text{max}}}{g_T}$. It is further observed that Equation (2.24) resembles the superposition integral of a single-pole low-pass filter. Therefore, it is concluded that when the signal voltage $v_{RF}$ is imposed at the input of the voltage-driven passive mixer which is loaded by a capacitive load $C_L$, it is multiplied by a mixing function $m'(t)$, amplified by a factor $A$ and then filtered by a single-pole low-pass filter [13]. The block diagram for this process is shown in Figure 2.8.

It is reported in [12, 17] that single-balanced voltage-driven passive mixer as shown in Figure 2.9 (a) provides a conversion gain, 2.1 dB as reported in [12] or 1.186 dB as demonstrated in [17]. This is a voltage conversion gain approximately 6 dB higher than the double-balanced topology discussed above. Reference [18] proposed a way to achieve a comparable conversion gain with double-balanced configuration by adding
Figure 2.9: (a) Simplified schematic of the single-balanced voltage-driven passive mixer and (b) Conceptual illustration of summing the outputs of two single-balanced mixers in current domain.

Although the voltage-driven passive mixer is usually loaded with the small capacitance of the next stage and the input impedance looking into the voltage-driven passive mixer is assumed to be high, it may present an appreciable loading effect to the LNA. It is demonstrated in [17] that the input impedance $Z_{in,SB}$ of the single-balanced structure shown in Figure 2.9 (a) can be obtained as

$$Z_{in,SB} = \frac{1}{2} \left\{ R_{ON} + \frac{1}{jC_L\omega_{in}} \left[ \frac{1}{2} + \frac{1}{j\omega_{in}T_{LO}} (1 - e^{-j\omega_{in}T_{LO}/2}) \right] \right\} ,$$

where $R_{ON}$ is the ON-resistance of the transistors, $C_L$ is the load capacitance, $\omega_{in}$ is the angular velocity of the input signal and $T_{LO}$ is the period of the LO signal.
Current-Driven Passive Mixers

When driven by current source, passive mixers present different properties. Figure 2.10 (a) shows the architecture of a current-commutating passive mixer, where the transconductance stage is modeled as a current source with a high output impedance $Z_S$, and the differential input impedance of the next stage is $2Z_L$. The signal current from the transconductor is ac coupled into the switching core through the capacitor $C$, which ensures the switching transistors to operate in deep triode region with no dc bias current flowing through. Therefore the associated flicker noise is significantly reduced. Then the down-converted current is loaded by the input impedance $Z_L$ of the next stage, which is generally a transimpedance amplifier (TIA). Similar to the voltage-driven passive mixer, the dc bias voltage at the drain and source of a
current-driven passive mixer, $V_B$ in Figure 2.10, is set by the input bias voltage of the TIA [19], and results in three operation modes: On-overlap, zero-overlap and OFF-overlap [19, 14, 20, 16, 15]. Although a voltage-driven passive mixer can work in all three modes as discussed before [14], and an active mixer always works in ON overlap because all the transistors in a switching pair are ON during the transition period [14], a current-driven passive mixer is preferred to be operated in ON overlap in order to eliminate large voltage swing at the input when all of the switches are momentarily off during the overlap period [19]. The LO switch should be strong to minimize the overlap period.

Assuming the transistors are driven by an ideal square wave LO with 50% duty cycle, in which case at any moment, one transistor is on in a switching pair. Since the on transistor is in deep triode region, it can be modeled as an ON-resistor $R_{ON}$ in series with an ideal switch as shown in Figure 2.11(a), where $Z_{L,RF}$ stands for the load impedance $Z_L$ after being transformed into the RF domain. The junction and parasitic capacitances of the switching transistors are not shown here because they can be easily lumped into the RF or IF impedances if they are not negligible [21].

The output voltage $v_{IF}(t)$ is obtained as [21, 22]

$$v_{IF}(t) = [i_{RF}(t) \cdot f_{squareWave}] \ast 2Z_L(t), \quad (2.26)$$

where * is the convolution integral. Due to the lack of reverse isolation between the RF and IF sections, the same mixer also acts as a voltage commutating mixer by translating the voltage across the IF loads to the RF side. This can be interpreted by envisaging the topology shown in Figure 2.11(a) as the structure shown in Figure 2.11(b), where $v_{IF}(t)$ is the source voltage while $v_{RF}(t)$ is its resulting open load
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Figure 2.11: (a) Passive current-driven mixer with switching transistors modeled as on resistances in series with ideal switches and (b) passive current-driven mixer commutes the IF voltage to the RF side.

output voltage. According to the symmetry between the source and drain terminals, $v_{IF}(t)$ experiences the same square wave function of the switches and the expression of $v_{RF}(t)$ is derived as

$$v_{RF}(t) = v_{IF}(t) \cdot f_{squareWave} = \{[i_{RF}(t) \cdot f_{squareWave}] \ast 2Z_L(t)\} \cdot f_{squareWave}.$$  \hspace{1cm} (2.27)

The input impedance $Z_{L,RF}$ can be derived as [22]

$$Z_{L,RF} = \frac{4}{\pi^2} \sum_{n=1,3,5,...}^{\infty} \frac{1}{n^2} [Z_L(n\omega_{LO} + \omega_{RF}) + Z_L^*(n\omega_{LO} - \omega_{RF})].$$  \hspace{1cm} (2.28)

It is further investigated in [22] that if the IF load is resistive, $Z_L = R_L$, then $Z_{L,RF} = R_L$ is observed. On the other hand, if the IF load is capacitive with a capacitance of
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Ignoring the higher order terms, the input impedance $Z_{L,RF}$ is computed as

$$Z_{L,RF} \approx \frac{j8}{\pi^2 C_L \omega_{LO}^2 - \omega_{RF}^2} \approx \begin{cases} \frac{4}{\pi^2} \cdot \frac{1}{j(\omega_{RF} - \omega_{LO})C_L}, & \omega_{RF} \approx \omega_{LO} \\ \frac{8}{\pi^2} \cdot j\omega_{RF} \left(\frac{1}{\omega_{LO}^2 C_L}\right), & \omega_{RF} \approx 0, \end{cases}$$

It is reported in [21] that if the source load $Z_S$ is a parallel LC, by making the ac coupling capacitor $C$ resonate with $Z_S$, the current flowing through $C$ and commutated by the switching core can be the current from the transconductance stage magnified by a factor, which is the effective $Q$ of $Z_S$ and $C$. A maximum conversion gain can be obtained as [21]

$$CG_{max} = \frac{1}{2\pi} \sqrt{\frac{R_p}{R_{ON} + \frac{2}{\pi^2} R_L}},$$

where the IF load impedance $Z_L$ is assumed to be purely resistive with a value of $R_L$ and the inductor loss is modeled by a parallel resistor $R_p$. This is a larger conversion gain than that of the conventional design [23, 24], where the transconductor current is simply delivered to the mixer through a large series capacitor $C$ without magnification.

2.4 Noise Model

As a critical parameter of a down-converting mixer, noise has been extensively studied, both for active mixers [25, 9] and passive mixers [14, 19]. The most commonly discussed noises are flicker noise and thermal noise. The former one dominates at the low frequencies and the latter is more critical at the higher frequencies. In this section, only the most relevant noise sources are modeled to provide a background
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Resistor Thermal Noise

The random thermal agitation of the charges in a conductor introduces a random voltage fluctuation across the conductor, which has a zero average current. The power spectral density is given by [26]

\[ \overline{V_{n,R}^2} = 4kTR, \]

where \( k \) is the Boltzmann constant. It is shown that the spectral density of the resistor thermal noise is proportional to the temperature and remains flat over a wide frequency range, which is up to THz. Resistor thermal noise can be represented as a series voltage source or a parallel current source with a noiseless resistor as shown in Figure 2.12. Note that only when loaded by the matched load, a maximum noise power is delivered, which is referred to as the maximum available noise of a resistor.

Transistor Noise

The thermal noise in MOSFETs is mainly the drain current for later noise analysis, while for the noise analysis on circuit level and for different types of mixers, the reader is referred to [25, 9, 14, 19, 17].

Figure 2.12: Two representations of the resistor thermal noise (a) series voltage source and (b) parallel current source.
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Figure 2.13: Drain current noise modeled as a parallel current source connected between the drain and source terminals.

noise due to the fact that they behave as voltage-controlled resistors. It is commonly modelled as a current source connected between the drain and the source as shown in Figure 2.13. The spectral density is

\[ I_{nd} = \sqrt{4kT\gamma g_m}, \]

where \( \gamma \) is the excess noise coefficient and \( g_m \) is the drain-source conductance when \( V_{ds} = 0 \). The value of \( \gamma \) depends on the technology, which is unity when \( V_{ds} \) is zero and reduced to 2/3 for long-channel devices in saturation. For short-channel FETs, \( \gamma \) increases to a larger value [26, 6].

Another noise presents in FETs is the flicker noise, which is also referred to as 1/f noise. It is originated from random trap and release of the charge carriers at the interface between the silicon crystal and the gate oxide due to the dangling bonds. It is commonly modeled as a voltage source in series with the gate as shown in Figure 2.14 (a) and its spectral density is expressed as

\[ \overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f}. \]
Figure 2.14: Transistor flicker noise (a) modeled as a series voltage source at the gate and (b) modeled as a parallel current source connected between the drain and source terminals.

where $K$ is a constant depend on the process. It can be seen that flicker noise can be reduced by increasing the device size. Also, PMOS devices tend to have better flicker noise performance due to the buried-channel effect [27]. The other way of modelling flicker noise is to refer it to the drain and model it as a current source connected between the drain and the source of the transistor, as depicted in Figure 2.14 (b), in which case the spectral density modifies to

$$
\bar{I}_n^2 = \frac{K g_m^2}{C_{ox} WL} \cdot \frac{1}{f}.
$$

(2.34)

The significance of these two noises in MOSFET is usually characterized by the $1/f$ noise corner frequency,

$$
f_C = \frac{K}{C_{ox} WL g_m \frac{\gamma}{2kT}}.
$$

(2.35)

Figure 2.15 shows that below $f_C$, the noise is dominant by the flicker noise whereas for frequencies above $f_C$, thermal noise is more crucial.
2.5. FULLY DIFFERENTIAL CONFIGURATION

The differential configuration has many advantages over its single-ended (S-E) counterpart, such as high immunity to common mode interference and elimination of even-order nonlinearity [28, 29]. Besides, differential structure can also provide twice voltage swings of the S-E configuration, which is very attractive as lower supply voltage is favourable in modern communication devices. Therefore, many circuits are designed to be differential, such as low noise amplifiers and mixers. In addition to the above stated advantages, the differential configuration provides high port isolations for mixers due to its double-balanced structure. Thus, lots of widely used mixers, for instance the Gilbert Cell based mixers, adopt differential topologies. However, despite of the wide application of the differential circuits, commonly used measuring instruments, such as the power spectrum analyzer (PSA) and vector network analyzer (VNA), can still only provide a S-E stimulus and receive a S-E input. Therefore,
additional circuits are usually implemented to provide the single-end to differential conversion or vice versa. This can be realized either by on-chip circuits or off-chip devices such as power splitting/combining baluns. In this thesis, the fully differential structure is used in all three designs. In order to achieve a better understanding, each part of the differential structure is investigated. An approach of excluding the effects of the off-chip components is also illustrated so that the performance of the on-chip designs can be properly evaluated.

As shown in Figure 2.16, the input S-E signal is converted into a differential signal through a passive balun. Then the differential signal is injected into the on-chip differential mixing circuit and the final output differential signal is terminated with an active buffer, which converts the differential signal back to a S-E signal. At the same time, the buffer acts as a high impedance load for the mixer. It also provides a low output impedance of 50 Ω to match the input impedance of the following measuring instrumentations. Note that all the off-chip components and measuring equipment are connected by coaxial cables and the differential probes are used to implement the on-wafer tests.

Figure 2.16: Schematic of the fully differential configuration.
2.5. FULLY DIFFERENTIAL CONFIGURATION

2.5.1 Passive Balun

A passive balun is usually based on a hybrid transformer and splits the input signal power stimulated at port 1 equally between port 2 and port 3, but with 180° phase difference (Figure 2.17). According to Reference [28], a passive balun is also bidirectional, which means that if any two of its three ports are loaded with the standard resistance, usually 50 Ω, then the input impedance looking into the last port is 50 Ω as well. In order to satisfy the above characteristics, a balun model shown in Figure 2.17 is obtained and used in circuit schematic simulations, where \( R \) is the internal resistor to dissipate the common-mode component of the incident power. For chip measurements, an 180° hybrid coupler made by KRYTAR company is chosen to realize the S-E to differential conversion. The model used is 4010180, which works from 1 to 18 GHz, and presents less than ±0.6 dB amplitude mismatch and ±12 degrees phase mismatch. Ideally, the power is equally split at port 2 and 3. Thus, if the input voltage at port 1 is denoted as \( V_1 = V_{in} \), the output voltages at port 2 and 3 are \( V_2 = V_{in}/\sqrt{2} \) and \( V_3 = -V_{in}/\sqrt{2} \) respectively. Note that \( V_2 \) and \( V_3 \) are correlated, which gives a differential voltage of \( \sqrt{2}V_{in} \) across port 2 and 3. Due to this mechanism, there is a 3 dB voltage boost through the balun. This 3 dB voltage gain is compensated by subtracting 3 dB from the measurement data, so the results reported in this thesis characterize the performance of the on-chip circuits only.

2.5.2 High Linearity Off-Chip Buffer

Due to the linearity degradation and power consumption of on-chip buffer, in this thesis a highly linear off-chip buffer is used. The buffer is MAX4444 produced by Maxim Integrated Products, Inc and soldered on a commercially available circuit
2.5. FULLY DIFFERENTIAL CONFIGURATION

Figure 2.17: Passive balun (a) symbol and (b) balun model used for schematic simulations.

board. The original two 50 Ω input matching resistors are removed from the board for the purpose of providing a high load impedance to the mixing circuit. It serves as a differential-to-single-ended voltage converter which presents a voltage gain of 2 V/V. The output impedance is 0.7 Ω and the input parasitic capacitance as well as the differential input resistance of the buffer are estimated as 2.5 pF and 82 kΩ respectively. In order to achieve a voltage conversion gain of 1 V/V and match the output impedance to the load, a 50 Ω SMA resistor is connected at the output port of the buffer. Therefore, the buffer model shown in Figure 2.18 is obtained for schematic simulation.

2.5.3 Characterization of the Differential Configuration

In measuring the differential circuits, either advanced instrument which can provide differential stimulus or converting the results from S-E measurements is needed. Due to the availability of S-E equipment, the latter is used in this thesis. Namely, measured results are further processed to extract the parameters of on-chip circuits. The
2.5. FULLY DIFFERENTIAL CONFIGURATION

approaches used to obtain each parameter are explained in the following content.

**Differential Input Reflection Coefficient \( S_{11}^{\text{diff}} \)** since only a 2-port network analyzer is available, the differential input reflection coefficient \( S_{11}^{\text{diff}} \) is obtained by conducting a full two-port measurement for the input differential ports [30, 31]. First a full two-port calibration is conducted on a substrate wafer. Then \( S_{11}, S_{12}, S_{21} \) and \( S_{22} \) are recorded from a full two-port measurement, and the equivalent differential input reflection coefficient \( S_{11}^{\text{diff}} \) is calculated from Equation (2.36) [31]

\[
S_{11}^{\text{diff}} = \frac{1}{2}(S_{11} - S_{21} - S_{12} + S_{22}).
\]  

(2.36)

In the rest of the thesis, all the measured input reflection coefficients reported refer to the differential input reflection coefficient and denoted as \( S_{11} \).

**Conversion Gain and Linearity** For conversion gain and linearity measurement, the balun-chip-buffer cascade is measured as one block. The gain (loss) of off-chip devices, namely the power splitting balun and the active buffer can be measured independently so that their contribution to the conversion gain of the mixing

Figure 2.18: Circuit model for the off-chip buffer.
circuit can be simply compensated. They are also assumed to be linear enough to not affect the linearity of the on-chip circuit. So the result of linearity measurement is used as-is.

**De-embedding the Noise Figure of the Mixing Circuit**

Noise factor is measured for the balun-chip-buffer cascade with S-E instruments as shown in Figure 2.16, where the noise source is a HP 346B noise source works from 10MHz to 18 GHz and the output noise is measured by an Agilent PSA E4446A which works from 3 Hz to 44 GHz. Since both the off-chip balun and the active buffer contribute noise, the noise of the on-chip circuit needs to be de-embedded from the measured cascade noise, which is commonly done by the Friis’ equation [2]. However, the Friis’ equation is for calculating the noise factor of the two-port cascade, whereas the differential structure used involves three-port balun and buffer. Reference [28] provides an analysis of extending Friis’ equation to three-port by taking the noise correlation into consideration. Nevertheless, the power quantities used in [28] are not directly available in the differential configuration proposed in this thesis due to the high input impedance of the active buffer. Hence, an approach of adapting the noise de-embedding method in [28] with voltage quantities as in the direct method [17] is derived and illustrated in the following content.

Suppose that the differential mixer consists of two identical S-E mixers as shown in Figure 2.19, and each has an unloaded voltage gain $A_{v,Mix}$. Assume the balun and buffer are noise-free. If an S-E stimulus, which has a root-mean-square (rms) voltage of $V_{in}$, is presented at the input of the balun, the resulting differential voltage across port 1 and 2 of the buffer is $\sqrt{2}A_{v,Mix}V_{in}$. For the incident thermal noise voltage $V_n$ originated by the source resistor, it experiences the same gain as $V_{in}$ and therefore
Figure 2.19: Signals and noises in a differential mixer connected to an ideal balun and buffer.

presents a correlated differential waveform across the port 1 and 2 of the buffer, which has an equivalent noise spectral density of $\sqrt{2}A_{v,\text{Mix}}V_n$. Meanwhile, refer the noise in each S-E mixer to the output as two uncorrelated voltage sources and assume each has a spectral density of $V_{n,\text{Mix}}$, the value of the equivalent differential noise voltage presented across port 1 and 2 of the buffer is therefore $\sqrt{2}V_{n,\text{Mix}}$. As a result, the signal-to-noise ratio (SNR) at the output of the cascade can be obtained as

$$SNR_{\text{out}} = \frac{(\sqrt{2}A_{v,\text{Mix}}V_{\text{in}})^2}{(\sqrt{2}A_{v,\text{Mix}})^2V_n^2 + (\sqrt{2})^2V_{n,\text{Mix}}^2} = \frac{A_{v,\text{Mix}}^2V_{\text{in}}^2}{A_{v,\text{Mix}}^2V_n^2 + V_{n,\text{Mix}}^2}.$$  (2.37)

This result shows that with ideal, noise-free balun and buffer, the differential mixer presents the same noise factor as its constituting S-E mixer.

In practice, both balun and buffer are not noise-free, and their effects need to be de-embedded from the measured results so that the noise of the differential mixing circuit can be obtained. Figure 2.20 shows the structure for noise de-embedding. It
is assumed that port 2 and 3 of the passive balun are symmetrical, and both have an unloaded voltage gain of $A_{v,Bal}$ and an output noise voltage $V_{n,Bal}$, which are uncorrelated to each other. The same holds for the buffer, port 1 and 2 are assumed to be identical and the unloaded voltage gain from port 1 (port 2) to 3 is $A_{v,Buf}$. The buffer’s output noise voltage is denoted by $V_{n,Buf}$.

Figure 2.20: Schematic for de-embedding the noise figure of the differential configuration.

It can be shown that the output voltage at IF frequency $V_{out,IF}$ is

$$V_{out,IF} = \frac{Z_{in}}{R_s + Z_{in}} 2 A_{v,Bal} A_{v,Mix} A_{v,Buf} \frac{R_0}{Z_{out} + R_0} V_{in,RF},$$

(2.38)

where $Z_{in}$ and $Z_{out}$ are the input and output impedance of the cascade, while $R_s = R_0 = 50\,\Omega$ is the characteristic impedance of the measuring instruments. The factor 2 is due to the correlation of signals on the differential path. Assume the input and
the output are well matched, the cascade voltage conversion gain can be obtained as

\[ A_{v,Casc} = \frac{V_{out,IF}}{V_{in,RF}} = \frac{1}{2} A_{v,Bal} A_{v,Mix} A_{v,Buf}. \] (2.39)

According to the definition of noise factor, the cascade noise factor can be obtained as

\[ F_{Casc} = \frac{V_{n,out}^2}{A_{v,Casc}^2 V_{n,RS}^2} = 1 + \frac{V_{n,added}^2}{A_{v,Casc}^2 V_{n,RS}^2}. \] (2.40)

Note that the output noise at port 2 and 3 of the balun and the output noise of each S-E mixer are uncorrelated with each other, \( V_{n,added}^2 \) can be calculated as

\[ V_{n,added}^2 = (2A_{v,Mix}^2 A_{v,Buf}^2 V_{n,Bal}^2 + 2A_{v,Buf}^2 V_{n,Mix}^2 + V_{n,Buf}^2) \left( \frac{R_0}{Z_{out} + R_0} \right)^2. \] (2.41)

The noise factor and voltage gain from port 1 to port 2 (port 3) of the balun can be measured by using the structure as shown in Figure 2.21 (a). Similarly, the noise factor and voltage gain of buffer can be measured as illustrated in Figure 2.21 (b). It
2.5. FULLY DIFFERENTIAL CONFIGURATION

can then be shown that

\[
F_{\text{Bal}} = 1 + \frac{V_{n,\text{Bal}}^2}{(R_S+Z_{in,\text{Bal}})^2 A_{v,\text{Bal}}^2 V_{n,\text{RS}}^2}, \quad (2.42)
\]

\[
F_{\text{Buf}} = 2 + \frac{V_{n,\text{Buf}}^2}{(R_S+Z_{in,\text{Buf}})^2 A_{v,\text{Buf}}^2 V_{n,\text{RS}}^2}, \quad (2.43)
\]

where the input impedance of the balun and the buffer are assumed as \(Z_{in,\text{Bal}} = 50\Omega\) and \(Z_{in,\text{Buf}} = \infty\). The factor 2 in Equation (2.43) is due to the noise contribution from both the noise source as well as the termination load \(R_0\) at the other input port.

Following the same procedure, the noise of the mixer is derived as

\[
F_{\text{Mix}} = 1 + \frac{V_{n,\text{Mix}}^2}{(R_S+Z_{in,\text{Mix}})^2 A_{v,\text{Mix}}^2 V_{n,\text{RS}}^2}, \quad (2.44)
\]

where \(Z_{in,\text{Mix}} = 50\Omega\) is assumed because the input of the mixer is designed to be well-matched over the measured frequencies.

Substituting equations (2.41) to (2.44) into Equation (2.40), the noise factor of the cascade is expressed as

\[
F_{\text{Casc}} = 1 + \frac{F_{\text{Bal}} - 1}{2} + \frac{F_{\text{Mix}} - 1}{2 A_{v,\text{Bal}}^2} + \frac{F_{\text{Buf}} - 2}{A_{v,\text{Buf}}^2 A_{v,\text{Mix}}^2}, \quad (2.45)
\]

where \(F_{\text{Casc}}, F_{\text{Bal}}, F_{\text{Buf}}, A_{v,\text{Bal}}, A_{v,\text{Buf}}\) and \(A_{v,\text{Casc}}\) are all measurable parameters with S-E instrumentations while \(A_{v,\text{Mix}}\) can be calculated from Equation (2.39). Hence, the noise factor of the differential mixing circuit \(F_{\text{Mix}}\) can be derived.
2.6 Conclusion

This chapter provides the general ideas about mixers and the parameters used in mixer characterizations. Then the Gilbert cell based active and passive mixers are analyzed in detail. Next, models of resistor and transistor noise are reviewed as a background for later noise analysis. Finally, the fully differential structure that is used for all the designs in this thesis are well illustrated. Methods of obtaining each parameter have been given and serve as the guideline for data processing.
Chapter 3

A Broadband Low-Noise 2x Subharmonic Mixer

3.1 Introduction

Subharmonic mixers (SHM) can reduce the LO frequency to a fraction of the RF frequency. This is advantageous for telecommunications where superheterodyne receivers are dominant. It has been reported that a lower LO frequency operation has a significantly lower power consumption [32] and a better phase-noise performance for high frequency applications [33, 34]. SHMs have also gained interests in direct conversion systems [33, 32, 35], which are usually designed for low-power biomedical applications. This is because that the LO-to-RF leakage and subsequent LO self-mixing in a SHM will not cause DC offsets, which is especially problematic in a direct receiver system.

Since no DC current flows through the switches in a passive mixer, a low flicker noise can be achieved in passive mixers. Moreover, the stacked LO stages used to
achieve subharmonic performance in active Gilbert Cell based mixers result in a low voltage headroom. Therefore, in this design, a passive SHM is chosen. Currently 2x SHMs are widely discussed and 4x SHMs are of increasing interests too [36]. Although in principle SHMs of other orders are achievable, for order greater than 4 cases the circuit design gets more complicated with larger multiphase voltage controlled oscillator (VCO) or larger polyphase filter required, which tend to have adverse effects on the noise performance and other parameters of the mixer. Besides, the power consumption and the silicon real estate will also be increased.

In this chapter, a broadband passive 2x SHM is designed with the goal of achieving both low noise figure and high linearity. Fabricated in IBM’s 0.13µm technology and driven by a 1.5 V DC voltage, the mixer is designed to be broadband with a constant IF output at 140 MHz.

3.2 Concept of the Subharmonic Mixer

Many designs have been proposed in realizing subharmonic mixing [33, 37, 36, 38]. Active subharmonic mixers are mainly derived from modifying the Gilbert Cell by simply adding another LO switching stage [36, 38], which results in a low voltage headroom and has a limited application in low voltage designs. This problem is avoided in passive mixers. The switching transistors in a passive mixer operate in deep triode region and therefore do not have voltage drop. Moreover, since no dc bias current is steered between the switching transistors in a passive mixer, superior flicker noise performance can be obtained. As discussed in Section 2.3, a passive mixing core can be driven by both voltage signals or current signals. In this design, the current-driven topology is implemented due to its high linearity [24].
3.2. CONCEPT OF THE SUBHARMONIC MIXER

The block diagram of the passive 2x SHM is shown in Figure 3.1. The single-ended RF signal is converted to a differential signal via an off-chip balun. Each branch of the differential input signal then passes through a bias tee before reaching the chip. The bias tee circuits provide a dc path for the on-chip input matching stage. Since the passive SHM is operated in current domain, a low-noise transconductor amplifier (LNTA) is used to convert the input voltage signal to a current signal. Then this current signal is down-converted by a passive 2x subharmonic mixing core to the IF frequency. Quadrature LO signal is required for this 2x subharmonic mixing, and is implemented with an off-chip quadrature coupler and two on-chip single-ended to differential active baluns (phase splitters). At the IF side, a differential transimpedance amplifier (TIA) is designed to act as a current buffer as well as to transfer the output current into a differential output IF voltage. Due to the concerns of linearity and power consumption, an off-chip buffer is used here to convert the differential output voltage to a single-ended signal. Detailed design and analysis of each building block are addressed in the following session.

Figure 3.1: Block diagram of the passive SHM.
3.3 Circuit Design

In this section, each part of the passive subharmonic mixer (PSHM), namely the passive subharmonic mixing core, LNTA with noise cancellation, inverter-based TIA and the on-chip LO phase splitter, is fully analysed with detailed design considerations illustrated. In depth noise analysis is provided with mathematical calculations. The measured results are provided at the end of the chapter.

3.3.1 Passive Subharmonic Mixer Core

The mixing core shown in Figure 3.2 as described in [33, 32, 39] is chosen as the starting point for the mixer design in this chapter. This topology is a typical modification.
to the popular Gilbert Cell mixer by adding another LO stage so that the RF signal is successively mixed with a two-stage quadrature LO signal. Transistors $M_{1I}-M_{4I}$ form the first stage, which is a regular double-balanced passive mixer, and transistors $M_{1Q}-M_{4Q}$ form the second stage to achieve the subharmonic mixing. Consider the following switching behaviour in one cycle of the quadrature LO signal. During the first quarter-cycle, transistors $M_{2I}, M_{3I}$ and $M_{2Q}, M_{3Q}$ are on, the RF signal is modulated to the IF port with one polarity. During the second quarter-cycle, transistors $M_{2I}, M_{3I}$ and $M_{1Q}, M_{4Q}$ are on, the RF signal modulated to the IF port has a reversed polarity. Therefore, in a complete LO cycle, the polarity of the IF signal is changed four times, which means that the input RF signal is modulated four times, at twice the LO signal frequency. This process can be better illustrated by deriving the circuit’s mixing function. For simplicity, $v_{LOI}$ is assumed to be a square wave $f_{SW}(t)$, which has a period of $T_{LO}$. Accordingly, $v_{LOQ}$ is the phase-shifted version of $v_{LOI}$ and can be modeled as $f_{SW}(t - \frac{T_{LO}}{4})$. The switching transistors can be viewed as ideal switches driven by LO signals, where the ON resistances of the transistors have been neglected. As shown in Figure 3.3, the output currents of the first stage can be expressed as

$$i_1(t) - i_2(t) = i_{RF}^+ f_{SW}(t) \quad (3.1)$$

$$i_4(t) - i_3(t) = i_{RF}^- f_{SW}(t). \quad (3.2)$$

Similarly, the output currents of the second stage are

$$i_5(t) - i_6(t) = [i_1(t) + i_3(t)] f_{SW}(t - \frac{T_{LO}}{4}) \quad (3.3)$$

$$i_8(t) - i_7(t) = [i_2(t) + i_4(t)] f_{SW}(t - \frac{T_{LO}}{4}). \quad (3.4)$$
Therefore, the ideal mixing function can be obtained as

\[ i_{IF}(t) = i_{IF}^+(t) - i_{IF}^-(t) \]
\[ = i_{RF}(t)f_{SW}(t)f_{SW}(t - \frac{T_{LO}}{4}) \]
\[ m(t) = \frac{i_{IF}(t)}{i_{RF}(t)} = f_{SW}(t)f_{SW}(t - \frac{T_{LO}}{4}), \] (3.6)

which is plotted in Figure 3.4. It can be easily seen that \( m(t) \) has a frequency twice of the LO frequency. According to the Fourier series, this mixing function can be represented by odd harmonics of \( 2\omega_{LO} \) [33] as

\[ m(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \cos(2n\omega_{LO}t), \quad n \text{ is ODD.} \] (3.7)

Assuming \( i_{RF}(t) = I_{RF} \cos(\omega_{RF}t) \), where \( I_{RF} \) and \( \omega_{RF} \) are the amplitude and the
angular velocity of the RF signal, \( i_{IF}(t) \) can be obtained as

\[
i_{IF}(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \cos(2n\omega_{LO}t) \cdot I_{RF} \cos(\omega_{RF}t)
\]

\[
= \frac{2}{\pi} I_{RF} \sum_{n=1}^{\infty} \frac{1}{n} \left[ \cos(\omega_{RF} - 2n\omega_{LO})t + \cos(\omega_{RF} + 2n\omega_{LO})t \right]; \quad n \text{ is ODD.}
\]

Since the required IF signal is \( \omega_{IF} = \omega_{RF} - 2\omega_{LO} \), in which case \( n = 1 \), therefore the corresponding ideal conversion loss can be readily calculated from Equation (3.8) as

\[
CL = \pi/2 \approx 3.9 \text{ dB}.
\]

The above discussion is based on the assumption that LO signal is an ideal square
wave, other types of LO such as zero-overlap sinusoidal, make-before-break (ON-overlap) and break-before-make (OFF-overlap) waves [13, 19], may also present at the gates of switching transistors. Despite that the corresponding mixing function and conversion gain of each LO drive derived in Reference [13] are for fundamental voltage-driven passive mixers, similar conclusions can be obtained for the PSHMs. It should be noted that, although the conversion gains for different LO drives are different, the mixing functions are always waves switching between +1 and −1, at twice LO’s frequency. This mixing character reveals that the two series switching stages are correlated, instead of being multiplied by two 90° phase shifted signals sequentially. Thus, the conversion loss of the PSHM is the same with the fundamental counterpart, which is π/2 for ideal case, rather than being the square of the conversion loss of the fundamental mixer, which is (π/2)². This has been verified mathematically in the above discussion (Equation (3.9)).

In mixer designs, switching transistor size, LO drive and switching duty cycle are three crucial parameters. The choices of those parameters are discussed below.

It is explained in [19] that the on resistance of the switching transistors should be small in order to reduce the current loss as well as to stabilize the voltage swing at the input port. It is also shown in [33] that high switch conductance is critical in achieving good noise and gain performance. From Equation (2.19), we can see that the conductance is proportional to the transistor size and therefore a larger transistor width should be chosen. However, large devices require large LO drive, and at high frequencies there is higher capacitive coupling to the substrate due to the parasitic capacitances which causes higher loss through substrate. As such, there is an optimum transistor width considering the conversion gain and noise performance. In this work,
a transistor width of 40 µm is chosen with the minimum transistor length of 130 nm.

Ideally, the switching transistors should be biased at the threshold voltage in order to be switched 50% duty cycle. However, in real circuits, the threshold voltage value is vague within a certain range, the LO dc voltage at the gates either yields OFF overlap and ON overlap. It is demonstrated in [19] that a current-driven passive mixer is better to operate in ON overlap in order to avoid large swings at the input, which is introduced by the momentarily off of all switches during the OFF overlap. Therefore, in this work, the LO dc bias at the gates of the switching transistors is chosen to be slightly above the transistors’ simulated threshold voltage so that ON overlap is obtained. Moreover, since high switch conductance is preferred, LO swing should be high. A 0 dBm LO drive is chosen in this design.

The switching duty cycle plays an important role too. It is reported in [40, 33] that conversion gain is susceptible to switching duty cycle errors due to the phase errors in the quadrature LO signals. Suppose there is a phase error $\Delta \theta$, the corresponding time delay is equal to $\Delta t = \Delta \theta (\frac{T}{\pi})$. The conversion gain is then modified to [33]

$$CG_{\Delta \theta} = \frac{2}{\pi} \cos^2(\theta).$$

(3.10)

Based on (3.10), it is reported in [33] that for a phase error within $+10^\circ$ and $-10^\circ$, a less than $\pm0.3$ dB conversion gain reduction is presented.

### 3.3.2 Broadband Noise-Cancelling Transconductor

Since this 2x PSHM works in current domain, a transconductor stage is required to transfer the input voltage signal to a current signal. Transconductance amplifiers are widely used for this purpose and various designs have been reported [41, 42, 43, 44].
The operational transconductance amplifier proposed in [42] is shown in Figure 3.5 (a). A feedforward-regulated cascode stage is implemented and a wide bandwidth of 12 GHz is achieved. Active inductor load is used to improve the linearity performance. However, the small transconductance presented in this topology results in a poor noise performance. In [41], a transconductor as shown in Figure 3.5 is implemented with transconductance boosting methods, which includes input cross-coupling, current reuse complementary input and back gate connection. The reported transconductance is boosted up to three times of the single CG input matching transistor.

In this design, a low-noise transconductance amplifier (LNTA) with noise cancellation is implemented, which is inspired by the common-gate common-source (CG-CS) LNA designs proposed in [43, 45, 46]. The CG-CS configuration is able to provide wideband matching as in the CG configurations. Moreover, doubled transconductance and noise cancellation can be achieved at the same time.
The circuit of the implemented LNTA is shown in Figure 3.6. Note that the dc biasing circuitry is not shown. CG transistors $M_1$ and $M_3$ are used as the input stage to provide broadband matching because the input impedance looking into the source of a transistor in saturation is approximately $1/g_m$. Then two CS transistors $M_2$ and $M_4$ are cross-connected to give a higher transconductance as well as to cancel the noise of the CG transistors. Since the input impedance of the CS transistors is the gate-to-source capacitance $C_{gs}$, which is large at low frequencies, the input impedance of the CG-CS structure is dominated by the CG transistors. The cross-connected outputs of the differential CG-CS pairs result in the summation of the signal currents at the output nodes. This mechanism is illustrated by the small signal model of the transconductor as shown in Figure 3.7, where the channel length modulation and body effect of the transistors are neglected for simplicity. It can be seen that the
output currents are

\[ i_o^+ = i_2 + i_3 = g_{m2}v_{in}^+ - g_{m3}v_{in}^- \] (3.11)

\[ i_o^- = i_1 + i_4 = -g_{m1}v_{in}^+ + g_{m4}v_{in}^- \]

and the transconductance can be readily calculated as

\[ G_m = \frac{i_o^+ - i_o^-}{v_{in}^+ - v_{in}^-} = \frac{(g_{m1} + g_{m2})v_{in}^+ - (g_{m3} + g_{m4})v_{in}^-}{v_{in}^+ - v_{in}^-} = g_{m,CG} + g_{m,CS}, \] (3.12)

where \( g_{m1} = g_{m3} = g_{m,CG} \) and \( g_{m2} = g_{m4} = g_{m,CS} \) are assumed. It shows that the transconductance of the CG-CS configuration is the sum of the CG and CS transconductance, and is therefore higher than the configurations which use only one CG transistor as the input stage. If the channel modulation and body effect need to be included, the effective input impedance and the transconductance can be derived

---

Figure 3.7: Model of the CG-CS transconductor.
3.3. CIRCUIT DESIGN

as

\[
Z_{\text{in,eff}} \approx \frac{r_{o1} + Z_L}{1 + (g_{m1} + g_{mb1})r_{o1}} \quad (3.13)
\]

\[
G_{m,\text{eff}} \approx \frac{1 + (g_{m1} + g_{mb1})r_{o1}}{r_{o1} + Z_L} + \frac{g_{m2}r_{o2}}{r_{o2} + +Z_L}, \quad (3.14)
\]

where \(r_{o1}\) and \(r_{o2}\) are due to the channel length modulation of \(M_1\) and \(M_2\). Since the body of \(M_2\) is grounded, only \(M_1\) has body effect and is represented by \(g_{mb1}\). \(Z_L\) is the load impedance, which is the parallel of the active load and the input impedance of the next stage.

Next, the noise cancellation property of the LNTA circuit is observed. It is implemented to cancel the high noise presented by the CG matching transistors. By simply cross-connecting the outputs of the CG-CS pair, noise cancellation is achieved in addition to the improved transconductance and no additional circuitry is required. To understand the mechanism, the transistor noise is modelled as a noise current source connected between the drain and the source (Section 2.4). Then the half-circuit of the LNTA is plotted in Figure 3.8 for conceptual noise analysis, where \(Z_S\) is the source impedance and \(i_{nd1}\) represents the total drain current noise of CG transistor \(M_1\).

Assuming \(i_{n1}\) is the total current flowing through the CG transistor \(M_1\), which can be expressed by \(i_{nd1}\) as

\[
i_{n1} = \frac{i_{nd1}}{1 + \frac{Z_L+Z_S}{r_{o1}} + (g_{m1} + g_{mb1})Z_S}. \quad (3.15)
\]

\(i_{n1}\) produces a noise voltage \(v_{nx}\) across the source resistance and it is equal to \(i_{n1}Z_S\). It also produces a noise voltage on the load \(Z_L\), which can be obtained as \(v_{ny} = i_{n1}Z_L\) at the output node \(v_o^+\). Note that \(v_{nx}\) and \(v_{ny}\) are 180° out of phase. The noise
voltage $v_{nx}$ is amplified by the CS stage, yielding a noise voltage $v_{nz} = -g_{m2}Z Lv_{nx}$ at the output node $v_o^-$. Due to the property of CS amplification, $v_{nz}$ is also $180^\circ$ out of phase with $v_{nx}$, thus, in phase with $v_{ny}$. With proper scaling of the related parameters, $v_{ny}$ and $v_{nz}$ can be cancelled out at the differential output because they present as common-mode signals.

$$v_o^+ - v_o^- = v_{ny} - v_{nz} = i_{n1}(1 - g_{m2}Z_s)Z_L$$  \hspace{1cm} (3.16)

From the above equation it can be concluded that the condition for full noise cancellation is $g_{m2} = 1/Z_s = g_{m1}$, in which case the overall transconductance $G_m$ of the CG-CS transconductor is twice of that of the CG transconductor.

A few points are summarized here for the above analysis. First, since $M_1$’s thermal noise, flicker noise and substrate noise can all be referred to the output of the transistor, they can all be cancelled [47]. Second, only the noise produced by the CG
structure is cancelled, the noise due to the active load and the CS transistor \( M_2 \) can not be cancelled by this configuration. Third, noise originated from the CG transistor can be cancelled because it becomes a common-mode signal at the differential output, while the differential input signal remains to be differential at the output nodes \( X \) and \( Y \) and will be added instead of being cancelled.

After achieving the overall idea of the noise cancelling mechanism of the CG-CS configuration, a more detailed noise analysis of the whole LNTA is given in the following content so that the noise figure can be derived mathematically and design guidelines can be provided. Note that in the following analysis, only thermal noise of the transistors and resistors are considered. Figure 3.9 shows models for all the noise origins in the circuit.
According to the definition of noise factor,

\[ F = \frac{SNR_{in}}{SNR_{out}} = 1 + \frac{|i_{n,\text{added}}|^2}{G_{m,eff}^2|v_{ns}|^2}, \tag{3.17} \]

where \( G_{m,eff} \) is the effective transconductance of the LNTA, \( i_{n,\text{added}} \) is the noise current generated in the circuit and \( v_{ns} \) is the noise voltage from the source.

Observing Figure 3.9, we can see that the added noise comes from the transconductance stage \( |i_{n,G_m}|^2 \) as well as the active load \( |i_{n,\text{actLoad}}|^2 \). Thus, the added noise can be written as

\[ |i_{n,\text{added}}|^2 = |i_{n,G_m}|^2 + |i_{n,\text{actLoad}}|^2, \tag{3.18} \]

where

\[
|i_{n,G_m}|^2 = |i_{n1}|^2(g_{m2}Z_s - 1)^2 + |i_{nd2}|^2 \tag{3.19}
\]
\[
= |i_{n1}|^2(g_{m2}Z_s - 1)^2 + 4kT \gamma_n g_{m2}
\]
\[
|i_{n,\text{actLoad}}|^2 = |i_{nd5}|^2 + |i_{n,R_0}|^2 = 4kT \gamma_p g_{m5} + \frac{4kT}{R_0}, \tag{3.20}
\]

where \( i_{nd2} = 4kT \gamma_n g_{m2} \), \( i_{nd5} = 4kT \gamma_p g_{m5} \) are the drain noise currents of \( M_2 \) and \( M_5 \) respectively (flicker noise not included) and \( i_{n,R_0} = 4kT/R_0 \) is the noise current of resistor \( R_0 \).

Since the source generally has a resistive output impedance \( Z_s = R_s \), the noise voltage at the input of the circuit is dominantly the thermal noise of \( R_s \) and it can be expressed as

\[ v_{ns} = \sqrt{4kT R_s} \frac{Z_{in,eff}}{R_s + Z_{in,eff}}. \tag{3.21} \]
Combining equations (3.18) to (3.21) and substituting into Equation (3.17), the noise factor of this LNTA can be obtained as

\[ F = 1 + \frac{|r_{in}|^2 (g_m R_s - 1)^2}{4kT R_s^{-1} (R_s \parallel Z_{in,eff})^2 G_{m,eff}^2} + \frac{r_n g_m + r_p g_m + R_0^{-1}}{R_s^{-1} (R_s \parallel Z_{in,eff})^2 G_{m,eff}^2}. \] (3.22)

The second term is the noise produced by the CG configuration, and it can be cancelled when \( g_m^2 = 1/R_s \) is satisfied. Also, assume the input impedance is designed to be broadband matching by making \( Z_{in,eff} = R_s \), Equation (3.22) can be further simplified as

\[ F = 1 + 4\frac{r_n g_m + r_p g_m + R_0^{-1}}{R_s G_{m,eff}^2} = 1 + 4\frac{r_n g_m + r_p g_m + R_0^{-1}}{R_s} \left[ \frac{1+(g_m b + g_m b_1) r_o}{Z_L + r_o} + \frac{g_m r_o}{Z_L + r_o} \right]^2. \] (3.23)

Although Equation (3.23) is only a first order approximation of the noise factor as the high frequency noise parameters are not included, it provides a guideline for designing the LNTA circuit. It can be seen that large \( R_0 \) and smaller \( g_m \) are preferred in order to lower their noise contribution. The body effect of \( M_1 \) is helpful in increasing the effective transconductance \( G_{m,eff} \) and reducing the noise factor.

### 3.3.3 Transimpedance Amplifier

It has been widely recognized that a current-driven passive mixer is preferably loaded by a low input impedance TIA, which reduces the voltage swing at the source and drain of the switching transistors and provides a good linearity. Two widely used TIA designs include the CG structure [48, 32] as shown in Figure 3.10 (a), and the operational amplifier (op-amp) with RC feedback [41, 24] as shown in Figure 3.10 (b).
Since the input impedance of the CG amplifier is $1/g_{m, CG}$, low load impedance can be obtained by making the CG transconductance large. The overall conversion gain of the mixer using CG TIA is derived as \[48\]

$$A_v = \frac{v_{IF}}{v_{RF}} \approx \frac{2}{\pi} G_m R_L, \quad (3.24)$$

where $G_m$ is the transconductance of the transconductance amplifier, $2/\pi$ is the ideal conversion loss through the passive mixing core, and $R_L$ is the load of the CG TIA.

The input impedance of the op-amp based TIA is \[44\]

$$Z_{in, TIA} = \frac{Z_f}{A_{op-amp} + 1}, \quad (3.25)$$

Where $A_{op-amp}$ is the open-loop voltage gain of the operational amplifier and $Z_f$ is
the impedance of the RC feedback network. Due to high voltage gain of the op-amp, this input impedance is very low, making it an excellent load for the passive mixer. The overall voltage gain of the mixer using op-amp based TIA is [44]

\[
\frac{v_{IF}}{v_{RF}} \approx \frac{2}{\pi} G_m Z_f. \tag{3.26}
\]

In this work, instead of using complicated multi-stage operational amplifier as proposed in [44, 24], a simple inverter with resistive feedback is implemented as the TIA for better linearity and lower power consumption. The TIA circuit is shown in Figure 3.11.

![Figure 3.11: Schematic of the implemented transimpedance amplifier.](image)

### 3.3.4 LO single-ended to Differential Phase Splitter and Buffer

In order to implement quadrature LO signals to the mixer core, an off-chip hybrid coupler first produces LO signals with 0° and 90° phase shifts. Then, two on-chip single-ended to differential active baluns generating LO signals with phases of 0°,
3.4 Measurement Results

The microphotograph of the fabricated chip is shown in Figure 3.13. It is fabricated with IBM’s CMOS 130 nm technology with 8 metal layers, which are 3 thin, 2 thick and 3 RF metal layers. For measuring purpose, three differential ports of the mixer, namely RF, LO and IF ports, are connected with GSGSG coplanar waveguide (CPW).
Figure 3.13: Microphotograph of the passive subharmonic mixer.

probes, which all have a pitch of 100 µm. The differential RF signal is generated with a passive balun and then the differential IF signal is loaded by an active buffer. The quadrature LO signal is generated by an off-chip 2-way 90 degree power splitter, which is model ZAPDQ-4 from Mini-Circuits and works from 2 GHz to 4.2 GHz. Then the quadrature LO signal is injected into the differential probe and further split into four signals with 90° phase shift by two single-ended to differential splitters on chip (Figure 3.12).

The DC supply voltage is 1.5 V while the gates' biasing voltages are slightly tuned first to achieve the optimum conversion gain and noise figure. Then the tuned voltages are kept the same throughout the following tests. The input LO power level is set to
compensate the loss through the cables and the quadrature power splitter so that the LO power that is injected into the LO port is approximately 0 dBm, same with the designed LO power level.

$S_{11}$ As indicated in Section 2.5.3, a full two port measurement is done with VNA. Then by substituting the obtained data into Equation (2.36), the differential input reflection coefficient is calculated and depicted in Figure 3.14. It can be seen that good input match is achieved. The $S_{11}$ curve rises gradually from -16.6 dB at 1 GHz to -11 dB at 10 GHz. Across the entire frequency range from 1 GHz to 10 GHz, $S_{11}$ is well below -10 dB.

**Conversion Gain** With the loss in the transmission line and passive balun compensated, the conversion gain is plotted in Figure 3.15. The output IF frequency was measured at 140 MHz. Note that the 3 dB voltage gain boost due to the balun is removed, so the reported value shown below is the differential voltage conversion gain of the on-chip mixing circuit. The RF frequency was swept from 4.5 GHz to 8.5 GHz.
with a step size of 0.25 GHz. It can be seen that across the whole frequency range, the conversion gain is relatively flat and stably decreases from 16 dB at frequency 4.5 GHz to 13 dB at frequency at 8.5 GHz. The measured upper 3 dB cut-off frequency is then 8.5 GHz. Therefore, a 3 dB bandwidth of about 4 GHz is concluded for this design.

**Double-Sideband Noise Figure**  Similarly, the RF frequency is varied from 4.5 GHz to 8.5 GHz with a step size of 0.25 GHz for the noise figure measurement. Since no suitable broadband tunable filter was available, double-sideband noise figure $NF_{DSB}$ was measured due to its simplicity and no need of adding 3 dB loss compensation.

In order to de-embedding the noise effect of the off-chip circuitry, the following steps are used. First, the noise figure and gain of the passive balun are measured as shown in Figure 2.21 (a). Then the passive balun is directly connected to the active buffer, and the noise figure of the balun-buffer cascade is measured. By using the
3.4. MEASUREMENT RESULTS

Friis’ cascade noise equation, the noise figure of the buffer can be calculated. Next, the noise figure of the balun-mixer-buffer cascade is measured. With the balun and buffer’s noise figures obtained from the previous steps and the conversion gain of the mixer known from the above conversion gain measurement, the noise figure of the mixer can be calculated by using the Friis’ noise equation again. The obtained result is shown Figure 3.16, which shows that the DSB NF maintains to be low through the entire measured frequency range, mostly well below 10 dB. The lowest value is 8 dB at frequency 7.75 GHz while the highest value is 10.5 at 7.25 GHz.

P1dB and IP3  P1dB and IP3 are two important parameters in characterizing circuits’ linearity. For P1dB measurements, a single tone in injected into the circuit and the output power at the IF frequency is measured versus the input signal power. For IP3 measurements, two RF tones separated by 1 MHz are injected and the output power at the IF frequency as well as the third order intermodulation frequency is measured. The P1dB and IP3 curves at 5 GHz are given in Figure 3.17 (a) and (b)
Figure 3.17: Measured P1dB and IP3 versus input power (a) P1dB measurement at 5 GHz and (b) IP3 measurement at 5 GHz.

respectively. The dashed lines shown in each figure are extracted based on the first few points. It is marked that at 5 GHz, the input referred P1dB and IP3 are -10.8 dBm and -3.7 dBm respectively.

Since this mixer is designed to be broadband, it is necessary to how know the P1dB and IP3 change with frequency. Thus, they are plotted in Figure 3.18 as a summary for the linearity performance versus frequency. It is shown that the both the IP1dB and IIP3 curves are relatively flat over the measured frequency range, which indicates
3.4. MEASUREMENT RESULTS

![Figure 3.18: Measured P1dB and IP3 versus input frequency.](image)

that the linearity doesn’t degrade as the operating frequency increases.

**Port Isolations** Port isolation is another important parameter for mixer evaluations. LO-to-IF, LO-to-RF as well as the RF-to-IF isolations are tested and the result is shown in Figure 3.19. Although for double-balanced mixers, the even LO harmonics are generally well rejected, 2LO-to-IF and 2LO-to-RF isolations are presented here for complexity because the designed circuit is a 2x subharmonic mixing circuit. Also due to its 2x subharmonic property, the LO frequency is measured over a range that is half of the measured RF frequency range (Figure 3.19 (a) and (b)), while the 2x LO frequency range is the same with the RF frequency range (Figure 3.19 (d)). It can be seen that the overall isolations between ports are high, with more than 50 dB isolations achieved between all the ports for most of the measured frequency.

**Power consumption** The complete circuit consumes a dc current of 29 mA from a 1.5 V voltage source. Therefore, the power consumption is 43.5 mW. Note
3.4. MEASUREMENT RESULTS

![Graphs showing measurement results for different frequency bands and isolation levels.](image)

Figure 3.19: Measured port isolations (a) LO-to-IF isolation and (b) LO-to-RF isolation and (c) RF-to-IF isolation and (d) 2LO-to-RF and 2LO-to-IF isolation.

that the passive mixing core doesn’t consume any dc current, while the LNTA and TIA consumes a total dc current of approximately 17 mA. The remaining 12 mA current consumption is due to the on-chip quadrature LO generation circuits, namely the two LO active baluns and the LO buffers.

The mixer is also very compact and the area consumed excluding the pads is only 0.7mm x 0.7mm.
Table 3.1: Comparison with recent subharmonic mixers.

Table 3.1 summarizes the performance of this work and gives a comparison with the recently published subharmonic mixers.

It can be seen from the table that compare to the other recently reported works, the proposed PSHM achieves a wide bandwidth of 4 GHz instead of a narrow working frequency range. Moreover, the noise figure of this PSHM is competitively low through the whole frequency band. The lowest DSB noise figure is 8 dB and the average noise figure is approximately 9 dB. Besides, the proposed mixer also has a comparable conversion gain of more than 13 dB through the whole frequency range while maintaining an excellent linearity. The chip is compact with a core size of 0.49 mm².

### 3.5 Conclusion

A broadband low-noise passive subharmonic mixer was designed in CMOS 130 nm technology. The noise-cancelling LNTA provides broadband matching along with improved transconductance. The current-driven passive mixing core is loaded by the
3.5. CONCLUSION

small input impedance of the transimpedance amplifier, which allows a highly linear performance. Measured results show that the mixer is well matched over the entire frequency band with an $S_{11}$ well below -10 dB. A high conversion gain of 16 dB and a 3-dB frequency range from 4.5 GHz to 8.5 GHz are obtained. Excellent noise and linearity performance are achieved. In particular, the average DSB NF, IP1dB and IIP3 are approximately 9 dB, -4 dBm and -12 dBm respectively. The mixer also exhibits excellent port isolations and a compact size of 0.49 mm$^2$ excluding the pads. It consumes a total current of 29 mA from a 1.5 V voltage supply.
Chapter 4

Broadband Low-Noise Variable Gain Mixer

4.1 Introduction

Nowadays, development of modern communications has been posing higher demands on the performance, multi-functionality, size and cost of electronic devices. This could mean lower noise, broader bandwidth, variable gain, higher linearity and so on. Since the received signals usually present different amplitudes due to the various transmission conditions, gain variability is critical because it enables a system to adjust the received signal level. In other words, it increases the system’s dynamic range and maintains a reasonable output signal level for later processes.

Active mixers have conversion gain instead of conversion loss, which is the case of passive mixers, like the one discussed in the previous chapter. This is important because as one of the first stages of a receiving front end, conversion gain can suppress the noise of the following stages. Therefore, an active mixer topology is chosen in
4.2. VARIABLE GAIN MIXING CIRCUIT CONCEPT

this chapter. The transconductance stage with noise cancelling and current bleeding techniques used in this work is based on the research of [50], which has a superior low noise reported. Then variable gain controllability is utilised to increase the multifunctionality of the proposed designs while maintaining compact chip sizes. Instead of realizing the gain variability at the transconductance stage of the mixer [51] or stages preceding the mixer such as (operational transconductance amplifier) OTA [43] and LNA [52], two IF variable gain stages are implemented to provide gain control. This is advantageous because the noises of the later stages are scaled down by the gains of the previous stages. Therefore, by designing the transconductance stage with a fixed high conversion gain, the noise effects from the IF variable gain stage can be minimized. Thus, the overall noise of the variable conversion gain (VCG) mixers can be low.

In this chapter, two variable conversion gain mixers are designed and fabricated with CMOS 130 nm technology. Both of them operate from 1 GHz to 6 GHz, and have the same IF output frequency of 140 MHz. Low noise figure and more than 10 dB gain varying range are achieved.

4.2 Variable Gain Mixing Circuit Concept

Variable gain control, in general, is important in modern communications due to its capability of maximizing the overall system dynamic range and controlling the output signal level. It can be realized with either digital or analog methods. The digital methods generally employ arrays of resistors or capacitors, and yield discrete gain steps controlled by digital signals [53, 54, 55]. On the other hand, the analog methods provide continuous gain variations controlled by analog gain control signals.
4.3. CIRCUIT IMPLEMENTATION

Conventionally, this is performed by variable gain amplifiers (VGA). Recently, several designs that integrate VGAs with mixers, often referred to as VGMs, have been reported [43, 56, 57, 51, 58, 59]. Despite the advantage of combining the mixers and the VGAs into one entity, VGMs implemented with variable transconductors usually demonstrate high noise figures, especially at the low gain modes. In [51], for 3 different modes which present a maximum conversion gain of 24 dB and a minimum conversion gain of 9 dB, the DSB NF are reported as 8 dB, 16 dB and 23 dB respectively. In [57], a minimum 18.8 DSB NF dB is reported. Therefore, it is favourable to fix the transconductance while achieve gain control in IF domain.

In this chapter, two VCG mixing circuits are proposed. They have the same transconductor stage and active Gilbert switching core, therefore they present certain similarities in terms of broadband matching and port isolations. Same with the previous chapter, an off-chip passive balun is used to split the single-ended input signal into a differential one, while an off-chip highly linear buffer is used to provide a high output load as well as to convert the differential output voltage signal to a single-ended voltage signal. The block diagram of the two proposed VCG mixers is shown in Figure 4.1.

4.3 Circuit Implementation

In this section, the broadband, noise-cancelling transconductance stage is illustrated, including the current-bleeding and series inductive peaking techniques. It is based on the design of [50] due to its capability of providing wideband matching and superior noise performance. Then the two IF variable gain control designs are addressed, namely the current-summing variable gain stage and the $R - r$ variable gain topology.
Figure 4.1: Block diagram of the broadband low-noise variable-gain mixer.

The measured results of these two VCG mixers are presented at the end of the chapter.

### 4.3.1 Broadband Low-Noise Mixer

**Broadband Transconductor with Noise-Cancellation** A CG configuration is used as the input matching stage, as in the broadband LNTA presented in last chapter. This method is simple, since the impedance looking into the source is approximately $1/g_m$ and by properly scaling the CG transistor, a broadband input matching can be easily realized. However, the drawback is that the CG configuration exhibits high
noise. As such, noise cancellation is needed to cancel the noise generated by the CG stage. In Chapter 3, the cross-connected CG-CS structure cancels the noise of the CG transistor because it yields a common-mode signal at the differential output, which gets cancelled out. The noise cancelling mechanism is different in this design, where two CS transistors are connected as shown in Figure 4.2 (a) and noise cancellation is achieved at the output node of the transconductance in current domain.

Assume the total noise current flowing through the CG structure is \( i_{n1} \). The noise cancelling mechanism is illustrated in Figure 4.2(b). Two nodes are defined as X node and Y node in the figure. It can be seen that the noise voltages \( v_{nx} \) and \( v_{ny} \), which are the voltages produced by the noise current across the source impedance \( R_s \) and \( M_1 \)'s load resistance \( R_1 \), are 180° out of phase. Therefore, as those two noise voltage appear at the input of the CS transistors, the noise current \( i_{n,\text{out}} \) at the output node is

\[
i_{n,\text{out}} = g_{m3}v_{nx} - g_{m2}v_{ny} = (g_{m3}R_s - g_{m2}R_1)i_{n1}. \quad (4.1)
\]
It can be easily seen that the condition for fully noise cancellation is

\[ g_3 = \frac{R_1}{R_s} g_2. \] (4.2)

Similar to the LNTA in last chapter, only the CG noise is cancelled, the noises from \( R_1, M_2 \) and \( M_3 \), cannot be cancelled. However since CG stage is the most noisy part, a superior transconductor noise can be achieved. Moreover, as the broadband matching task is fulfilled by the CG transistor, the noise cancelling CS transistors \( M_2 \) and \( M_3 \) can be designed to provide high transconductance to suppress the noise of later stages. This is different from the LNTA presented in last chapter, where in order to obtain noise cancellation, the CS transistor’s transconductance needs to be equal to \( 1/Z_s \). Although in this topology, it seems that \( M_2 \) and \( M_3 \) can be designed arbitrarily large, the transistor size of \( M_3 \) is restricted as the large capacitance \( C_{gs} \) of \( M_3 \) can ruin the broadband matching scheme.

With the condition of perfect noise cancellation obtained as expressed in Equation (4.2), and \( R_s \) being a fixed value, there are three possible design options available:

1. \( g_{m2} = g_{m3}, \ R_1 = R_s \).
2. \( g_{m2} = ng_{m3}, \ R_1 = \frac{1}{n} R_s \).
3. \( g_{m3} = ng_{m2}, \ R_1 = nR_s \).

Studies that have been done in [45] show that the optimal design is option (3), which gives the lowest noise and provides a high conversion gain.

A detailed noise analysis is given mathematically in [7], and only key results are summarized here. Including the channel modulation and body effect of \( M_1 \), the input
impedance and effective transconductance of the transconductor are \[7\]

\[ Z_{in} \approx \frac{r_{o1} + R_1}{1 + (g_{m1} + g_{mb1})r_{o1}} \] (4.3)

\[ g_{m_{eff}} = g_{m3} + g_{m2} \left[ \frac{1 + (g_{m1} + g_{mb1})r_{o1}}{1 + \frac{r_{o1}}{R_1}} \right] \] (4.4)

The noise figure of the transconductance stage is derived as [7]

\[ F = \frac{SNR_{in}}{SNR_{out}} = 1 + \frac{|i_{n, out\,trans}|^2}{|i_{n, out\,in}|^2} \] (4.5)

\[ = 1 + \frac{|i_{n, in}|^2(g_{m3}R_s - g_{m2}R_1)^2 + 4kT\gamma(g_{m2} + g_{m3}) + 4kTR_1g_{m2}^2}{4kTR_s^{-1}(R_s \parallel Z_{in})^2} \left\{ g_{m3} + g_{m2} \left[ \frac{1+(g_{m1}+g_{mb1})r_{o1}}{1+\frac{r_{o1}}{R_1}} \right] \right\}^2 \]

Assuming that perfect noise cancellation and input matching are achieved, namely \( g_{m3} = \frac{R_1}{R_s}g_{m2} \) and \( Z_{in} = R_s \), and neglecting the body effect and channel length modulation of transistor \( M_1 \), which gives \( Z'_{in} = 1/g_{m1} \) and \( g'_{m_{eff}} = g_{m3} + g_{m2}g_{m1}R_1 \), Equation (4.6) reduces to

\[ F = 1 + \frac{\gamma g_{m3}}{g_{m3}(1 + \frac{R_s}{R_1})} + \frac{R_s^2}{R_1^2}g_{m3}^2 = 1 + \frac{\gamma}{g_{m3}R_s} \left( 1 + \frac{R_s}{R_1} \right) + \frac{R_s}{R_1} \] (4.6)

Several design considerations can be obtained by analysing the above equations. Equation (4.6) indicates that large \( R_1 \) and \( g_{m3} \) are preferred. However, as shown in Equation (4.3), \( R_1 \) has an effect on input matching and cannot be too big. For the same reason, although larger \( g_{m3} \) yields low noise figure, transistor \( M_3 \) cannot be too large because its capacitances \( C_{gs} \) and \( C_{gd} \) can ruin the broadband matching. On the other hand, the body effect of \( M_1 \) is favourable, because it allows bigger \( R_1 \) to be
used while retaining a good input matching capability. It also yields a higher $g_{m_{eff}}$, which is helpful in achieving a higher conversion gain and reducing the noise.

**Current Bleeding** Although the noise cancelling transconductor provides a high transconductance and a low noise, it also requires a large dc bias current. However, due to the voltage headroom limitation, large dc current reduces the load size and thus reduces the voltage conversion gain of the mixer. Moreover, since the dc bias current of a transistor in saturation is proportional to the square of its overdrive voltage, it requires a large LO swing for the switching transistors, which leads to a less ideal switching behaviour. As such, a current bleeding structure is used to reduce the dc current flowing through the switching transistors. In this case, PMOS current bleeding circuit is used rather than its NMOS counterpart in order to mitigates the loading effect introduced by the bleeding circuit [7]. The schematic of the current bleeding circuit is shown in Figure 4.3. It consists of two PMOS transistors in CS configuration and their drains are connected to the transconductor in parallel. Due to the high output impedance at the drains of the PMOS bleeding transistors, the signal current flows into the switching pairs, as the input impedance looking into the source of the switching transistors is small, which has a value of approximately $Z_{in,\text{switch}} = 1/g_{m,\text{switch}}$. Therefore, only a small lose due to this current bleeding structure. Due to the parasitic tail capacitance, which is a combination of the $C_{gs}$ of the switches, the output capacitances of the transconductor as well as the bleeding circuit, aggressive bleeding may significantly degrade the gain and needs to be avoided. For optimal noise performance, each transconductor is designed to consume a dc current of about 12 mA, in which case the bleeding circuit is required to take 80% of the dc current so that a high conversion gain of above 15 dB can be achieved [7].
Figure 4.3: Schematic of current bleeding, inductive peaking and switching core.

**Series Inductive Peaking** Inductive peaking is a widely used technique in extending the bandwidth and obtaining a maximally flat frequency response. In this design, series inductive peaking is adopted as shown in Figure 4.3 and the simplified circuit model is shown in Figure 4.4 [7].

It is assumed that for each switching pair, only one transistor is on at a time, and the signal current is switched to the output load $R_{load}$ with no loss. The transconductor preceding the mixing core is modelled as a voltage-controlled current source and the output parasitic capacitances of the transconductor as well as the current bleeding circuit are collectively represented by $C_{out}$. A step response can be used to
provide an intuitive explanation to the basic theory of inductive peaking. Without
the peaking inductors, the circuit presents a rise time of about $2.2RC$, where the rise
time is defined as the elapsed time between 10% and 90% of the final output voltage
value. After adding the peaking inductors, a high impedance is presented by the
inductors at the time when the step change is presented. This high impedance forces
all the current to go charging the capacitor and decouples the load resistor, in which
case, the rise time is decreased and therefore the bandwidth is expanded [60]. The
peaking inductors are placed between the bleeding circuit and the switching core, so
that effect of inductive peaking can be maximized.

4.3.2 Current Summing IF Variable Gain Stage

After down-converting the signal to the IF frequency, a variable gain stage is im-
plemented as shown in Figure 4.1. The current summing technique is used here to
achieve the gain variability due to its superiorities regarding with low-noise and low
distortion [61]. The circuit schematic is shown in Figure 4.5. By changing the con-
trol voltage $V_{ctrl}$, the current distribution is varied and the current flowing through
the load is increased or reduced, therefore the continuous voltage gain tunability is
obtained. This mechanism is illustrated by Figure 4.6 and analysed in the following content.

Suppose all the transistors work in saturation region with their body terminals grounded, namely there is no body effect, and the channel modulation effect can be neglected. Since the load resistance \( R_L \) is relatively small, the input impedances looking into the sources of the CG transistors \( M_1 \) and \( M_2 \) are approximately

\[
R_1 = \frac{1}{g_{m1}} = \frac{1}{\mu_n C_{ox} \frac{W_1}{L_1}(V_{ref} - V_S - V_{TH1})}
\]

\[
R_2 = \frac{1}{g_{m2}} = \frac{1}{\mu_n C_{ox} \frac{W_2}{L_2}(V_{ctrl} - V_S - V_{TH2})},
\]

where \( \mu_n \) is the charge carrier mobility in NFET, \( C_{ox} \) is the gate oxide capacitance.
per unit area, $V_{\text{ref}}$ is the reference voltage at the gate of the load branch, $V_{\text{ctrl}}$ is the control voltage at the gate of the current summing transistor. $W_1$, $L_1$, $V_{T1}$ and $W_2$, $L_2$, $V_{T2}$ are the widths, lengths, threshold voltages of $M_1$ and $M_2$ respectively.

Therefore, the input small-signal current $i_{\text{IF}}^+$ distributes on the two branches and the current gain of the structure in Figure 4.6 is

$$\frac{i_1}{i_{\text{IF}}^+} = \frac{g_{m1}}{g_{m1} + g_{m2}} = \frac{1}{1 + \frac{W_2(V_{\text{ctrl}} - V_S - V_{T2})}{W_1(V_{\text{ref}} - V_S - V_{T1})}},$$

where $L_1 = L_2$ is assumed.

As a result, the overall voltage gain of the current summing variable gain IF stage is

$$A_{v,\text{IF}} = g_m R_L \frac{1}{1 + \frac{W_2(V_{\text{ctrl}} - V_S - V_{T2})}{W_1(V_{\text{ref}} - V_S - V_{T1})}} = g_m R_L \frac{k}{1 + \alpha V_{\text{ctrl}}},$$

where $g_m = g_{m0} = g_{m5}$ is the transconductance of $M_0$ and $M_5$. $k$ and $\alpha$ are constants.
and they are expressed as

\[
k = \frac{1}{1 - \frac{W_2}{W_1} \frac{V_{S} + V_{TH2}}{V_{ref} - V_{S} - V_{TH1}}}.
\]

(4.11)

\[
\alpha = \frac{W_2}{W_1(V_{ref} - V_{S} - V_{TH1}) - W_2(V_{S} + V_{TH2}).}
\]

(4.12)

It can be seen in (4.10) that when \( V_{ctrl} \) is high, the voltage gain is low, whereas when \( V_{ctrl} \) is decreased, the voltage gain is increased correspondingly. By properly scaling the parameters such as \( W_1, W_2 \) and \( V_{ref} \), the gain control range can be well adjusted.

### 4.3.3 Linear-in-dB Variable Gain using \( R - r \) Attenuator

Linear-in-dB characteristic is preferred in automatic gain control (AGC) systems, which are widely utilised in modern communication systems to detect the variance of the signal amplitude and to provide a relatively constant output signal level. The linear-in-dB VGAs are commonly adopted in AGC systems due to their wide dynamic ranges and the ability to maintain a uniform loop transient response and a constant AGC loop settling time for different input signal levels [62, 63].

MOS devices have a square or linear characteristic. This is seen from the long channel devices equations that the drain current \( I_D \) is expressed as

\[
I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2
\]

in saturation region and

\[
I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2]
\]

in triode region. Thus, it is challenging to realize the exponential function needed for a linear-in-dB VCG mixer. Although a MOS transistor operating in sub-threshold region has logarithmic characteristics [64], it is not preferred due to its high noise, poor linearity, limited bandwidth and instability to temperature variance [64]. On the other hand,
although parasitic bipolar transistors present exponential relationship between their collector currents and base-to-emitter voltages, and are used for linear-in-dB realizations, they suffer from temperature instability and require complicated temperature compensation circuitry. Due to the above reasons, various methods of implementing FETs to realize the linear-in-dB gain controllability have been proposed. A brief summary of some recent works on linear-in-dB gain control schemes is provided in the following content.

The circuit shown in Figure 4.7 (a) is often used to obtain the pseudoexponential functions, which are widely adopted in realizing the linear-in-dB gain tunability [65, 58]. It is a differential pair driven by a variable tail current and loaded by a diode-connected pair, which is also biased by a variable tail current. Since the transconductance of the input transistors and the diode-connected load transistors can be expressed as $G_{m1,2} = k\sqrt{1 + x}$, $G_{m3,4} = k\sqrt{1 - x}$ respectively, where $k$ is a constant and $x$ is the control parameter, the gain of this configuration is obtained as $Gain = \sqrt{(1 + x)/(1 - x)}$. The gain variability is realized by varying the bias currents $I_a$ and $I_b$. For $|x < 0.7|$, a control range from $-15$ dB to $+15$ can be obtained. Aside from this most commonly used equation $(1 + x)/(1 - x)$, other functions such as $\sqrt{(1 + x)/(1 - x)}$, and $1 + (1 + \alpha x)^2$ are also used in approximating the exponential function $e^x$.

Signal summing technique used in last section can also be adapted to generate linear-in-dB performance by making the control signal $V_{ctrl}$ a linear-in-dB function of the input signal [66, 67, 68]. Various circuits have been designed to obtain this function and most of them adopt the exponential characteristic of the bipolar transistor. As such, additional temperature stabilization circuitry is needed, which is often
Figure 4.7: Recent commonly used linear-in-dB VGA topologies (a) differential amplifier with diode-connected loads and (b) current-steering variable gain amplifier and (c) differential cascode variable gain amplifier and (d) differential amplifier loaded with $R - r$ attenuator.
4.3. CIRCUIT IMPLEMENTATION

sensitive to temperature and process itself. MOSFET has been explored to obtain the exponential performance, but the resulting gain accuracy, noise and high-frequency performances were not as good comparing its bipolar equivalent circuit.

Figure 4.7 (c) shows a VGA that uses a differential cascode amplifier [69]. The idea is to tune the control voltage $V_{ctrl}$ at the cascode transistors’ gates and change the input transistors’ operation region from saturation to triode, so that the transconductance of the transistors can be adjusted. This technique has low distortion and yields a large bandwidth. Moreover, with the implementation of the constant tail current source, a good high frequency performance can be maintained. Nevertheless, this structure suffers from a limited voltage headroom and voltage swing if resistive loads are used. As such, active loads are usually adopted in low supply voltage applications instead. The linear-in-dB character requires extra complicated circuitry to generate.

Figure 4.7 (d) shows another topology with linear-in-dB performance. The quasi-exponential character is realized by a simple $R - r$ attenuation network, which is composed of a constant resistance $R$ and a variable resistance $r$. The variable resistance $r$ is realized using transistors in triode region [70, 71, 72]. By turning the transistors on successively, the quasi-exponential curve can be extended, which is because of the overlap of the transistor conductances [71, 72]. Due to its simplicity, temperature invariance, low power consumption and superior performance on high frequencies, this architecture is adopted in this chip as the IF variable gain stage and more design details are going to be demonstrated in the following text.

The $R - r$ attenuation load network depicted in Figure 4.8. The linear-in-dB gain variation is obtained by successively turning on/off transistors $M_1$ to $M_n$ in triode
region and gradually changing their conductances by varying the control voltages $V_{ctrl1}$ to $V_{ctrln}$. PMOS transistors are used as the triode region loads so that negative gate voltages can be used to achieve a larger gain range. Larger $|V_{gs}|$ is preferred which ensures the PMOS transistors work in the triode region when large output voltage swing is presented, thus yielding a better linearity. Furthermore, PMOS devices have superior low flicker noise character over NMOS devices due to the buried channel behaviour [27]. Also, since the signal is downconverted to the IF frequency, the fast speed requirements of MOS devices is relieved, in which case PMOS devices can be used without deteriorating the circuit performance.

It can be seen that this load network consists of fixed resistors ($R_{load}$), and the transistors cross connected between the differential output ($M_1$ to $M_n$). Assuming
that only one cross-connected PMOS transistor, $M_1$, is turned on. The triode transistor then presents a resistance of

$$r_{DS1} = \frac{1}{k'_p(W_p/L_p)(|V_{ctrl1} - V_O| - V_{THp})},$$

(4.13)

where $V_O$ is the dc voltage at the source of $M_1$ and $k'_p$, $W_p$, $L_p$, $V_{THp}$ are the device parameter, width, length and the threshold voltage of the PMOS transistors respectively. The equivalent resistance of this $R - r$ load network is derived as

$$R_L = R_{load} \parallel r_{DS1} = R_{load} \frac{1}{1 + 2R_{load}k'_pW_pL_p(|V_{ctrl1} - V_O| - V_{THp})},$$

(4.14)

According to the approximation that for small $x$ values, $1/(1 + x) \approx e^{-x}$, it can be seen in (4.14) that exponential characteristic exist between the control voltage and $R_L$ and thus the voltage gain. It’s reported in [71] that the curve presents an approximate exponential gain range of 6 to 7 dB with less than $\pm 0.5$ dB gain error. According to this mechanism, more transistors can be turned on additively in order to extend the quasi-exponential curve. In addition, it has been shown in [71] that with more FETs turned on, the piece-wise exponential curve becomes wider due to the overlap conductance of the previously turned on transistors. This mechanism is illustrated in Figure 4.9, with $V_{ctrl}$ being the control voltage of $M_1$, namely $V_{ctrl1}$, while the control voltage of $M_2$ is shifted from $V_{ctrl1}$ by a constant value, so that it can be turned on additively to extend the exponential curve. With the same idea, the control voltage $V_{ctrl3}$ of transistor $M_3$ is shifted by a constant value from $V_{ctrl2}$ and so on.
4.3. CIRCUIT IMPLEMENTATION

Figure 4.9: Extending the quasi-exponential gain by turning on the transistors additively.

The variable gain IF circuit with $R-r$ attenuator implemented in this VCG mixer design is depicted in Figure 4.10. Transistors $M_1$ and $M_2$ form the input pair while $M_3$ and $M_4$ consist the cascade stage in order to shield the drain voltages of the input stage from the voltage variations at the output nodes due to $R-r$ attenuation, so that the input stage works under a stabler state and thus the linearity is improved. Although the fixed resistors $R_{load}$ are used because they are free of distortions, they also present large voltage drops. Therefore, current sources $M_5$ and $M_6$ are implemented to take part of the dc current and reduce the voltage drops. In this work, a 10 dB gain control range is obtained by only two cross-connected PMOS triode transistors. The measured results are given in the next section.
4.4 Measurement Results

In this section, measurement results of the two VCG mixers are given separately. A table is given at the end of this section, which summarizes the performance of the proposed two designs and provides a comparison with several recently reported VCG mixers.

4.4.1 Current-Steering Variable Conversion Gain Mixer

The microphotograph of the fabricated chip is shown in Figure 4.11. It is fabricated with IBM’s CMOS 0.13 \( \mu \text{m} \) technology. The measurement setup is similar to the
Figure 4.11: Microphotograph of the broadband low-noise variable gain mixer.

PSHM, with differential ports RF, LO and IF connected to the CPW probes. The differential RF and LO signals are generated by two passive baluns and the differential IF output is injected into the off-chip active buffer. The chip is driven by a 1.5 V dc supply voltage and the gates voltages are slightly tuned first to get the optimum conversion gain and noise performance. In order to obtain the designed input LO power level, which is 0 dBm, the loss through the cables and the non-ideal LO balun is compensated for all the measurements. The obtained results are given as the following.

$S_{11}$ A full two port measurement is done with VNA to obtain the differential input reflection coefficient $S_{11}$, which is calculated according to (2.36) and is plotted
in Figure 4.12.

It can be seen that the input port is well matched and the $S_{11}$ is maintained below -10 dB through the whole frequency range from 1 GHz to 10 GHz. The lowest $S_{11}$ is measured as -21.5 dB at 4.5 GHz while the highest value -10 dB is measured at 10 GHz.

**Conversion Gain** Due to the wideband and variable gain properties, the conversion gain is measured versus both the input frequency and the control voltage. After compensating the loss of the off-chip circuitry and removing the 3 dB voltage gain from the RF balun, the obtained differential voltage conversion gain of the on-chip circuit is plotted in Figure 4.13 (a) and (b). In Figure 4.13 (a), conversion gain curves correspond to different gain control voltages $V_{ctrl}$ are plotted while the RF frequency is swept from 1 GHz to 6 GHz with a step size of 0.5 GHz. It can be seen that all the curves present the same trend across the measured frequency range. The conversion gain curves are almost flat from 1 GHz to 2.5 GHz and decrease gradually. The 3 dB cut-off frequency is the same for different gain modes, which is measured to be 6 GHz.
Figure 4.13: Measured differential voltage conversion gain (a) versus RF frequency and (b) versus control voltage.

Hence, a bandwidth of 5 GHz is observed. In Figure 4.13 (b), the conversion gain of each input frequency is plotted versus the control voltage. Similarly, the curves exhibit the same shape and a gain control range of approximately 13 dB is obtained for all the input frequencies as the control voltage varies from 0.7 V to 1.25 V.

**Double-sideband Noise Figure** The DSB NF is also measured versus the input frequency and the control voltage for a comprehensive evaluation. The off-chip
4.4. MEASUREMENT RESULTS

circuitry noise contribution is exempted, and the final $NF_{DSB}$ is illustrated in Figure 4.14. In Figure 4.14 (a), the NF is relatively flat over the frequency range, with about 3 dB increment from 1 GHz to 6 GHz. For the highest gain setting ($V_{ctrl} = 0.7$ V), an excellent NF from 3.8 dB to 5.8 dB is observed. Figure 4.14 (b) shows that the NF increases relatively fast as the conversion gain drops. The highest DSB NF presented is 14.3 dB at 6 GHz and $V_{ctrl} = 1.25$ V.

Figure 4.14: Measured DSB NF (a) versus RF frequency and (b) versus control voltage.
4.4. MEASUREMENT RESULTS

Figure 4.15: Measured P1dB and IP3 at 5 GHz and $V_{ctrl} = 0.7$ V (a) P1dB curve and (b) IP3 curve.

**P1dB and IP3** Figure 4.15 shows the P1dB and IP3 curves at 5 GHz and $V_{ctrl} = 0.7$ V (highest gain). It can be readily read from the figure that the input-referred P1dB and IP3 are -16.3 dBm and -7.9 dBm respectively. The corresponding output-referred P1dB and IP3 are 8.5 dBm and 17.2 dBm.

As a broadband and variable gain mixer, it would also be of interests to see the P1dB and IP3 variations in response to the input frequency as well as the conversion
4.4. MEASUREMENT RESULTS

Figure 4.16: Measured input referred P1dB and IP3 versus: (a) input frequency and (b) control voltage.

gain, which are given in Figure 4.16 (a) and (b) correspondingly.

It can be observed in Figure 4.16 (a) that the both the IP1dB and IIP3 curves are relatively flat, which means that a good linearity is achieved over the frequency range of interest. The average IP1dB is approximately -17 dB while the average IIP3 is around -8 dB. On the other hand, as the control voltage changes, the IP1dB and IIP3 curves present reasonable fluctuations. The minimum IP1dB is -17.7 dB and
4.4. MEASUREMENT RESULTS

Figure 4.17: Measured port isolations (a) LO-to-RF and LO-to-IF isolation and (b) RF-to-IF isolation.

the minimum IIP3 is -9 dB at 0.8 V. The peak IP1dB value is about -3 dB at 1 V, whereas the peak IIP3 is -12.7 dB at 1.1 V (Figure 4.16 (b)). It should be noted that either in Figure 4.16 (a) or (b), the IP1dB and IIP3 curves exhibit similar trends.

Port Isolations  Isolations between ports are also tested. LO-to-RF, LO-to-IF isolations are given in Figure 4.17 (a) and the RF-to-IF isolation is shown in Figure 4.17 (b). It is obvious that good LO-to-IF and RF-to-IF isolations are obtained, with more than 50 dB isolation presented over most frequencies. On the other hand, the LO-to-RF isolation decreases from 50 dB at 1 GHz to 30 dB at 6 GHz. This is because that at higher frequencies, the parasitic capacitances of the transconductor become more prominent due to the Miller effect, especially the large noise-cancelling CS transistors. Besides, the gate-source capacitances of the switching transistors also contribute to the degradation of the LO-to-RF isolation. However, more than 30 dB isolation is still obtained through the entire frequency range.

Power consumption  The complete circuit consumes a total dc current of 30
4.4. MEASUREMENT RESULTS

Figure 4.18: Microphotograph of the broadband low-noise mixer with linear-in-dB gain variation.

mA from a 1.5 V voltage source and a core area of 0.66 x 0.66 mm$^2$ excluding the pads.

4.4.2 Variable Conversion Gain Mixer with $R - r$ Attenuator

Figure 4.18 shows the microphotograph of the fabricated chip, which is again fabricated with IBM’s CMOS 130 nm technology. The measurement setup is the same with the that of the last VCG mixer and the output IF frequency is also 140 MHz.

$S_{11}$ The differential input reflection coefficient $S_{11}$ is plotted in Figure 4.19. Due to the same configuration of the input transconductanor, this variable gain mixer has a similar input reflection coefficient. The optimum input match is achieved at 4.4
4.4. MEASUREMENT RESULTS

GHz with a $S_{11}$ of -20.4 dB.

**Conversion Gain** The differential voltage conversion gain of the on-chip circuit is plotted both versus the input frequency (Figure 4.20 (a)) and versus the control voltage (Figure 4.20 (b)). Here, the control voltage refers to $V_{ctrl1}$, while $V_{ctrl2}$ is equal to $V_{ctrl1} - 0.5V$.

As shown in Figure 4.20 (a), the conversion gain curves at different control voltages present similar frequency response. From 1 GHz to 2.5 GHz, the curves remain flat. The 3-dB cut-off frequency is 6 GHz and the bandwidth is 5 GHz, which is the same with the variable gain mixer in last section due to the same transconductor. However, the conversion gain response to the control voltage is different from the last VGM due to the different variable gain scheme. Figure 4.20 (b) indicates the conversion gain changes linearly with the control voltage. As the control voltage varies from 0.8 V to -0.5 V, a 10 dB gain control range is obtained with a linear-in-dB error of less than ±0.5 dB.
Double-sideband Noise Figure  After de-embedding, the DSB NF of the on-chip circuit is plotted versus the input frequency in Figure 4.21 (a) and versus the control voltage in Figure 4.21 (b). It can be seen that although the DSB NF increases when the frequency increases and when the control voltage decreases, a below 12 dB noise figure is achieved for all the operating frequency and gain settings.

P1dB and IP3  The P1dB and IP3 curves at 5 GHz and $V_{ctrl} = 0.8V$ (highest
Figure 4.21: Measured DSB NF (a) versus RF frequency and (b) versus control voltage.

Gain), are shown in Figure 4.22 (a) and (b). It is marked on the plot that the input-referred P1dB is -13.8 dBm, while the input-referred IP3 is -5.7 dBm.

The IP1dB and IIP3 responses to the input frequency and control voltage are illustrated in Figure 4.23 (a) and (b) separately. It can be seen from Figure 4.23 (a) that both IP1dB and IIP3 curves are relatively flat over the measured frequency range. Nevertheless, it is shown in Figure 4.23 (b) that although P1dB stays stable
as the control voltage changes, the IIP3 curve rises as the control voltage decreases. This means that as the conversion gain decreases, the third-order linearity of the design improves, which is believed to be a consequence of the changing load network. Detailed mechanism of this improved third-order intermodulation performance needs further investigation in future works.
4.4. MEASUREMENT RESULTS

![Graph](image)

Figure 4.23: Measured input referred P1dB and IP3 (a) versus input frequency and (b) control voltage.

**Port Isolations** Isolations between ports are also tested. LO-to-RF, LO-to-IF isolations are given in Figure 4.24 (a) and the RF-to-IF isolation is shown in Figure 4.24 (b). Similar to the last variable gain mixer, good LO-to-IF and RF-to-IF isolations are obtained, with more than 50 dB isolations presented over the whole frequency range. Due to the parasitic capacitance, the LO-to-RF isolation decreases from 50 dB at 1 GHz to 30 dB at 6 GHz.
4.4. MEASUREMENT RESULTS

Figure 4.24: Measured port isolations (a) LO-to-RF and LO-to-IF isolation and (b) RF-to-IF isolation.

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<td>18.8 (min)</td>
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Table 4.1: Comparison with recent variable conversion gain mixers.

**Power consumption** The total dc current consumed by this design is 28 mA and the dc supply voltage is 1.5 V. The core area of the chip is 0.66 x 0.66 mm$^2$ excluding the pads.

Table 4.1 summarizes the performance of the proposed two VCG mixers and gives a comparison with the recently published variable gain mixers.
It can be concluded from the table that by implementing the variable gain circuit at the IF stage, a low noise figure can be obtained through the whole frequency and conversion gain range. The lowest noise figures for both proposed VGMs are the same, which are measured as 3.8 dB. This value is lower than that of the other recently reported works listed in Table 4.1. Moreover, the continuous conversion gain ranges achieved are competitive, that a 13 dB range is obtained for the VGM with current-steering IF stage and a 10 dB range for the VGM with $R - r$ attenuator. Both of the proposed VGMs have a wide frequency range from 1 to 6 GHz. These improved characters make the designed VGMs suitable for low-noise, variable-gain and broadband applications. The core areas of both mixers are equally 0.44 mm².

4.5 Conclusion

In this section, two broadband, low-noise, variable conversion gain mixers are designed in CMOS 130 nm technology. The broadband transconductor is implemented with noise cancellation and current steering to provide low noise and high transconductance. Series inductive peaking is used to extend the frequency range. Two variable gain IF designs are proposed, using the current summing structure and the $R - r$ attenuation network respectively. Measured results show that both VCG mixers operate from 1 GHz to 6 GHz, with a S11 below -10 dB. A 13 dB gain range is achieved by the VCG mixer using current summing IF stage, while a 10 dB gain range is achieved by the VCG mixer using the $R - r$ attenuator IF stage. At the meantime, excellent noise and linearity performance are obtained in both designs.
Chapter 5

Summary and Conclusions

5.1 Summary

In this thesis, three broadband mixing circuits are presented in CMOS 130 nm technology, with special attention being paid to achieve low mixer noise. As one of the first few stages in a receiver, mixer’s noise performance is crucial in determining the system’s dynamic range and reducing the bit error rate, which means, improving the system’s ability of interpreting signals accurately. The widely used Gilbert cell mixers suffer from poor noise performances, therefore, different topologies have been studied to improve the noise feature of the Gilbert cell mixers, including both passive and active mixing circuits with noise cancellation techniques. In addition, variable conversion gain is also investigated to achieve a compact, multi-functional mixer.

The first circuit is a passive 2x subharmonic mixer that works from 4.5 GHz to 8.5 GHz. There are many advantages of reducing the LO frequency to a fraction of the RF frequency, including the improved LO phase noise performance and reduced dc offsets, which is especially important in a direct conversion system. By designing the
subharmonic mixer as two-stage passive Gilbert cell working in current domain, one can reduce the flicker noise which is proportional to the dc bias current commutated in the switching pair. Measurement results show that this subharmonic mixer has a high conversion gain of 16 dB and a low average DSB NF of 9 dB.

The second design is a broadband, low-noise variable gain mixer with variable conversion gain. The transconductor noise is improved by the implementation of the noise cancelling and current bleeding techniques. Gain variation in IF domain maintains the good noise performance of the transconductor stage. Measurements show that a wide gain control range of 13 dB is obtained, while the noise is lower than 14.2 dB over the entire frequency and conversion gain range. The lowest DSB NF is measured as 3.8 dB.

The third design targets at the linear-in-dB variable conversion gain, which is a feature required in automatic gain control systems. It uses the same transconductor stage with the second design, so that a broadband, low noise figure performance is obtained. A 10 dB linear-in-dB gain range is achieved with a linear-in-dB error less than ± 0.5 dB.

5.2 Future Work

Each design can be improved with several modifications in future studies.

For the 2x subharmonic mixer, which is designed for heterodyne receivers, it can be modified to a direct-conversion mixer. The low flicker noise character due to its passive current driving configuration, as well as the high immunity to dc offsets due to the subharmonic mixing, are required merits in a direct conversion receiver. The inverter-based transimpedance amplifier can be replaced by the op-amp based
transimpedance amplifier for higher conversion gain and lower input impedance, so that the mixer’s linearity and noise features can be further improved. The quadrature LO can be fully implemented on chip to increase the design integrity.

For the current summing variable conversion gain mixer, the already presented linear-in-dB gain control character needs to be further studied. Its gain control range can be further extended. The NF degradation as the conversion gain decreases should also be further investigated.

For the variable conversion gain mixer using R-r attenuator, more cross-connected transistors can be implemented to further extend the linear-in-dB gain control range. The voltage difference between each control voltages should be generated on chip so that the number of required dc biases can be reduced.

Next, all the mixers can be implemented with on-chip balun and buffer. Due to the loss of the off-chip balun and the lack of accurate active buffer model for simulation, derivations are introduced during measurement. Furthermore, if all components can be integrated on chip, then no de-embedding process is needed, therefore the accuracy of the obtained results can be increased.
Bibliography


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