A Scalable Model of Shielded Capacitors Using Mirror Image Effects

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Summary
Comb capacitors suitable for use in advanced complementary metal-oxide semiconductor (CMOS) technology nodes are frequently constructed from low metal layers located closely above the conductive silicon substrate. This results in high parasitic capacitances across the thin dielectric between the two layers. Therefore, a shield for reducing this parasitic capacitance is proposed in order to use the comb capacitor at high frequency. From electromagnetic (EM) simulation results using a 3D EM simulator, the quality factor (Q-factor) of the proposed shielded comb capacitor for the differential signal improved by 20% at 30-110 GHz compared to the unshielded capacitor. Consequently, a scalable model is proposed, which operates up to millimeter-wave frequencies. The results are verified by experimental data using fabricated comb capacitors from a 90nm 1P9M CMOS process. Compared with the experimental results, the simulated common-mode and differential-mode S parameters of the model has a root-mean-square (r.m.s.) error of under 2.1%.

Key words:
Comb capacitor, Shield, Scalable model, quality-factor, CMOS.

1. Introduction
Proliferation of millimeter-wave applications such as high-speed wireless data communications and the automotive radar have been actively studied, where small and low-cost millimeter-wave RF transceivers are required. Although millimeter-wave RF front-ends are conventionally realized using compound semiconductors, they can be achieved by sub-100nm CMOS process that has low power consumption [1]. In the CMOS process technology, on-chip capacitors are available. On-chip capacitors include the metal-insulator-metal (MIM) capacitor that is constructed from a thin insulation film between two plane metals [2], [3]. They also include the comb capacitor that uses metals in the same plane as finger structures [4]-[9]. A MIM capacitor has the advantage of being insensitive to the silicon substrate since the electric field is largely enclosed between the upper metal layers that make up the capacitor. However, MIM capacitors do not follow process scaling because the capacitance is inversely proportional to the insulator thickness, which does not scale according to process technology. As a result, since the area occupied by capacitors become relatively large as CMOS process technology progresses, MIM capacitors using parallel metal plates will not be used in the advanced CMOS processes. On the other hand, comb capacitors can be used in the pure digital CMOS process technology at no extra cost if embedded with any accompanying digital logics. In addition, large capacitance per unit area can be obtained by feature miniaturization through process scaling. Consequently in sub-100nm CMOS process technologies, comb capacitors will be widely employed in frequency matching circuits, D.C. blocks, analog-to-digital converters (ADC), digital-to-analog converters (DAC) and other circuits. However, comb capacitors are sensitive to the low resistance of silicon substrate through the parasitic capacitive couplings between the substrate and the metal of the comb capacitor [9].

To reduce parasitic capacitances for high-frequency performance, a comb capacitor with floating shields is proposed in this work. This paper will first evaluate the effectiveness of the comb capacitor shield with results verified by simulations. With the shield, the quality factor (Q-factor) of the differential signals in the proposed comb capacitor is increased by 20% at 30-110 GHz, compared to a conventional comb capacitor. An electromagnetic 3D field simulator has been used for the evaluation. In order to use the proposed capacitors in circuits, a scalable model of up to millimeter-wave frequencies has been developed. The r.m.s. errors of the model’s simulated common-mode and differential mode S parameters are under 2.1% of their corresponding measured values. With this model, the shielded comb capacitor is expected to be useful in future millimeter-wave designs.

2. Analysis of the Floating Shield
Although a comb capacitor was proposed as a solution for advanced CMOS processes, performance of the capacitor is sensitive to the conductive substrate because it acts as a plate terminal of a capacitor formed across the dielectric under the bottom metal of the comb capacitor [4]-[9]. Nevertheless, the Q-factor of the capacitor is sufficiently

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high in the frequency range of a several mega-hertz to low gigahertz since the effect of this parasitic element is small [3]. However, the low substrate resistance and the non-negligible parasitic capacitance degrade the Q-factor of the capacitor in the millimeter-wave band. To reduce the effect of the low substrate resistance, a comb capacitor with floating shields is proposed. This follows similar methods of reducing the eddy current causing the substrate effect for the inductor and the transmission line by using an electric shield under the signal path as reported in [10]. A comb capacitor with floating shields that has a mesh structure is proposed, as shown in Fig. 1. Figure 1 shows a multi-layered comb structure. Lower metal layers provide a total large surface area for higher capacitance. Since the lower metal layers are closer to the substrate, the shield is employed to reduce the eddy current from flowing in the substrate.

To prevent eddy current from flowing in the shield itself, which will lead to the reduction of the inductance of transmission lines and inductors, slits are included in the shield that are perpendicular to the direction of the eddy current flow. However, for the case of the capacitor, planar shields without slits are preferred as inductance is not desired. The undesired inductance effectively reduces the self-resonant frequency of the capacitor. Hence, mesh shields, which is similar to un-patterned plane shields, are adopted to satisfy the metal density rule of the process. In addition, the shield is made floating to minimize parasitic capacitances. Although one layer is enough for the reduction of parasitic inductance, another top layer is also used for preventing outside noise since top two layers hardly contribute to capacitance increase due to large metal spaces.

In Fig. 2, $C_s$ is the series capacitance of comb capacitor, $R_s$ is the series metal resistance and $C_{ox}$ is the parasitic capacitance between the capacitor and substrate. $R_{sub}$ is the substrate resistance which affects the current flowing to the ground and $R'_{sub}$ is the substrate resistance along which the current between the two ports flows. Since the resistance of the silicon substrate is much higher than that of the metal, $R'_{sub}$ is not negligible as compared to the series resistance of the metal when differential signals are applied. This results in the degradation of the Q-value.

Next, the derivation of an equivalent circuit model of the comb capacitor with a floating shield is discussed. Figure 3 shows the schematic cross-sectional view and the equivalent circuit of the shielded capacitor. The top metal layer is used for decreasing the parasitic inductance and has no significant contribution to the substrate losses. The shield used on the lower side of the capacitor, however, is made from the bottom metal layer which is closely located to the substrate. It is therefore reasonable that the power losses in the substrate occur through this shield.
In Fig. 3, \( C_{\text{shield}} \) is the parasitic capacitance between the comb capacitor and the shield. \( C_{\text{ox}}' \) is the capacitance between the shield and the substrate. \( R_{\text{shield}} \) is the resistance of the shield and \( R_{\text{sub}}' \) is the resistance of the substrate. Due to the low resistance of the copper shield, \( R_{\text{shield}} \) is significantly smaller than the substrate resistance \( R_{\text{sub}}' \) and can effectively be neglected, unlike the unshielded capacitor model of Fig. 2(b). The equivalent circuit is shown in Fig. 3(b). It can be seen that the derived model of Fig. 3(b) does not contain the substrate resistance \( R_{\text{sub}}' \), unlike the unshielded capacitor made of Fig 2(b). Therefore, the shielded comb capacitor is not affected by the lateral substrate current which should experience the resistance \( R_{\text{sub}}' \). As a result, the differential signals through this shielded capacitor suffer lower losses.

To verify the improvements, the \( Q \)-factors of a shielded comb capacitor and a conventional comb capacitor are compared by using the electromagnetic 3D field simulation software, Ansoft HFSS.

\[
\frac{Q_{\text{diff}}}{\text{imag} (Y_{\text{diff}})} = \frac{\text{real} (Y_{\text{diff}})}{Q_{\text{diff}}} \quad (1)
\]

The \( Q \)-factor for a differential signal is defined as Eq. (1). Here, the \( Y \) parameters corresponding to the \( S \) parameters of the differential signals are labeled as \( Y_{\text{diff}} \). In the simulation, a single-layered comb capacitor is used and compared with another capacitor of the same design that has floating shields placed above and below it. Figure 4 shows schematic device structure for 3D electric-magnetic field simulation. In the simulation, although the process parameters provided from the foundry, such as metal thickness and conductivity, were used, they are not shown according to non-disclosure agreement.

Shown in Fig. 5, the differential \( Q \)-factor of the shielded comb capacitor improves by 20% from that of the unshielded capacitor at the frequency between 30 GHz and 110 GHz. Here, the capacitances of shielded and conventional capacitor are 11.5 fF and 10.9 fF, respectively.

### 3. Scalable Circuit Model

Figure 6(a) shows the proposed shielded comb capacitor structure with representations of the circuit elements as used in the equivalent circuit model of Fig. 6(b).
connections. In the figure, $C_t$ is the series capacitance of comb capacitor, $R_s$ is the series metal resistance and $C_{air}$ is the parasitic capacitance between the substrate and the capacitor. $R_{sub}$ is the substrate resistance that affects the current flowing to ground, while $C_t$ and $L_t$ are the capacitance and the inductance, respectively, of the extension lines. The following extraction methodology is presented.

In order to estimate the series capacitance accurately, equations derived using the appropriate analysis have to be employed. Consider the capacitance of infinitely large conducting plates that is given by Eq. (2).

\[ C = \frac{\varepsilon A}{d} \]  

where $\varepsilon$ is the dielectric permittivity, $A$ is the area of the plates and $d$ is the distance between the plates.

As the fringe capacitance of the plane metals is not included in the evaluation of Eq. (2), it is not appropriate to be used for estimating the capacitance of the comb capacitor structure, where the fringe capacitance may be significant. Figure 7 illustrates the cross-section of the comb capacitor structure using three fingers at each of the three metal layers. To obtain a more accurate estimation, the center plane between upper and lower layers is treated as a virtual ground considering the mirror image effect, as shown in Fig. 7. The fingers above the virtual ground are now treated as parallel signal lines above the ground as shown in Fig. 7(b). The expressions for estimating the capacitance of parallel lines, which has been reported [11], shown in Fig. 7. The fingers above the virtual ground are considered as parallel lines shown in Fig. 7(b). The expressions for estimating the capacitance of the comb capacitor is considered as parallel lines shown in Fig. 8 by applying an ac current to the capacitor.

For the estimation of the series resistance $R_s$, the comb capacitor is considered as parallel lines shown in Fig. 8 by applying an ac current to the capacitor.

\[ C_{couple} = \varepsilon_{air} \left\{ 1.144 \frac{T}{S} \left( \frac{H}{H + 2.059S} \right)^{0.9944} \right\} + 0.7428 \left[ \frac{W}{W + 1.592S} \right]^{1.144} + 1.158 \left[ \frac{W}{W + 1.874S} \right]^{0.1612} \left( \frac{H}{H + 0.9801S} \right)^{1.179} \]  

where $W$ is the line width, $H$ is the distance from the lines to the virtual ground, $S$ is the space between the lines, and $T$ is the thickness of the lines. $N_f$ is the number of fingers, $L_f$ is the length of a finger and $N_{layer}$ is the number of metal layers used as fingers. $C_t$ is estimated from the results given by Eqs. (3) and (4) as

\[ C_t = N_f \cdot L_f \cdot N_{layer} \cdot (k_1 \cdot C_{air} / 2 + k_2 \cdot C_{couple}) \]  

where $k_1$ and $k_2$ are fitting parameters for considering process variations of metal fingers and dielectric layers. It is noted that $C_{air}$ is divided by two since each vertical capacitance between two fingers is the half of $C_{air}$.

The resistance of the parallel lines due to skin effect is estimated by Eq. (6).

\[ R_s = \frac{L_f}{w \sigma \delta (1 - e^{-T/\delta}) \cdot N_f \cdot N_{Layer}} \]  

where the skin depth $\delta$ can be obtained according to Eq. (7).

\[ \delta = \sqrt{\frac{2}{\omega \mu \sigma}} \]  

$\omega$ is the angular frequency, $\mu$ is the permeability and $\sigma$ is the conductivity.
Next, we consider the estimation of the substrate resistance \( R_{\text{sub}} \) and the parasitic capacitance \( C_{\text{ox}} \). According to Eq. (2), it is expected that the capacitance \( C_{\text{ox}} \) increases in proportion with the base area of the comb capacitor. Hence, \( C_{\text{ox}} \) can be estimated using a fitting coefficient \( k_3 \) according to Eq. (8).

\[
C_{\text{ox}} = k_3 \cdot \frac{\text{Area}}{N_f}
\]

\[
\text{Area} = N_f \cdot L_f \cdot W + S_{\text{connector}}
\]

\( W \) is the width of a finger and \( S_{\text{connector}} \) is the area of the tapered transmission line connection between the output to the exterior and the comb capacitor core. \( \text{Area} \) refers to the area of the base of the comb capacitor.

The current that flows from each finger across the vertical oxide capacitance \( C_{\text{ox}} \) and into the substrate will experience a resistance \( R_{\text{sub}} \). Recognizing that \( R_{\text{sub}} \) decreases in proportion to the base area of the capacitor, \( R_{\text{sub}} \) can be defined according to Eq. (9) using a fitting coefficient \( k_4 \).

\[
R_{\text{sub}} = k_4 \cdot \frac{N_f}{\text{Area}}
\]

The parasitic elements due to the extension lines, \( L_t \) and \( C_t \) are estimated directly from the measurement data. This inductance and capacitance of the extension lines are fitted with constants of \( k_j \) and \( k_o \), respectively, since they are not dependent on the size of a comb capacitor. Next, the extraction of the fitting parameters from measurements will be made by considering the common mode and differential mode separately. Common-mode \( S \) parameters are obtained according to Eq. (10).

\[
S_{\text{common}} = \frac{S_{11} + S_{12} + S_{21} + S_{22}}{2}
\]

Assuming that the effects of the extension lines are small, the equivalent circuit model of the comb capacitor can be drawn according to Fig. 9 when common-mode signals are injected into ports 1 and 2. In this case, the substrate resistance and the oxide capacitance remain while the connection between the ports 1 and 2 can be considered open since the potential difference between them is zero.

The admittance can be obtained from the common-mode \( S \) parameters according to Eq. (10). The substrate resistance and the oxide capacitance can then be obtained from the real and imaginary part of the \( Y \) parameters as shown in Eq. (11) and Eq. (12).

\[
R_{\text{sub}} = \text{real} \left( \frac{1}{Y_{\text{common}}} \right)
\]

\[
C_{\text{ox}} = \frac{\text{imag}(Y_{\text{common}})}{2\pi f}
\]

Eq. (13) shows the differential-mode \( S \) parameters.

\[
S_{\text{diff}} = \frac{(S_{11} + S_{22} - S_{12} - S_{21})}{2}
\]

The \( Y \) parameters corresponding to the \( S \) parameters of the differential signals are labeled as \( Y_{\text{diff}} \).

Since the series capacitance \( C_s \) is large compared with \( C_t \) and \( C_{\text{aux}} \), the self-resonant frequency can be approximated according to Eq. (14).

\[
f_s = \frac{1}{2\pi \sqrt{L_t C_s}}
\]

The series inductance \( L_t \) can be therefore be obtained when the self-resonant frequency \( f_0 \) is known. Recall that the capacitance \( C_s \) can be obtained by estimation and fitting, as had been explained.

4. Experimental results

Shielded comb capacitors are fabricated and measured to verify the validity of the proposed model. Figure 10 is the chip micrograph of the fabricated capacitor.
The process used is a 90nm CMOS 1P9M process. The metal layers from 2 to 7 are used for the fingers of the comb capacitor, while layers 1, 8 and 9 are used as floating shields. Measurement results for comparison are obtained after de-embedding using open and short test structures fabricated on the same chip, corresponding to $Y$ and $Z$-parameter subtractions respectively. The extension lines from the capacitor as described in the previous section are not de-embedded as they are a necessary part of the capacitor when used in circuits and have been modeled with values of $k_5$ and $k_6$. The variable parameters for design are the number of fingers $N_f$ and the length of fingers $L_f$. In the fabricated structures, the numbers of fingers are 32, 60, and 90 and the lengths of fingers are 9.5, 20.7, and 30.3\(\mu\)m. To maximize the capacitance per unit area, the line widths and spaces are selected for their minimum values.

<table>
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<th>Parameters in the models</th>
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<th>$k_2$</th>
<th>$k_3$</th>
<th>$k_4$</th>
<th>$k_5$</th>
<th>$k_6$</th>
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<td>$k_1$</td>
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<td></td>
<td></td>
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<tr>
<td>$k_2$</td>
<td></td>
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<td></td>
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<td></td>
<td>9.78 \times 10^{-10}</td>
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<td></td>
<td></td>
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<td>7.17 pH</td>
</tr>
</tbody>
</table>

Table 1 shows the values of parameters using in this model. In addition, capacitances and resistances calculated using in this model as a function of $L_f$ are shown in Fig. 11. It is noted that since $R_s$, being estimated from Eq. (6), is frequency-dependent resistance, values at 10GHz were shown in Fig. 11.

Figure 12 shows the comparison between the model and the measurement results. This figure shows the magnitude and the phases of the $S$ parameters in common and differential modes when the length of finger is 9.5\(\mu\)m for 32, 60 and 90 fingers.

Figure 13 shows the magnitude and the phases of the $S$ parameters in common and differential modes for capacitors with 60 fingers when the length of each finger is 9.5, 20.7 and 30.3\(\mu\)m. For both cases of varying the number of fingers and varying the length of each finger, the $S$ parameters of the models in differential mode and common mode fit well with measurement results. Through the fabrication of capacitor test structures using a 90nm 1P9M process, it has been verified that the r.m.s. errors between model characteristics and measurements to be within 2.1% for common mode and within 1.4% for differential mode.

![Fig.11. Capacitances and resistances calculated from the proposed model as a function of $L_f$.](image-url)
Fig. 12. Comparison between measurements and model simulations for different number of fingers.
Fig. 13. Comparison between measurements and model simulations for different finger lengths.
5. Conclusions

A shield for reducing the parasitic capacitance is proposed in order to use the comb capacitor at high frequency. Using a 3D EM simulator, the quality factor (Q-factor) of the proposed shielded comb capacitor for the differential signal is found to improve by 20% at 30-110 GHz compared to the unshielded capacitor. In addition, a scalable model is presented, which is accurate up to millimeter-wave frequencies. The accuracy is verified by experimental data using fabricated comb capacitors from a 90nm 1P9M CMOS process. Compared with the experimental results, the simulated common-mode and differential-mode S parameters of the model has an r.m.s. error of under 2.1%.

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References


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