Extending Synchronization from Super-threshold to Sub-threshold Region

Jun Zhou, Maryam Ashouei, David Kinniment*, Jos Huisken and Gordon Russell*

IMEC Netherlands & *Newcastle University
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
Sub-threshold Operation

- Minimum energy point VDD
- Low Performance Requirement

![Energy per Cycle Graph]

- Dynamic
- Leakage
- Total

Minimum Energy VDD
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
Multi-Low-VDD Systems on Chip

- VDD/Clock Domain A: Norm VDD
- VDD/Clock Domain B: Low VDD
- VDD/Clock Domain C: Sub-threshold VDD

Network on Chip

Synchronizers
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
Synchronizer Performance (MTBF)

\[
MTBF = \frac{t_s - T_d}{e^{\frac{\tau}{T_w f_c f_d}}}
\]

- \( t_s \): Synchronization Time
- \( T_d \): Normal Propagation Delay
- \( \tau \): Metastability Time Constant
- \( T_w \): Metastability Window
- \( f_c \): Clock Frequency
- \( f_d \): Incoming Data Frequency

**In the Super-threshold Region:**

- \( T_d \propto VDD \), \( VDD \downarrow \rightarrow T_d \uparrow \rightarrow MTBF \downarrow \downarrow \)
- \( \tau \propto \frac{C}{g_m} \) and \( g_m \propto I_d \propto VDD^2 \), \( VDD \downarrow \rightarrow \tau \uparrow \rightarrow MTBF \downarrow \downarrow \)

**In the Sub-threshold Region:**

- \( T_d \propto \frac{VDD}{e^{VDD}} \), \( VDD \downarrow \rightarrow T_d \uparrow \uparrow \rightarrow MTBF \downarrow \downarrow \downarrow \)
- \( \tau \propto \frac{C}{g_m} \) and \( g_m \propto I_d \propto e^{VDD} \), \( VDD \downarrow \rightarrow \tau \uparrow \uparrow \rightarrow MTBF \downarrow \downarrow \downarrow \)
Jamb Latch

Schematic

τ vs VDD

Vdd

Data

Clock

A

B

Reset

Out

4.0E-07
1.2E-07
3.4E-08
9.5E-09
2.8E-09
1.0E-09
3.2E-10
9.0E-10
3.2E-11
1.0E-11

VDD (V)

0.2
0.4
0.6
0.8
1
1.2

0.2 0.4 0.6 0.8 1 1.2

0.2 0.4 0.6 0.8 1 1.2

0.2 0.4 0.6 0.8 1 1.2
Improved Latch

Schematic

Jamb Latch

Improved Latch

$\tau$ vs VDD
Normal Propagation Delay $T_d$
Sub-threshold MTBF

$$MTBF = \frac{e^{-\frac{t_s - T_d}{\tau}}}{T_w f_c f_d}$$

At 0.3 V, $T_w = 30 \sim 50$ ns. Assuming that $f_c = f_d = 300$ KHz:

<table>
<thead>
<tr>
<th></th>
<th>$\tau$</th>
<th>$T_d$</th>
<th>MTBF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jamb Latch</td>
<td>400 ns</td>
<td>0.7 us</td>
<td>0.17 s</td>
</tr>
<tr>
<td>Improved latch</td>
<td>92 ns</td>
<td>1.5 us</td>
<td>2 days</td>
</tr>
</tbody>
</table>

Two factors are not taken into account in the calculation:
1. System MTBF = Single MTBF / Num of Synchronizers
2. Large Process Variation in the Sub-Threshold Region
Process Variation

\[ MTBF = \frac{\frac{t_s - T_d}{\tau}}{T_w f_c f_d} \]

Mean: 440 ns  
Std: 230 ns

Variation of Tau for Jamb Latch at 0.3 V
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
Increasing Transistor Size?

\[
\tau \propto \frac{C}{g_m}
\]
Applying Forward Body Bias (FBB)

Advantages:

1. Increase $g_m$ without increasing C. So tau is reduced.

2. Propagation delay is reduced like other logic circuits.

3. Process variation is improved.

Super-threshold: $g_m = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)$

Sub-threshold: $g_m = \frac{I_d}{n \cdot V_{th}}$, $I_d \propto e^{-V_T}$
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
**Tau vs FBB**

- **Jamb Latch with FBB**: 8 times reduction
- **Improved Latch with FBB**: 7 times reduction

Decreasing VDD
Propagation Delay vs FBB

Jamb Latch with FBB

Improved Latch with FBB

5 times reduction

4 times reduction
Process Variation

Without FBB at 0.3 V

Mean: 440 ns
Std: 230 ns

With FBB at 0.3 V

Mean: 54 ns
Std: 25 ns

Std: 10 times reduction

Mean: 440 ns
Std: 230 ns
Sub-threshold MTBF

\[ MTBF = \frac{t_s - T_d}{e^\tau} \frac{T_w}{f_c f_d} \]

At 0.3 V, \( T_w = 7 \sim 15 \text{ ns} \), assuming that \( f_c = f_d = 300 \text{ KHz} \):

<table>
<thead>
<tr>
<th></th>
<th>( \tau )</th>
<th>( T_d )</th>
<th>MTBF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jamb Latch</td>
<td>400 ns</td>
<td>0.7 us</td>
<td>0.17 s</td>
</tr>
<tr>
<td>Improved latch</td>
<td>92 ns</td>
<td>1.5 us</td>
<td>2 days</td>
</tr>
<tr>
<td>Jamb Latch with 0.3V FBB</td>
<td>49 ns</td>
<td>0.14 us</td>
<td>( 1.35 \times 10^{17} ) years</td>
</tr>
<tr>
<td>Improved Latch with 0.3V FBB</td>
<td>13 ns</td>
<td>0.32 us</td>
<td>( 4.88 \times 10^{89} ) years</td>
</tr>
</tbody>
</table>
• Sub-threshold Operation
• Synchronization in Multi-Low-VDD Systems on Chip
• Low Voltage Synchronizer Design
• Sub-threshold Synchronizer Design
• Results
• Implementation
• Conclusion
Full-VDD Biased Synchronizer

Advantage:

1. Full-VDD bias gives large performance improvement.

2. No on-chip voltage generation circuit needed (Min Power and Area Overhead).

3. The Bias can be disabled when VDD is higher than the PN junction conducting voltage (0.7 V) to avoid performance degradation.
- Sub-threshold Operation
- Synchronization in Multi-Low-VDD Systems on Chip
- Low Voltage Synchronizer Design
- Sub-threshold Synchronizer Design
- Results
- Implementation
- Conclusion
Conclusions

1. For the first time, synchronizer performance is investigated in the near-threshold and sub-threshold region.
2. The investigated synchronizers shows unacceptable MTBF especially when taking into account the process variation.
3. Applying Forward Body Bias significantly improves $T_d$ and $\tau$. It also greatly reduce the impact of process variation on synchronizer performance. As a result, MTBF is significantly improved.
4. A full-VDD biased synchronizer scheme is proposed to improve synchronizer performance in the near-threshold and sub-threshold region with minimal area and power overhead.
Thank you!