A PROGRAMMABLE PRE-CURSOR ISI EQUALIZATION CIRCUIT FOR HIGH-SPEED SERIAL LINK OVER HIGHLY LOSSY BACKPLANE CHANNEL

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ABSTRACT

This paper presents a programmable pre-cursor ISI equalization circuit for high-speed serial data transmission over highly lossy electrical backplane channels. Although decision-feedback-equalizer (DFE) provides an effective way to compensate various channel impairments, such as frequency dependent loss, dispersion and reflections in the legacy backplane environment, for high-speed, highly lossy band-limited channel, the pre-cursor inter-symbol interference (ISI) is still a significant problem for channel equalization. A programmable pre-cursor ISI equalizer combined with a 3-tap DFE is implemented to work at 10-Gb/s and compensate the channel loss of -20 dB. The results show it outperform a traditional 5-tap DFE.

Index Terms—Backplane, ISI, equalization, decision-feedback equalizer (DFE), band-limited channel, serial link, SerDes, wireline transceiver.

1. INTRODUCTION

The continuous improvement on the performance of CMOS ICs made it possible to transmit signals at the data rates above multi-Gb/s over cables or backplanes. Due to the price-competitiveness of the legacy backplane, it is still one of the main transmission media for high-speed serial communications. The backplane is a complex environment consisting of at least 11 different components and presents a serious challenge to data rates above 5-Gb/s [2]. The multi-Gb/s data rates serial communications are running into the bandwidth limitation of the backplanes. The bandwidth limitation is mainly caused by dielectric loss, skin effect, and impedance discontinuities of the media. At data rates above the bandwidth of the band-limited channels, the received signals are severely distorted due to the inter-symbol interference (ISI).

Equalization is one of the means to compensate the distortion caused by the effects of the band-limited transmission media. The equalizer can be implemented as pre-emphasis (or de-emphasis) in the transmitter, or decision-feedback equalizer (DFE) in the receiver. There are several categories of equalizers used extensively, linear or non-linear equalizers, continuous-time or discrete-time equalizers, etc. Among all the types of equalizers, DFE is the most effective one and it is regarded as the sub-optimum receiver without any decision delay [8]. Compared with the pre-emphasis in the transmitter, the DFE can be implemented with adaptation algorithms to compensate the time variation and piece-wise variation of the transmission properties of the backplane channels without extra back-channel transmission as in adaptive pre-emphasis.

Although the adaptive DFE has advantages over other equalization methods, it can not remove the pre-cursor ISI. The reason is that DFE is a strictly causal system or it removes ISI on the basis of decisions that have been made (the past bits). Therefore, the DFE performance heavily depends on the joint channel pulse response. The joint channel pulse response can be reshaped with linear equalizers. Because the properties of a backplane channel are time variant and piecewise variant, the linear equalizers used to reshape the joint channel pulse response should be programmable. This paper describes a programmable pre-cursor ISI equalization method for 10-Gb/s transmission over a backplane channel with ~20 dB loss at Nyquist frequency. This equalizer, combined with a 3-tap DFE, has better performance than a 5-tap traditional DFE.

The next section discusses the general properties of the backplane channels. A brief review of some widely used equalization structures is also given. In Section 3, the proposed pre-cursor ISI equalization circuit and DFE circuits are presented. Results on this equalizer are compared with the results on a 5-tap traditional DFE are followed in Section 5. Conclusion is drawn in Section 5.

2. BACKPLANE CHANNEL AND EQUALIZATION

2.1 Backplane Channel Characteristics

The magnitude and phase frequency response of a typical backplane channel is shown in Fig. 1. The attenuation is about ~20 dB at the 5-GHz (Nyquist frequency for 10-Gb/s data rates). The 3-dB bandwidth of this backplane is 500-MHz. The phase response is shown in wrapped mode to 5-GHz frequency, the nearly linear phase response can be observed, and the delay at 5-GHz is 5.43-ns. Therefore, the distortion of the received signals is mainly from the frequency dependent loss of the channel. The notch around
4-GHz is caused by the impedance discontinuities and this results in reflection that deteriorates ISI in the receiver.

The channel pulse response when a 1-V 100-ps rectangular pulse is applied to the input is shown in Fig. 2. The received pulse is attenuated in magnitude, extended in time and delayed by ~5.45-ns. The pre-cursor ISI (83.33-mV) is comparable to the second post-cursor ISI (92.06-mV). Therefore, for this channel, the DFE with as many taps as possible to completely remove post-cursor ISI can not achieve the same performance of a 3-tap DFE when pre-cursor ISI is not removed. For this channel with the pre-cursor ISI, the maximum received signal eye height that a conventional DFE can achieve is the distance from the main tap to the pre-cursor tap (315.4mV – 83.33mV = ~232mV).

2.2 Channel Equalization

The equalization is one of the effective means to compensate the impairments caused by the low-cost backplane environment. It can be implemented with different structures.

Pre-emphasis (also called feed-forward equalizer) is usually a multi-tap FIR filter implemented in the transmitter. Constrained by the peak transmitter power, it actually de-emphasizes the low frequency components to achieve a response whose Discrete Fourier Transform is flat. Therefore, the de-emphasis FIR reduces the ISI at the expense of received signal swing, and the signal-to-noise ratio (SNR) in the receiver is decreased. Another disadvantage of the equalizer in the transmitter is the difficulty to use adaptive algorithm without a back-channel.

For high-speed multi-Gb/s data transmission, it becomes more and more difficult to implement receiver equalizer in the format of FIR filter except for DFE, because it must perform delaying, multiplying, and adding analog (or multi-level) signals in only one bit period (the baud period). Therefore, some continuous-time equalizer utilizes inductors or/and capacitors to obtain zeros at high frequency to flatten frequency response. It can be implemented with on-chip inductors. Conventional design of this type of equalizer does not provide any programmability to modify the inductance or/and capacitance.

Although the feedback branch of DFE is also FIR filter, its inputs are binary. This advantage greatly simplifies circuit implementation at high data rates. In addition DFE theoretically does not enhance noise as linear equalizers do. The filter coefficients of the DFE can be adapted easily with a sign-sign least-mean-square (SS-LMS) algorithm. The tap coefficients are adapted with equation 1.

\[ C(n + 1) = C(n) + 2\mu \text{sgn}[e(n)]\text{sgn}[d(n)] \]  

(1)
where, \(C(n+1)\) is new coefficient value, \(C(n)\) is present coefficient value, \(\mu\) is the convergence factor, \(e(n)\) is the error signal, \(d(n)\) is the received data signal and \(\text{sgn}[f]\) is sign function.

Despite the various advantages of DFE it does not necessarily outperform other equalization methods for a channel with strong pre-cursor ISI. To achieve the best performance, a conventional equalizer is usually used as a feed-forward-equalizer (FFE) to reduce pre-cursor ISI, and DFE is used to remove post-cursor ISI. Unfortunately, it has been reported the combination of transmitter FFE and DFE only damages the link performance for highly distorted channels [3]. The combination of receiver FFE and DFE may help. However, if the FFE does not provide any programmability, it may reshape the channel response to give more pre-cursor ISI when the channel properties vary.

### 3. Proposed Pre-Cursor ISI Equalization

#### 3.1 Equalization Architectures

There are several high-speed equalization architectures published recently. A parallel-path equalizing filter with inductors and adaptive current source circuit is proposed for 40-Gb/s copper cable with -10dB loss [4]. The equalizer is designed with 10 on-chip inductors. Another Rx equalizer is a 4-stage equalizer for 6-Gb/s and each RxEQ unit in one stage can compensate 5-dB at 3-GHz (Nyquist frequency) with 4-bit programmability [5]. These equalizers are merely linear continuous-time equalization methods in the receiver side. In paper [1], a 4-tap transmitter FFE and 5-tap receiver DFE are designed to work at 10-Gb/s. However, as discussed in paper [3], transmitter FFE reduces SNR of the received signals, and it interacts with DFE adaptation. This topology only deteriorates link performance. Therefore, this paper locates the optimum sampling instants to reduce pre-cursor ISI and use unrolling DFE to eliminate post-cursor ISI.

We proposed a continuous-time pre-cursor ISI linear equalization (prLE) circuit for highly lossy backplane channel in this paper. It is composed of 4-bit programmable capacitive degeneration, and two optional on-chip spiral inductors. The circuit is shown in Fig. 4. The on-chip inductors and capacitors generate two zeros above the bandwidth of the channel to amplify the attenuated high frequency signals and boost the effective bandwidth. Therefore, the pre-cursor ISI can be reduced. The inductors can be optionally bypassed for some type of channel with low loss.

The voltage transfer function of the continuous-time prLE is

\[
A_p(s) = \frac{V_{OUT}(s)}{V_{IN}} = \frac{g_m}{1 + g_m (R_s \parallel 1/C_s)} \cdot (R_s + sL_d) \quad (2)
\]

where, \(g_m\) is the transconductance of NMOS MN1/MN2.

![Fig. 4. The pre-cursor ISI linear equalization (prLE) circuit.](image)

The source degeneration capacitor \(C_s\) is programmable with four control bits.

\[
C_s = \sum_{i=1}^{4} b_i C_{S_i} \quad (3)
\]

The DC gain of the prLE is determined by the load resistance \(R_L\) and source degeneration resistance \(R_s\).

\[
A_p|_{DC} = \frac{R_s}{R_L} \quad (4)
\]

At frequency above the channel bandwidth, the two zeros from the load inductors and source capacitor would enhance the gain of the prLE. With \(g_m (R_s \parallel /sC_s) \gg 1\), the gain is

\[
A_p(s) = \left(\frac{R_L + sL_d}{R_s}\right)(1 + sR_s C_s) \quad (5)
\]

#### 3.2 Equalizer with prLE and 3-tap DFE

It can be seen from Fig. 8 that the prLE not only reduces the pre-cursor ISI, but also makes the post-cursor ISI smaller. In this work, the equalization scheme combines in the receiver side a prLE for pre-cursor ISI reduction and a 3-tap DFE for post-cursor ISI removal. There are trade-offs in the design. The prLE is not used to compensate all the channel loss in the whole pass-band, but to boost the channel bandwidth to reduce pre-cursor ISI. If the gain of the prLE is too large, it will also amplify much of the noise and crosstalk at frequencies where SNR is poor. The prLE can be programmed to cope with time variant channel and piece-wise variant channel.
A sign-sign LMS adaptive DFE follows the prLE is used to remove post-cursor ISI. For the highly lossy backplane channel without prLE, the height of the eye-opening can not be improved even with 5 or more taps DFE. This is because the pre-cursor ISI would be the dominant interference. With prLE in the receiver to compensate the channel bandwidth, both the pre-cursor ISI and post-cursor ISI can be reduced. Therefore, the adaptive DFE can be implemented with 3-tap in this architecture. The entire equalization circuit in the receiver is shown in Fig. 5.

![Fig. 5. The equalization circuit in the receiver.](image)

The magnitude and phase frequency response of the prLE is shown in Fig. 6. With the two zeros, the gain is boosted for 3-dB at 500-MHz for this high loss channel, and about 14-dB at 5-GHz (the Nyquist frequency). From the phase response, the two zeros also introduce phase distortion, but it is neglectable in the systems. The decrease of the magnitude above is due to the CMOS technology.

![Fig. 6. The frequency response of the pre-cursor ISI equalizer.](image)

The frequency response of the channel, the prLE and the channel+prLE is shown in Fig. 7. The bandwidth of the channel is extended to around 2-GHz with the 4-bit programmable prLE.

![Fig. 7. The frequency response of the channel, prLE and combination.](image)

4. EXPERIMENT RESULTS

The equalizer with prLE and 3-tap DFE (EUQ2) is compared with the equalizer with 5-tap DFE (EQU1).

4.1 Impulse Response

The 1-V 100-ps square impulse response of the EQU1 and EUQ2 is shown in Fig. 8. For the EQU1 (up) with 5-tap DFE, the five post ISIs are cancelled at the sampling points (the circles in the plot, and the pre-cursor one is not changed which is almost 1/3 of the main tap and close to the 2nd post ISI in magnitude. However, the pre ISI of the EQU1 is 1/5 of the main tap, and the post 3 ISIs are cancelled with the 3-tap DFE.

![Fig. 8. The impulse response of equalized signals, prLE+3-tap DFE and 5-tap DFE.](image)
frequency. The pre-cursor ISI is 26.4% of the main tap for EUQ1, and 15.4% for EUQ2. The 3rd post-cursor ISI is lower than the first pre-cursor ISI; therefore, 3-tap DFE for post-ISI cancellation is adequate.

Table 1: Comparison of impulse response with and without pre-cursor ISI equalization (prLE)

<table>
<thead>
<tr>
<th></th>
<th>w/o prLE</th>
<th>w/ prLE</th>
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<tbody>
<tr>
<td>Pre-cursor ISI 1</td>
<td>83.33mV</td>
<td>139.7mV</td>
</tr>
<tr>
<td>Main tap</td>
<td>315.4mV</td>
<td>906.6mV</td>
</tr>
<tr>
<td>Post-cursor ISI 1</td>
<td>215.5mV</td>
<td>169.3mV</td>
</tr>
<tr>
<td>Post-cursor ISI 2</td>
<td>92.06mV</td>
<td>-196.3mV</td>
</tr>
<tr>
<td>Post-cursor ISI 3</td>
<td>49.46mV</td>
<td>-115.6mV</td>
</tr>
<tr>
<td>Post-cursor ISI 4</td>
<td>32.92mV</td>
<td>-23.07mV</td>
</tr>
<tr>
<td>Post-cursor ISI 5</td>
<td>30.38mV</td>
<td>11.11mV</td>
</tr>
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</table>

4.2. Eye Diagram

The proposed equalization system is designed for 10-Gb/s data rate over the highly lossy backplane channel (-20dB loss at 5-GHz). The eye diagram of 5-tap DFE and 3-tap DFE with prLE are compared and shown in Fig. 9. As shown in Fig 9, the received signal (a) is severely distorted due to the frequency-dependent loss of the channel; (b) the equalized signal with only 5-tap DFE, the vertical height of the eye is 165.8-mV. This is because the pre-cursor ISI is 83.33-mV which is comparable with the 2nd post-cursor ISI. The eye-opening can not be improved with even more taps on the DFE; (c) the signal is equalized with prLE. The eye is opened, however the signal to noise ratio is not improved too much; (d) the signal is compensated with prLE and 3-tap DFE. The height of the eye is 558.6-mV which is enhanced about three times than the 5-tap DFE equalization method.

The vertical height of the received signals at the data center sampling point (the dot line in Fig. 9) are compared, as shown in Fig.10. From the plot, we can see the received signals (a) are spread between 0-V and 1-V, and it is difficult to detect the high or low logic levels from the distorted signals. From the histogram plot of 5-tap DFE in Fig. 10(b), the center distributions of the low or high levels are 0.1-V or 0.5-V, respectively. The magnitude and the eye opening of the received signals are improved with prLE and 3-tap DFE equalization scheme, as shown in Fig. 10(b). Now, the distribution centers of the low and high levels are 0.1-V and 1.0-V, respectively.

Table 2: Comparison of eye diagram of the two architectures at 10-Gb/s.

<table>
<thead>
<tr>
<th></th>
<th>Vertical height</th>
<th>Horizontal Jitter</th>
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<tbody>
<tr>
<td>DFE w/o prLE</td>
<td>165.83mV</td>
<td>29.65ps</td>
</tr>
<tr>
<td>DFE w/ prLE</td>
<td>558.60mV</td>
<td>27.60ps</td>
</tr>
</tbody>
</table>

The horizontal jitters of the received signals with the two equalization architectures (5-tap DFE and prLE + 3-tap DFE) are compared and shown in Fig. 11. There is a little improvement on the jitter performance with the pre-cursor ISI linear equalization (prLE) in the receiver.
5. CONCLUSION

The bandwidth of the transmission media and the data rates of signals transmission conflict with each other. The inter-symbol interference (ISI) is severe when the Nyquist frequency of the transmitted signals is more above the bandwidth of the channel. To transmit signals at high speed and make the bandwidth used efficiently, the pre-coding (to lower the signals bandwidth requirement) or equalization (to compensate the channel bandwidth) is extensively utilized in modern serial data communications. Decision-feedback equalizer (DFE) is still the very effective equalization method for cancelling the post-cursor ISI with adaptive algorithms. In this paper, DFE combined with a programmable pre-cursor ISI equalization (prLE) can achieve larger eye-opening (higher SNR and lower BER) with better trade-off on noise amplification and pre-cursor ISI reduction.

6. REFERENCES


