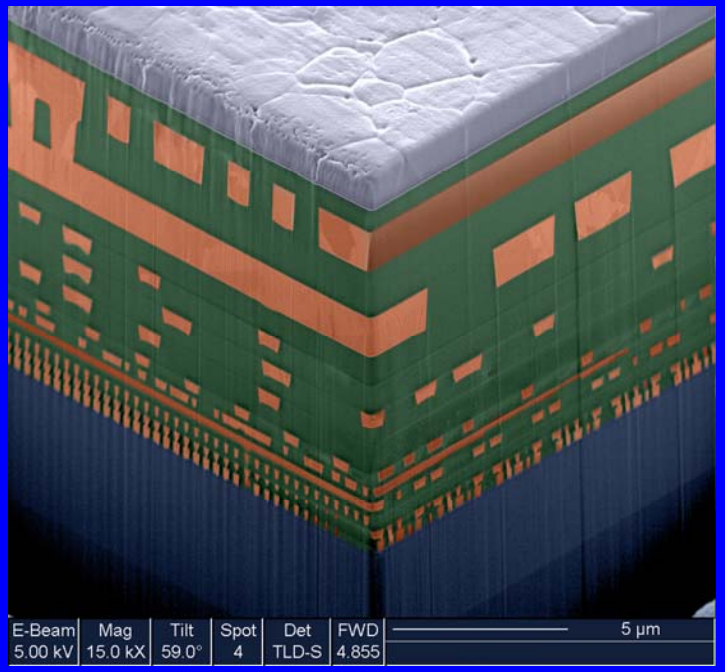
Copper Interconnect Technology for the 32 nm node and Beyond

Jeff Gambino

IBM Microelectronics

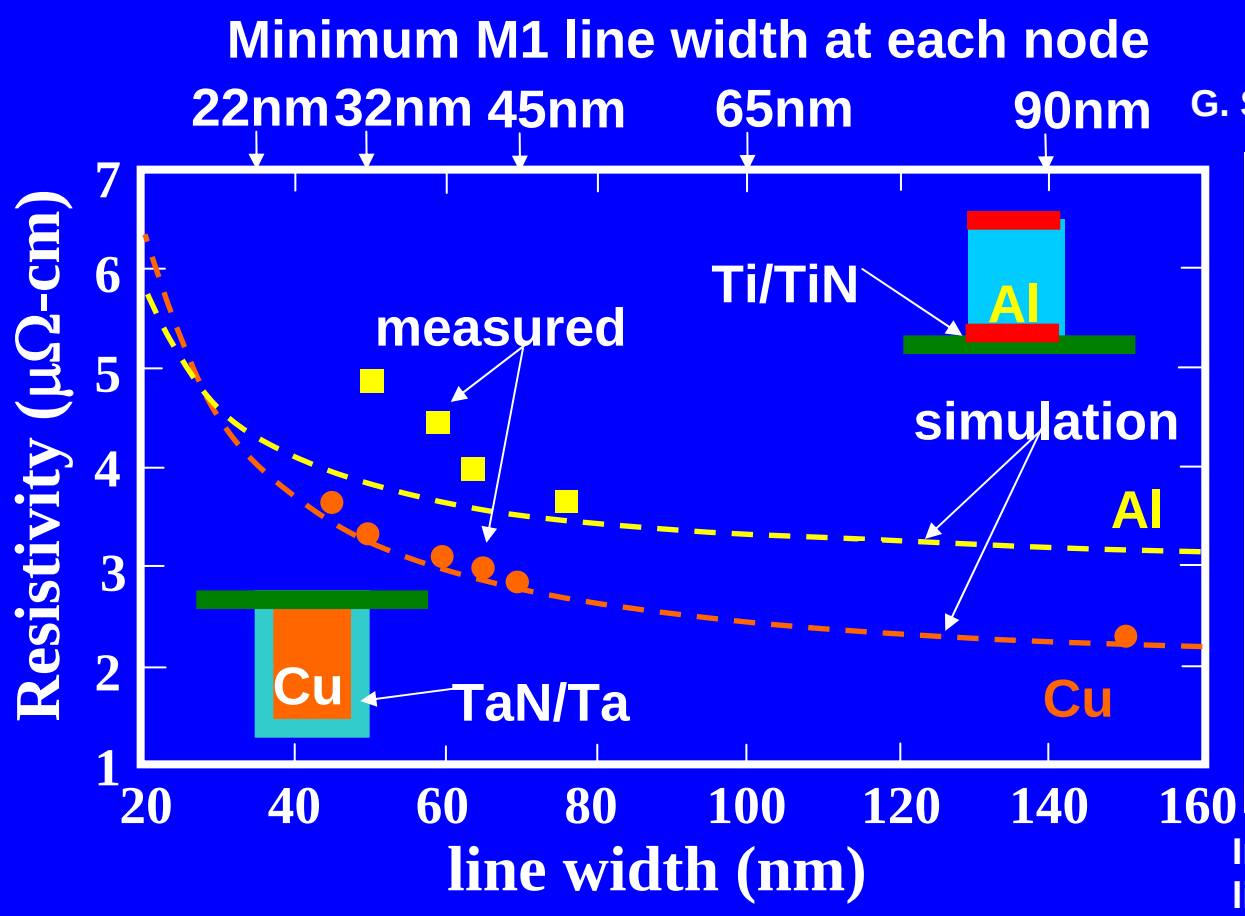
Essex Junction, Vermont



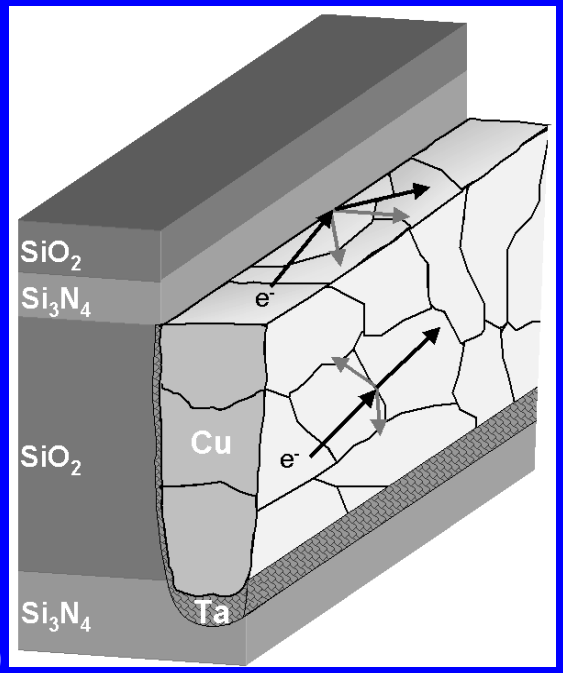
Outline

- Copper interconnect scaling
- Copper interconnect reliability
- Packaging + Through silicon vias (TSV)
- Passive devices

Effect of scaling on resistivity



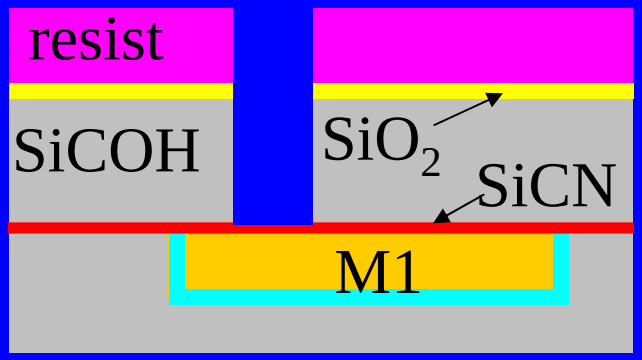
G. Schindler et al., AMC., 2002, p. 13.



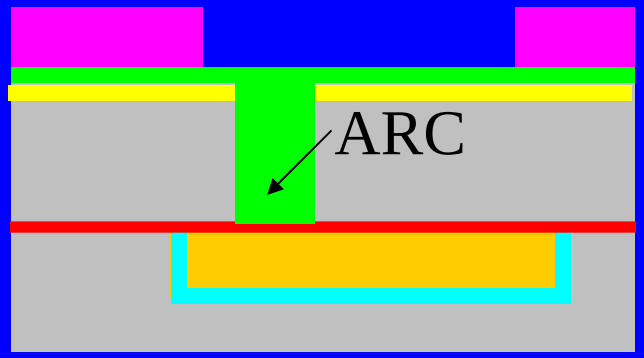
Increased resistivity for narrow lines due to grain boundary scattering, surface scattering, and Ta barrier layer.

H.B. Lee et al., IITC Proc., 2007, p. 64.

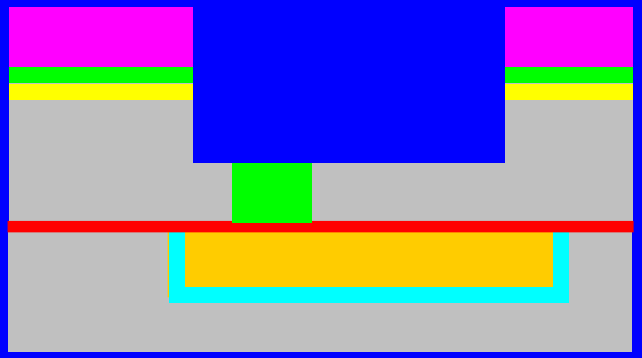
Dual damascene process in SiCOH; via-first



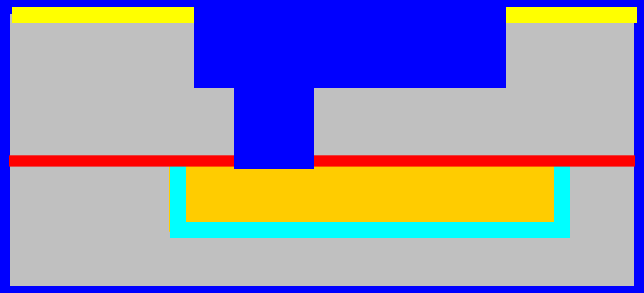
1. V1 via lithography + RIE



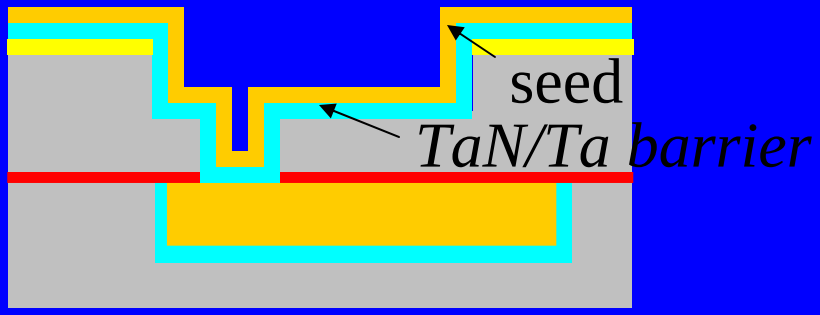
2. M2 trench lithography



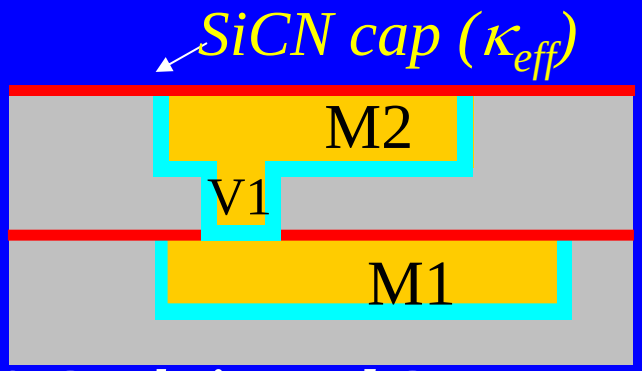
3. M2 RIE



4. M2 resist strip + SiCN RIE

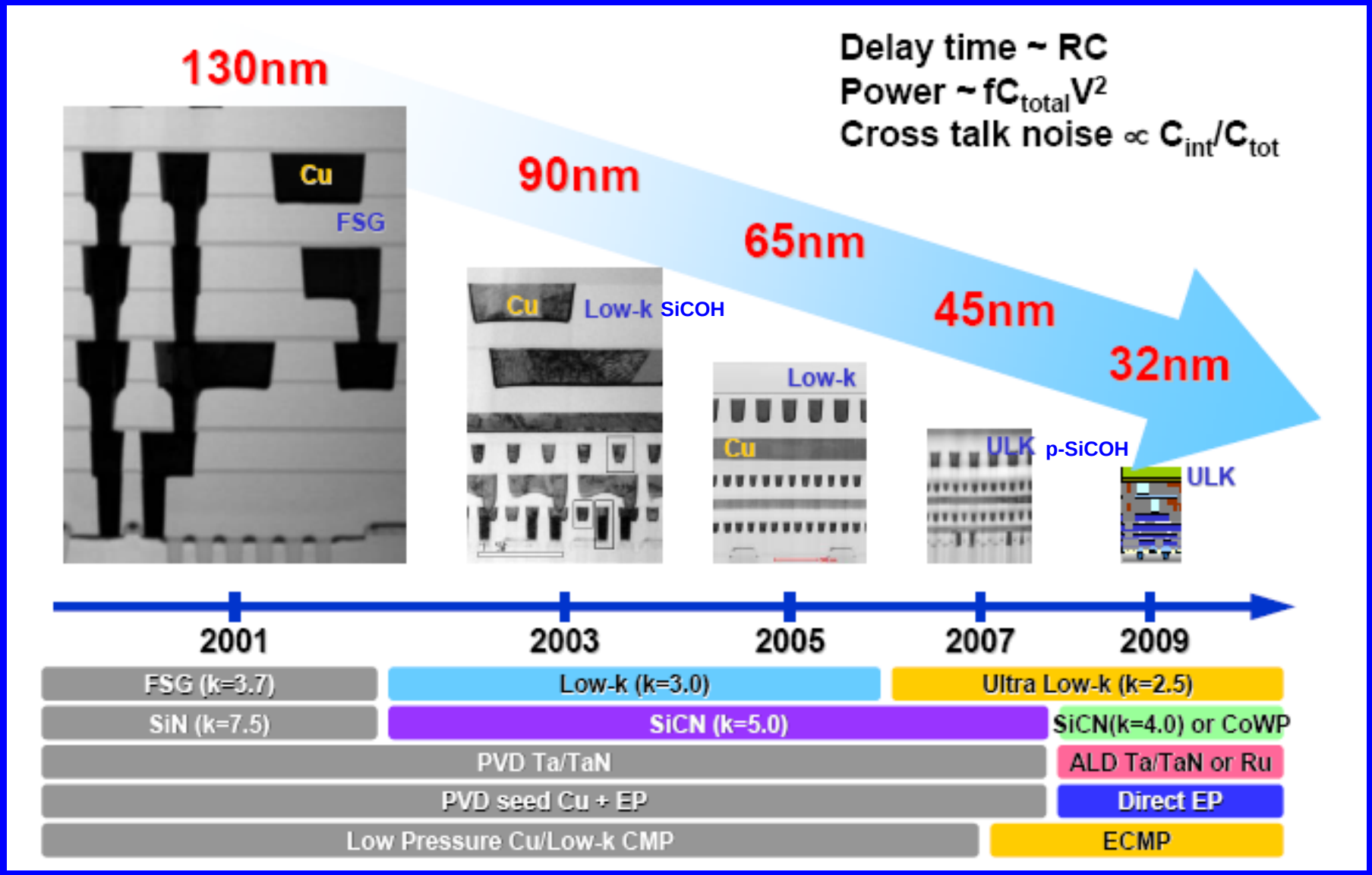


5. Deposit liner and seed



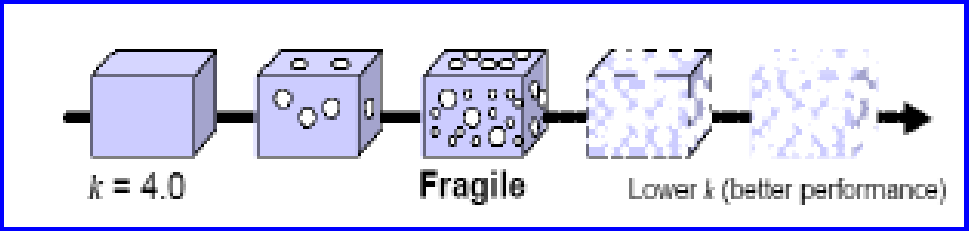
6. Cu plating and CMP, cap

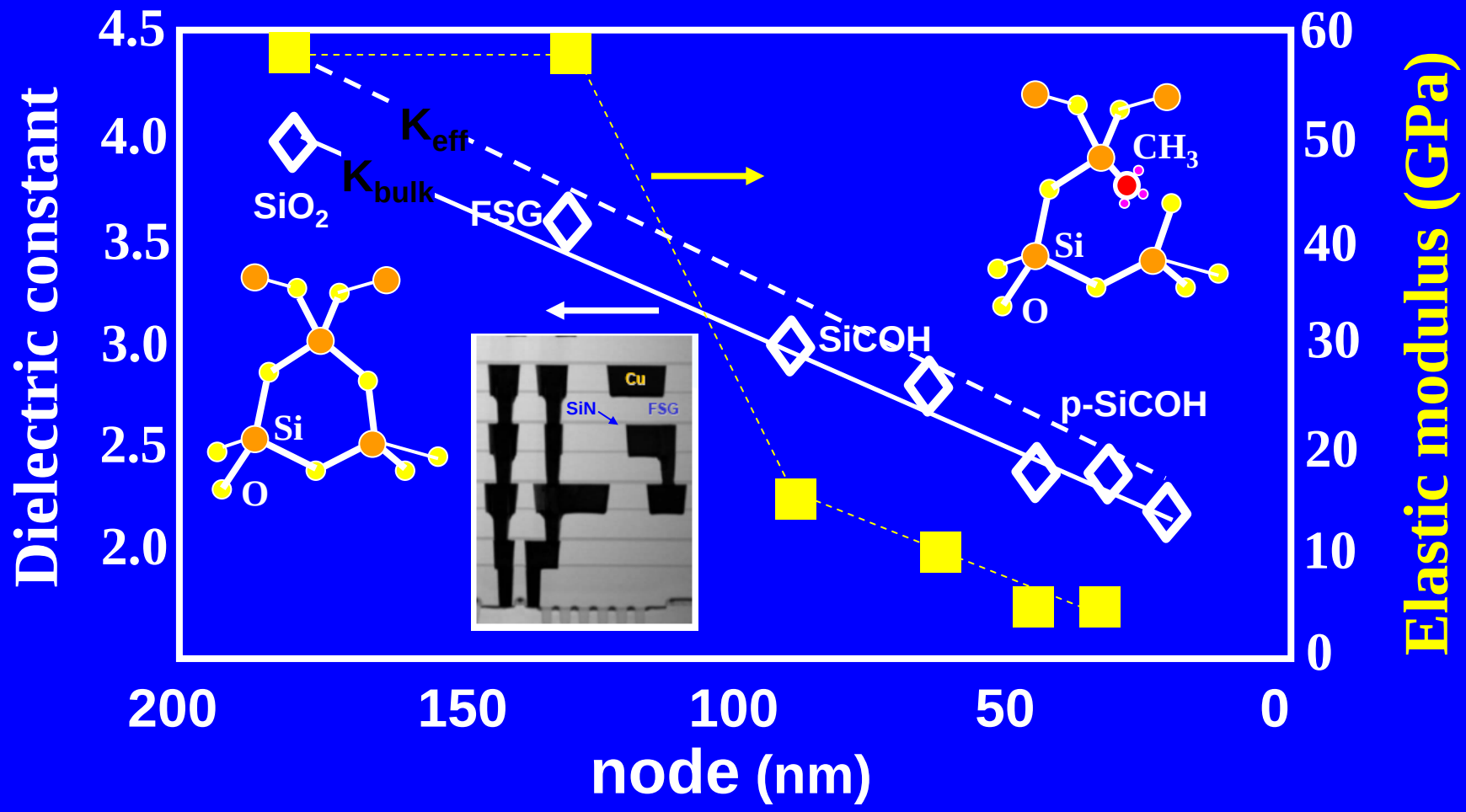
Interconnect roadmap



H.-K. Kang, tutorial on Advanced Logic Technology, 2007

Dielectric trend



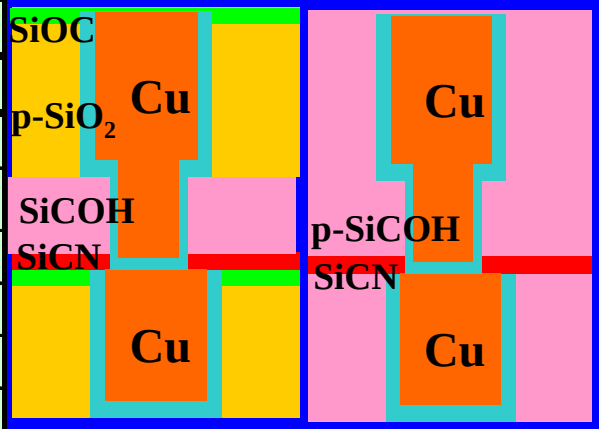


BEOL integration at 32 nm node

Y. Hayashi et al., AMC Proc., 2005.
M. Tada et al., IEDM Proc., 2006.
M. Aimadeddine et al., IITC Proc., 2007.
X. Chen et al., VLSI Symp., 2008.

reference	Hayashi et al		Tada et al		. Aimadeddine et	
company	Toshiba		NEC		ST	
patterning	hardmask		hardmask		hardmask	
integration	hybrid		hybrid		homo. low-k	
layer	material	κ	material	κ	material	κ
polish stop	SiOC	2.6	SiOC	3.1	******	****
trench dielectric	PAE	2.6	p-SiO_2	2.4	SiOC	2.3
trench etch stop	******	***	******	*****	*****	*****
via dielectric	SiOC	2	SiOC	2.8	SiOC	2.3
cap	CuSiN	***				
via etch stop	SiC	3	SiCN		SiCN	
κ_{eff}		2.4		2.9		

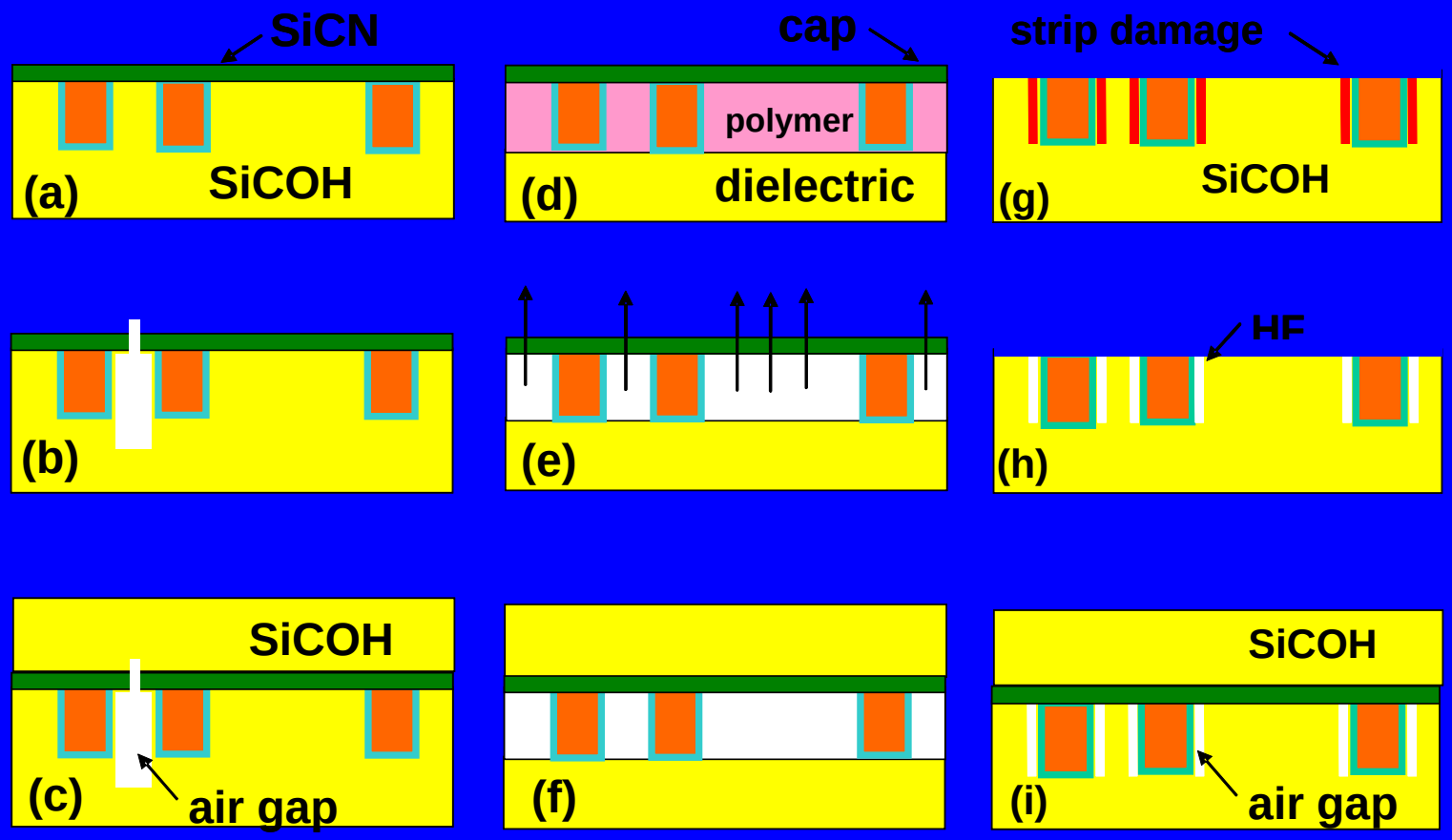
Rule	Pitch (nm)	Scaling factor from 45nm
Contacted Gate Pitch	126	70%
CA pitch	100	63%
N+/P+	56 (space)	70%
1X metal	100	71%
1.3X metal	130	New level
2X metal	200	71%



Hybrid (NEC) Homo Low-k (ST)

Target for k_{eff} = 2.4

Air-gap



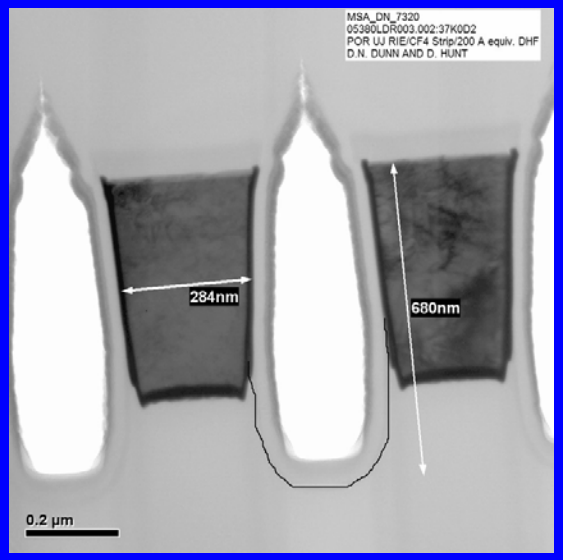
Masked etchback
(local airgap)

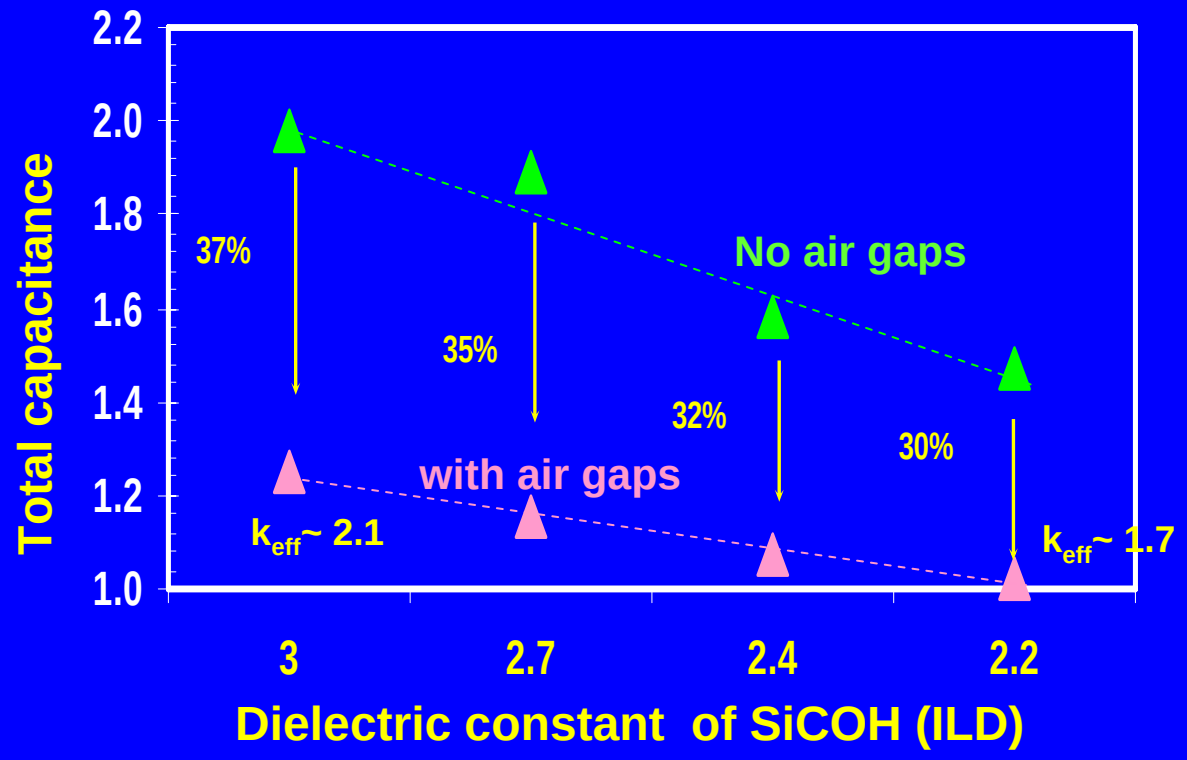
Thermal decomposition
(glocal airgap)

Sidewall airgap
(local airgap)

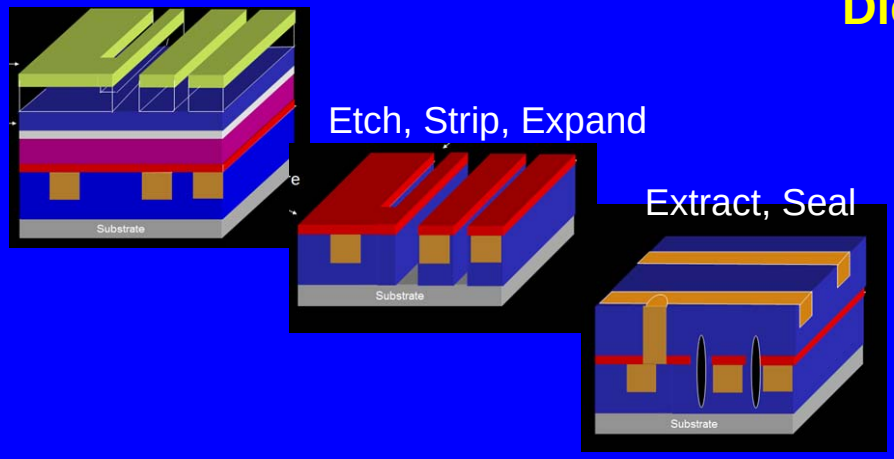
Air-gap

S. Nitta et al., AMC Proc., 2007
S. Nitta et al., IITC Proc., 2008





Gap/Blockout Mask



Etch, Strip, Expand

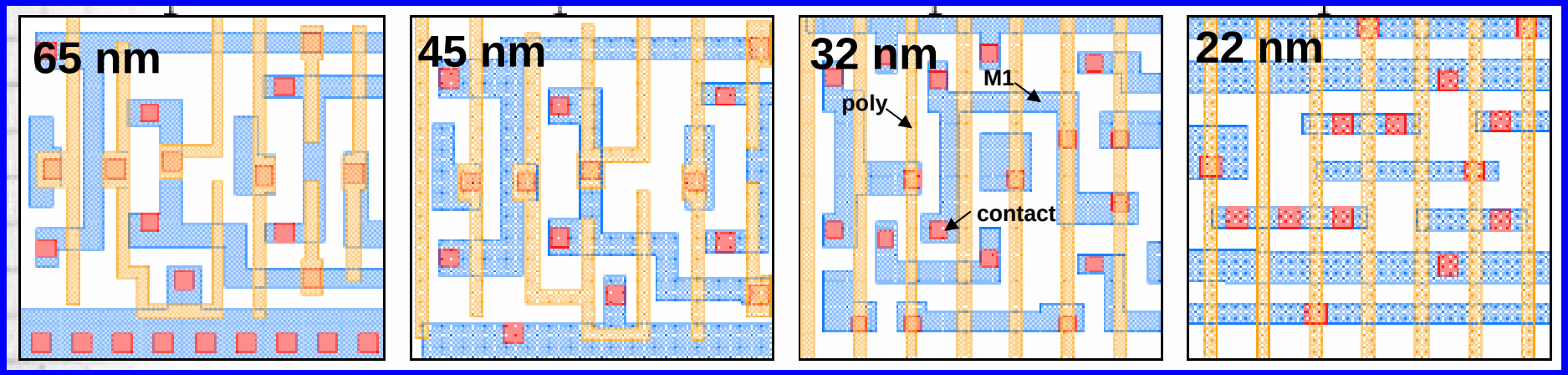
Extract, Seal

- No change to standard process flow for Cu
- Retain insulator beneath Cu lines for mechanical and thermal integrity
- Automated air-gap mask design

Lithography

B. Lin, CICC Proc., 2009

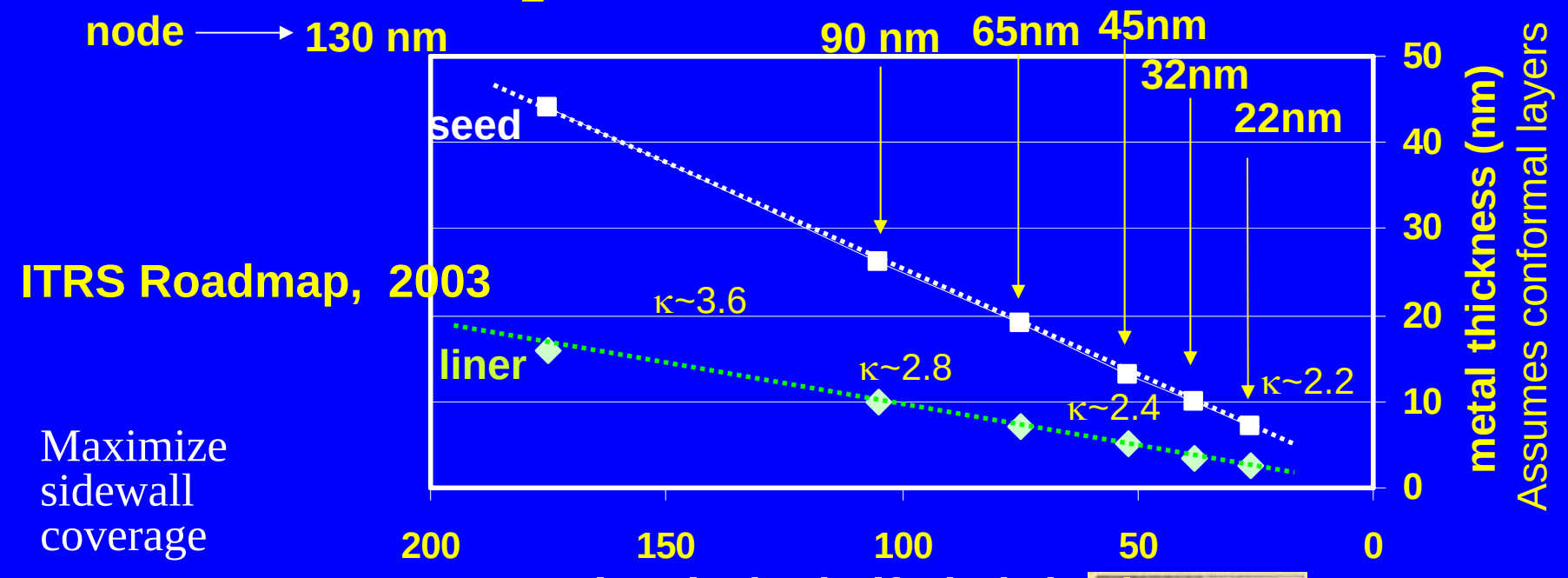
poly, contact, M1: more layout restrictions



Need to extend optical litho down to 22 nm node

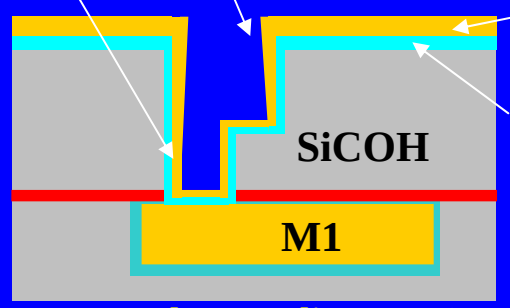
designs are on grid with single orientation

Roadmap for liner/seed thickness



Maximize sidewall coverage

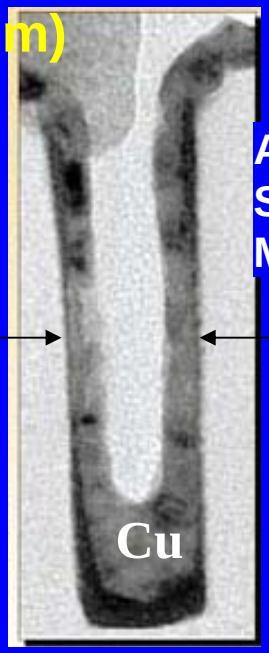
Minimize overhang



Seed; PVD Cu

Liner; PVD TaN/Ta
* Diffusion barrier
* Adhesion layer
* Redundant conductor

45 nm node: M1 liner = 4.0 nm; MX liner = 5.0 nm
32 nm node: M1 liner = 2.8 nm; MX liner = 3.5 nm
22 nm node: M1 liner = 2.0 nm, MX liner = 2.5 nm

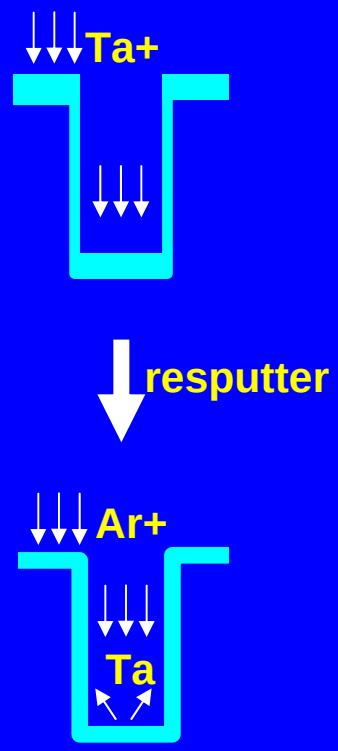


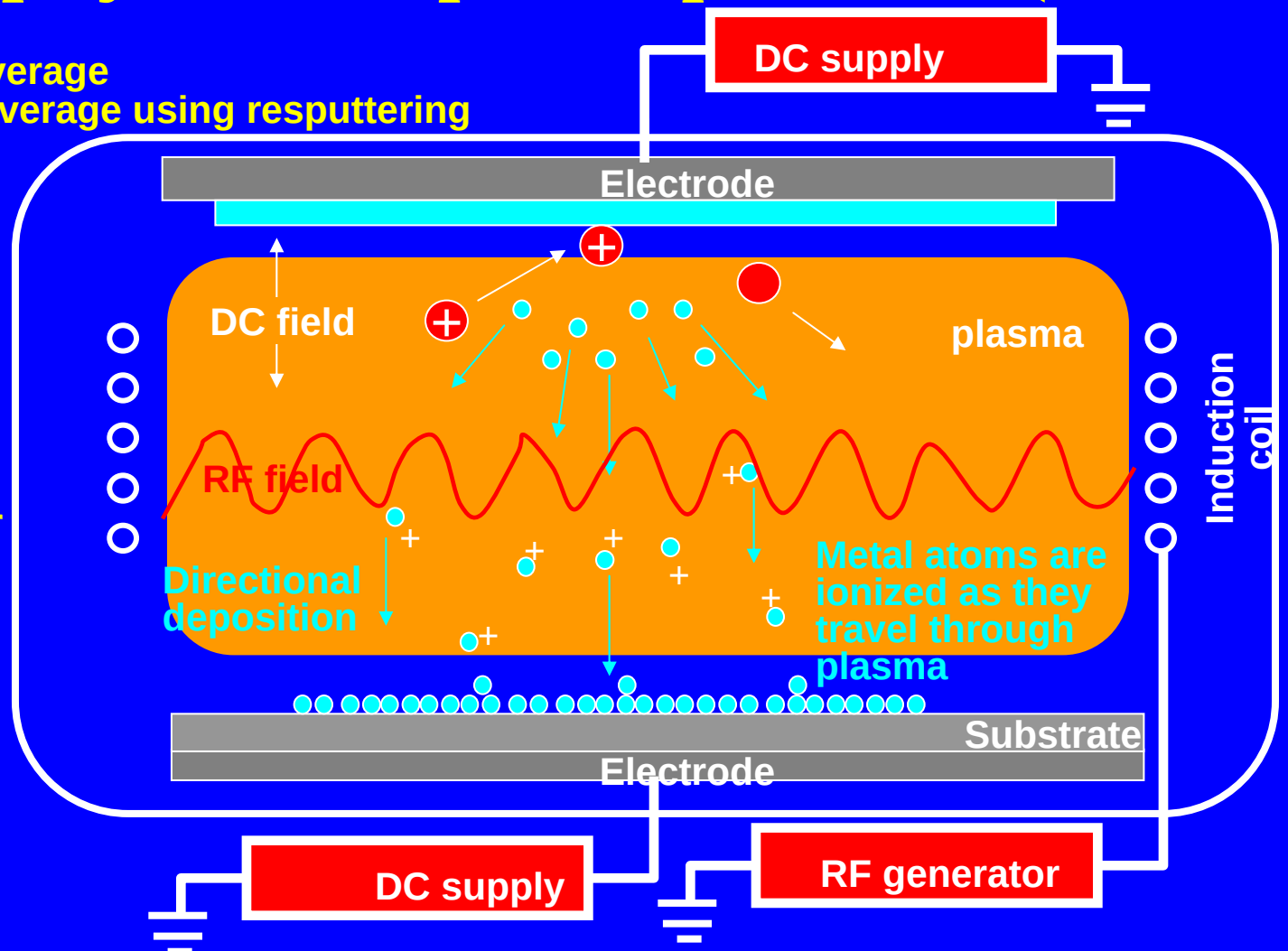
34 nm

A. Kumar et al., Semicond. Int., May. 2008, p. 26.

Ionized physical vapor deposition (I-PVD)

Advantages;
- **Better bottom coverage**
- **Some sidewall coverage using resputtering**



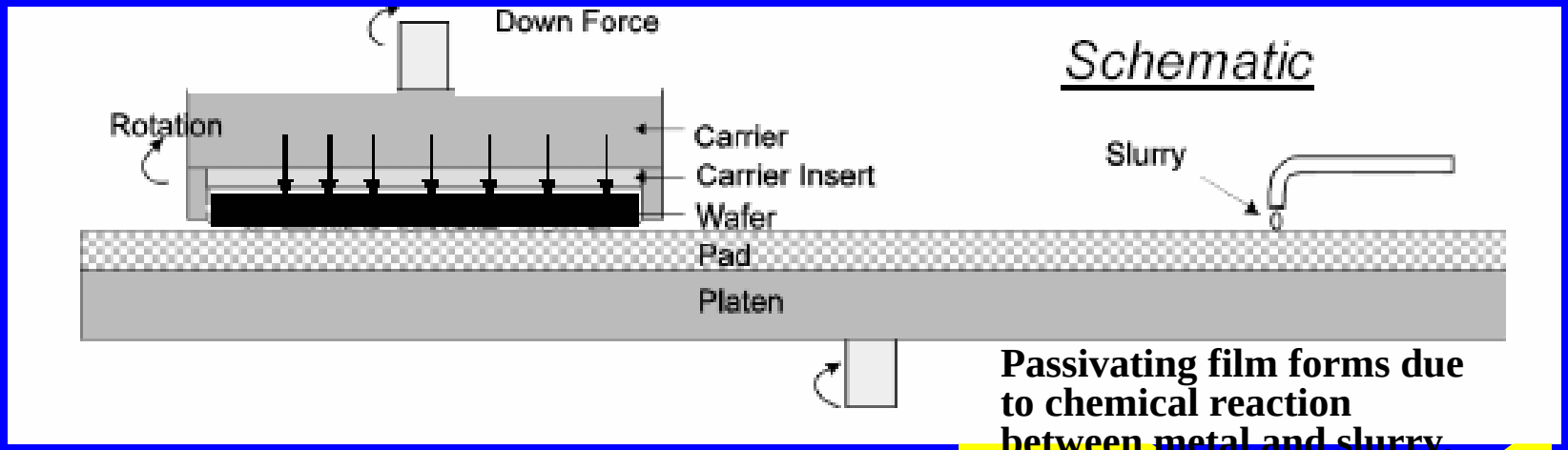


Methods based on ionized PVD:
SIP = self-ionized plasma
HCM = hollow-cathode magnetron

M. Quirk, J. Serda, "Semiconductor Manufacturing Technology, 2001, Chap. 12.

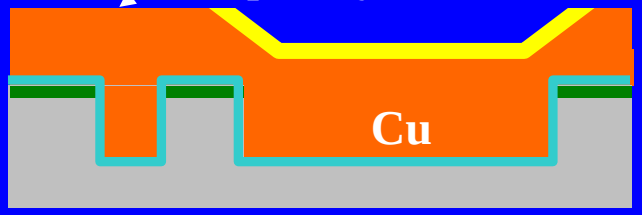
Chemical mechanical polishing (CMP)

M. Quirk, J. Serda, "Semiconductor Manufacturing Technology, 2001, Chap. 18.
W.Y. Hsu, IRPS Tutorial, 2004.



Passivating film forms due to chemical reaction between metal and slurry.

Film is removed from high spots by mechanical abrasion

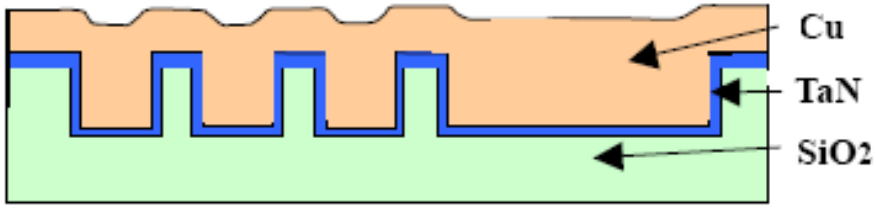
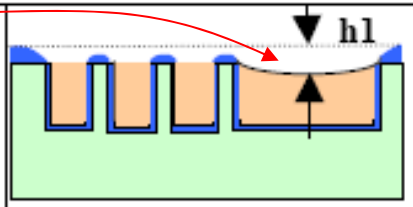
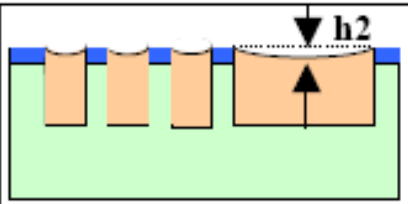
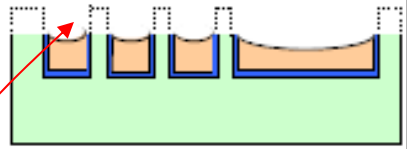
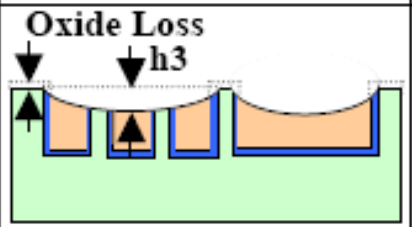
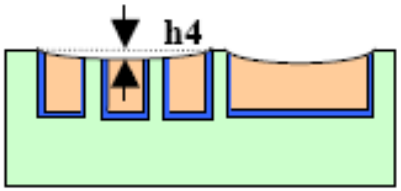


Process parameters:

- Pad type
- Slurry type
- Polish tool
  - Pressure (carrier and backside)
  - Velocity (carrier and platen)
  - Slurry flow rate
  - Temperature
  - Pad conditioner

CMP: insulator erosion and dishing

Y. Kamigata et al., MRS Proc., vol. 671, 2001, p. M1.3.1.

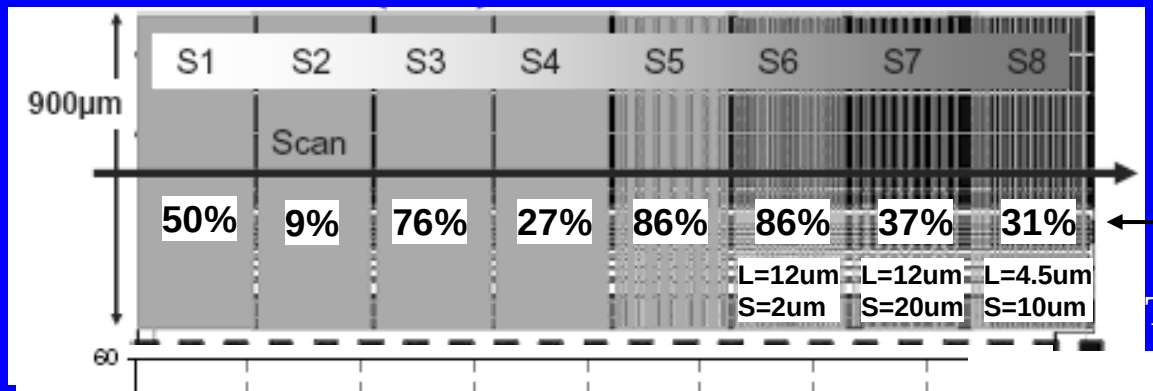
Selectivity	One Step CMP Cu/TaN/SiO2 = 1:1:1	Conventional Two Step Cu/TaN:High, TaN/SiO2 :Low	New Process Cu/TaN:Super High TaN/SiO2 : High	Remark
Initial				—
Cu-CMP	Dishing: Cu is removed in wide lines due to deformation of polish pad.			h1 >h2
TaN-CMP				h3 >h4
Issue	Insulator erosion: ILD is removed in regions with high metal pattern density due deformation of polish pad.	SiO2 Loss Large Dishing & Erosion	Stop on Barrier, Reduced Dishing, Erosion & SiO2 Loss	—

E-CMP: reduced erosion and dishing

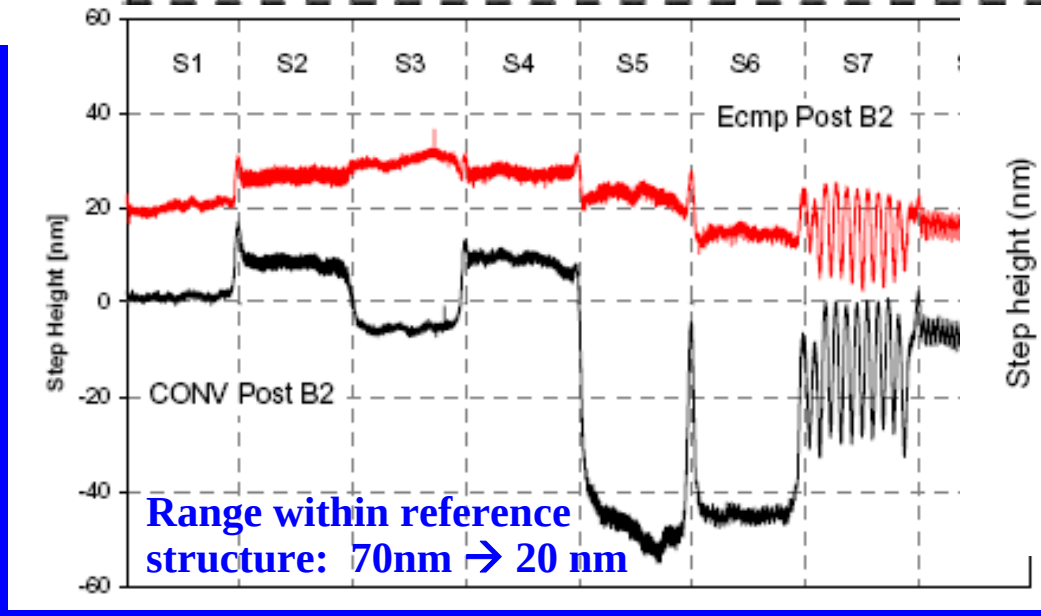
E-CMP = electro-chemical mechanical polishing

M. Mellier et al., IITC, 2007, p. 70.

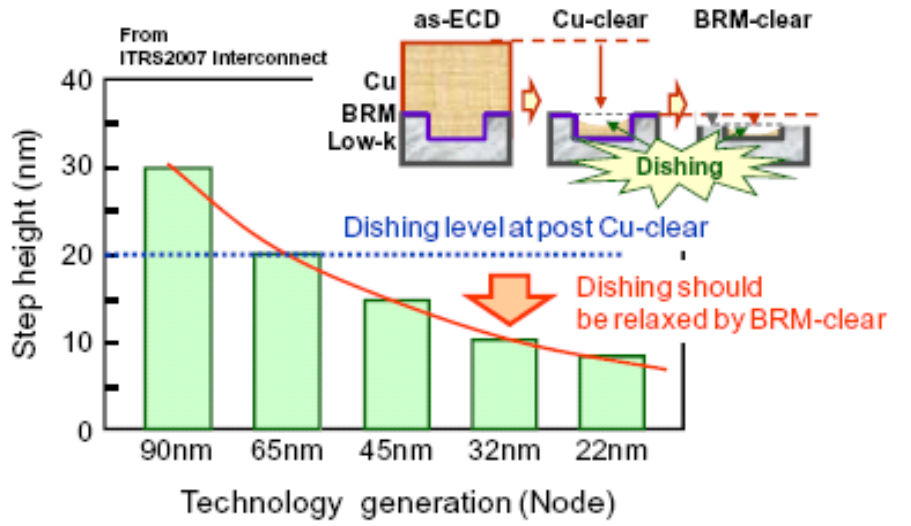
Improved local and global planarity.
Reduce variability in resistance.
Improved process window for litho.



T. Kanki et al., IITC Proc., 2007, p. 79.



Range within reference structure: 70nm → 20 nm



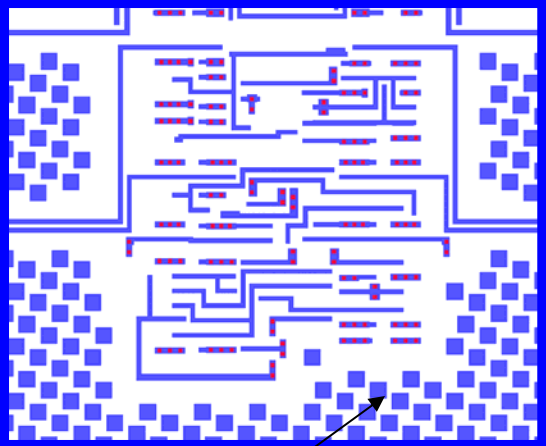
BRM = barrier metal

Cu Hole and Fill shapes

H. Landis, J. Sucharitaves, AMC Proc., 2006.

Guidelines for Dummy Shapes:

1. Big enough to resolve easily
2. Small and electrically isolated
3. Density → center of the process window
4. Place FILL shapes everywhere they fit

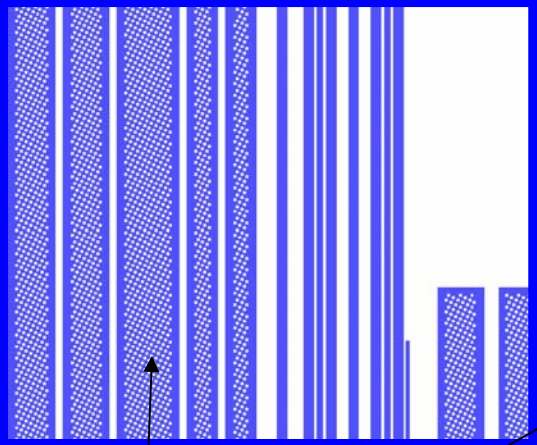


Cu Metal FILL

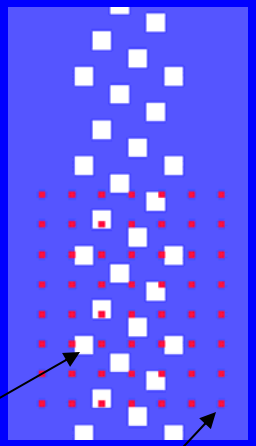
Improve CMP uniformity by adding holes in wide lines and dummy metal shapes during data prep

Metal HOLE issues

- Reduced conductivity
- Critical via interactions
- Design requirements (less holes)
- Manufacturability (more holes)



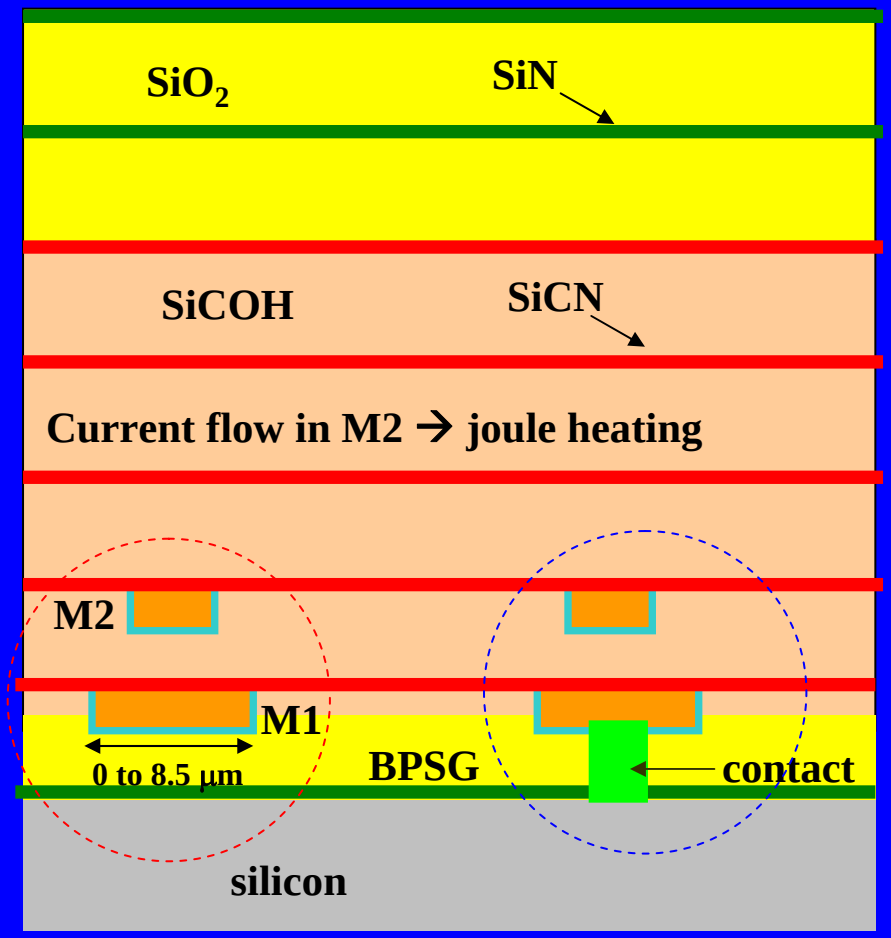
Cu Metal "Holes"



Vias

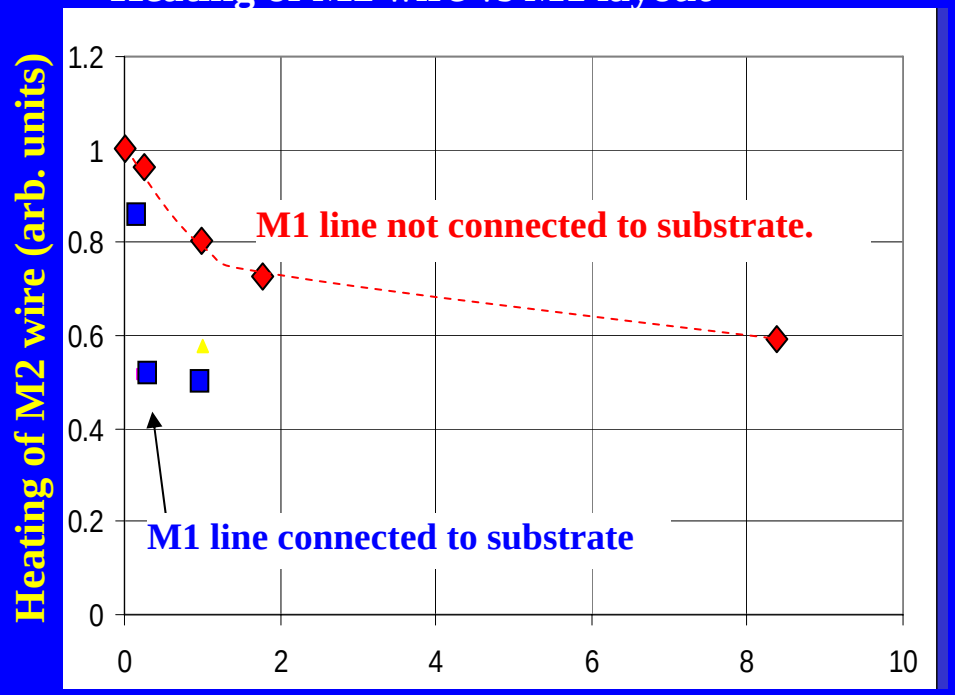
Effect of layout on interconnect heating

A. Strong, F. Chen, IRW, 2004.

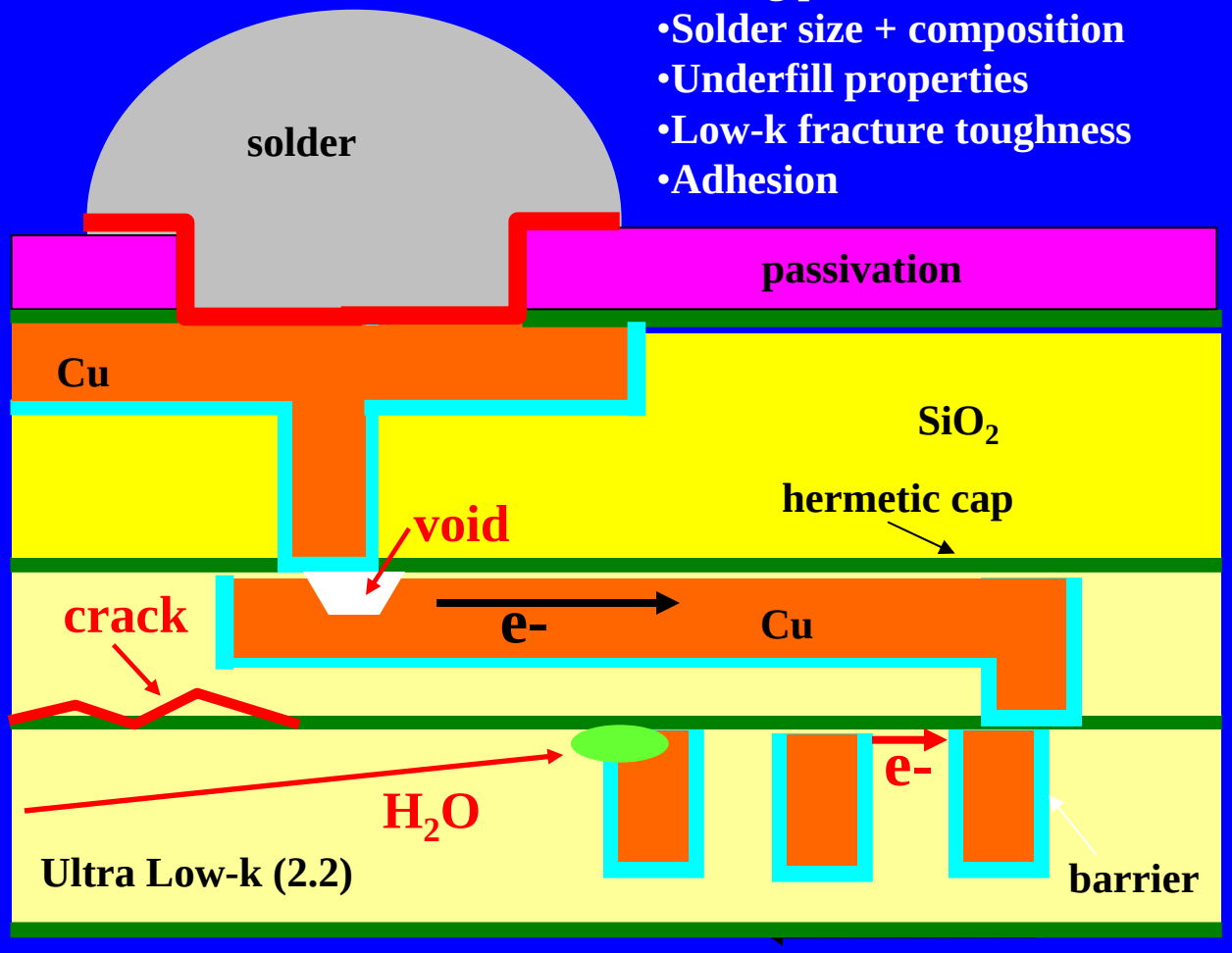


Thermal conductivity:
SiO_2 = 1.0 W/m-K
SiCOH = 0.4 to 0.6 W/m-K
p-SiCOH = 0.2 W/m-K

Heating of M2 wire vs M1 layout



Interconnect scaling: reliability



Cracks
- Dicing process
- Solder size + composition
- Underfill properties
- Low-k fracture toughness
- Adhesion

Cu oxidation
- Dicing process
- Cap layer integrity
- Low-k porosity

Voids in copper
- Cu fill
- cap layer adhesion
- Pattern fidelity
- Low-k damage
- Barrier integrity

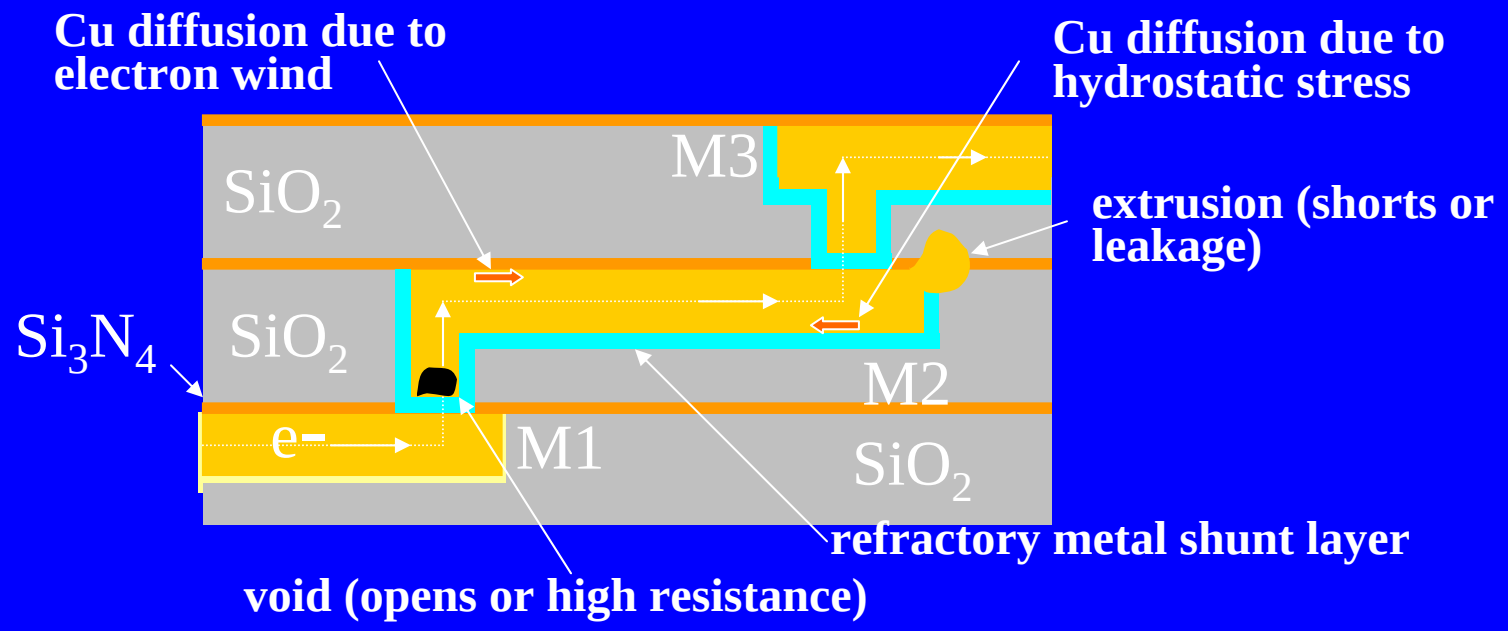
Dielectric breakdown
- Pattern fidelity
- Low-k damage
- Barrier integrity
- Contamination

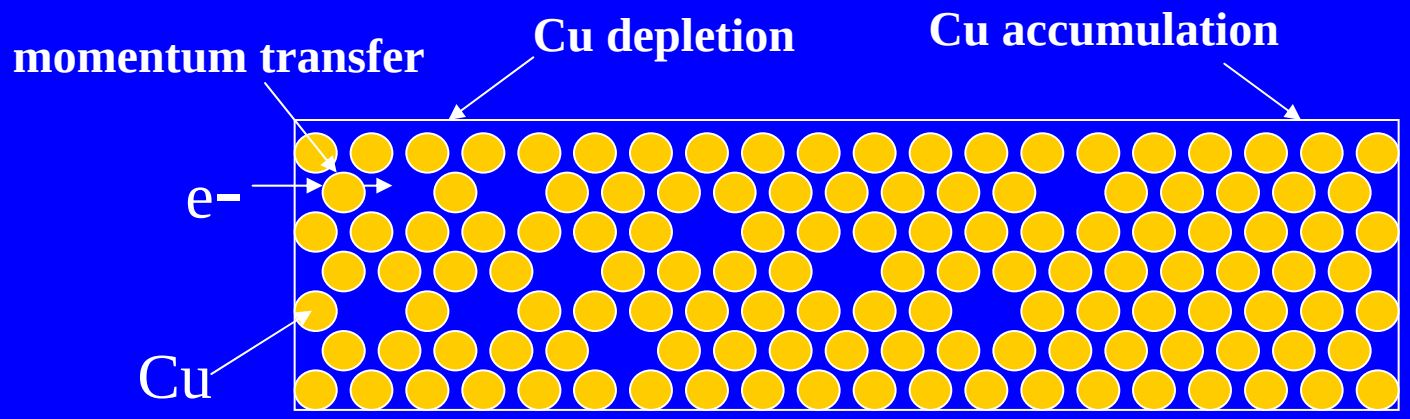
Outline

- Copper interconnect scaling
- Copper interconnect reliability
  - Electromigration
  - Stress-induced voids
  - Time Dependent Dielectric Breakdown
- Packaging
- Passive devices

Electromigration basics

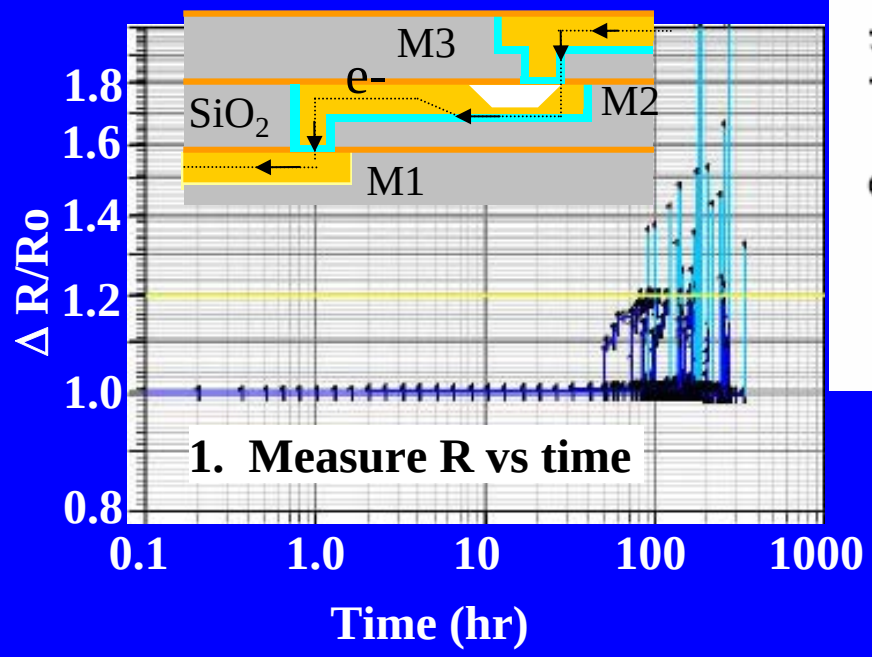
T. Sullivan, Int. Reliability Workshop, 2001
D. Pierce, P. Brusius, Microelec. Rel., 37, 1053 (1997)

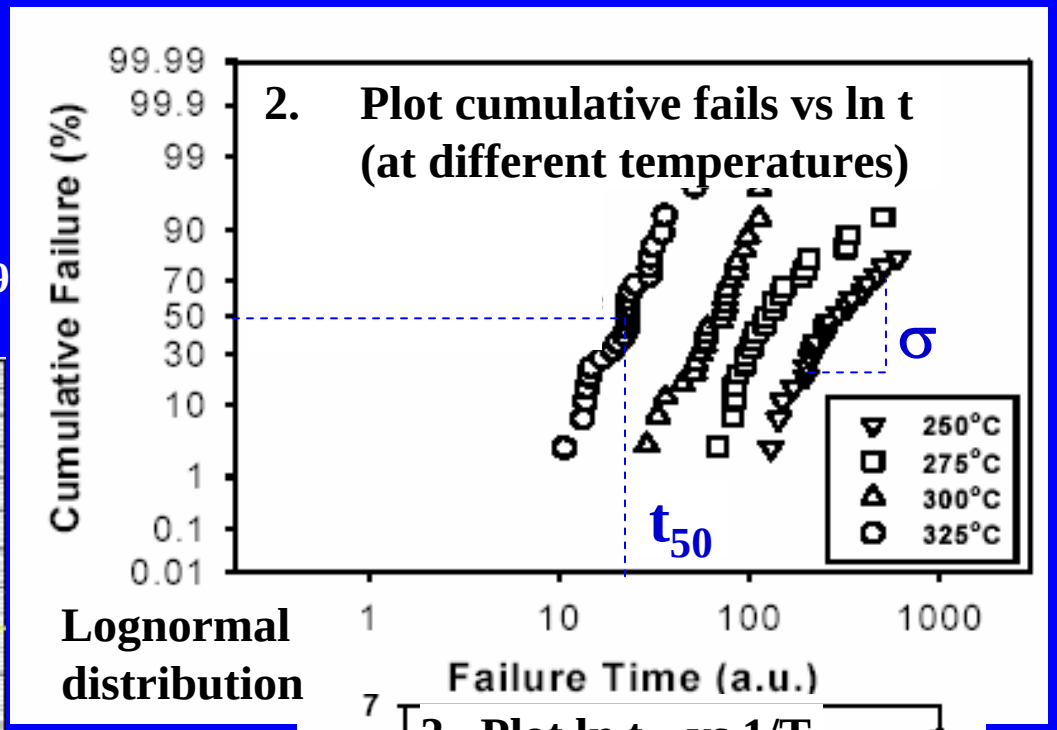




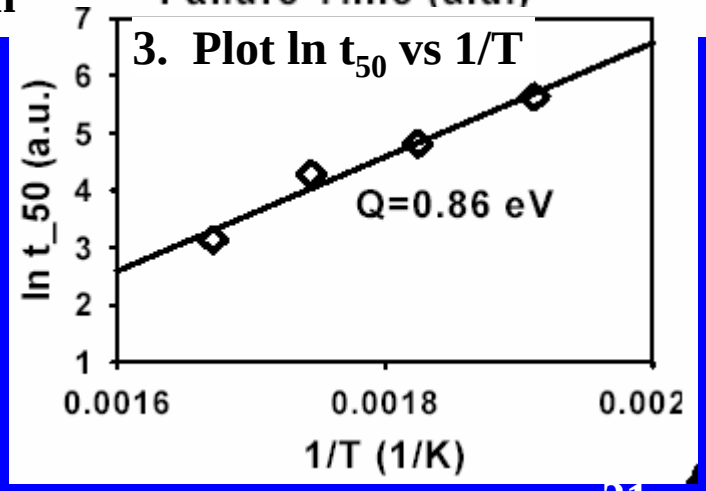
Electromigration test

Y.-J. Park, IRPS tutorial, 2006.
J.R. Black, Proc. IEEE, 57, 1587 (1969





Lognormal distribution



Activation energy for diffusion

Black's Law: $t_{50} = c \cdot j^{-n} \exp\left(E_a / kT\right)$

median time to fail

current density

Kinetics of electromigration

Fast diffusion path:
Cu – SiCN interface

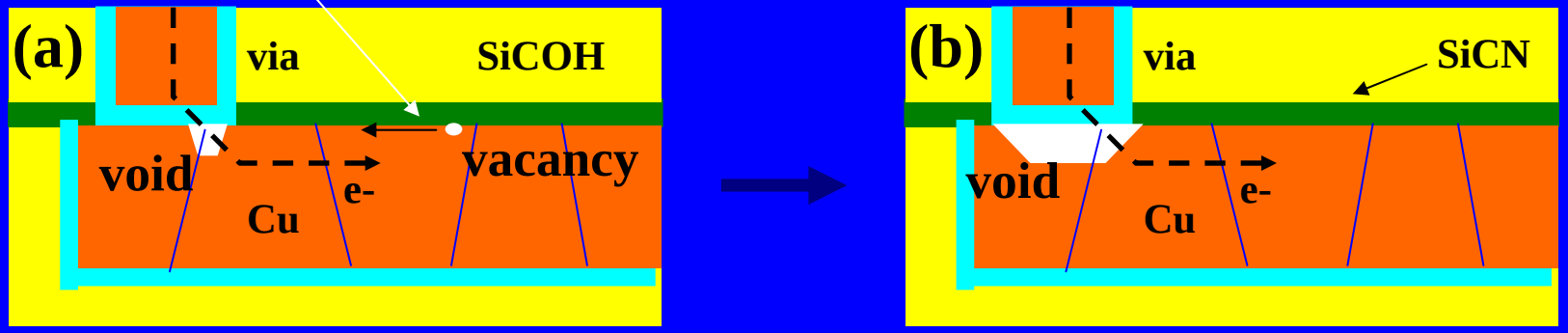
current exponent

$$t_{50} = c \cdot j^{-n} \exp\left(E_a / kT\right)$$

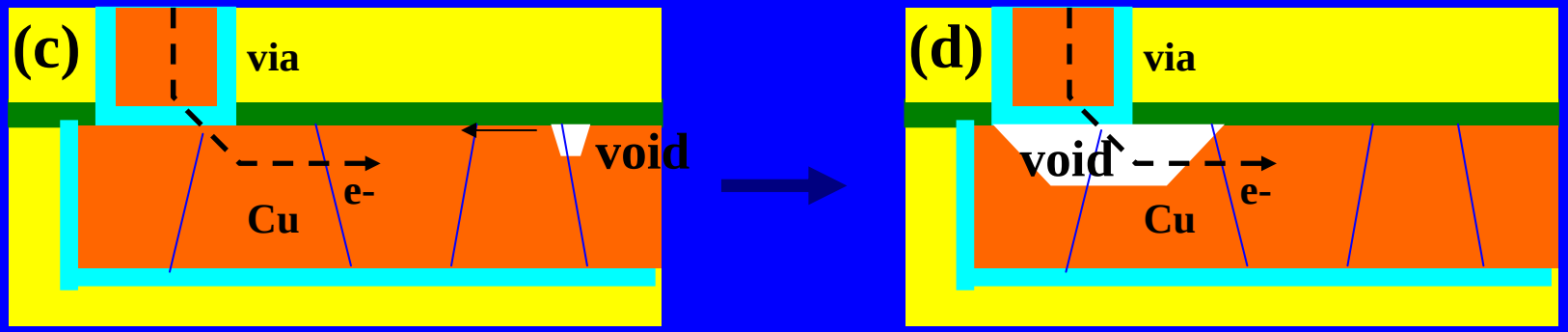
median time to fail

current density

Kinetics limited by void nucleation (n=2)

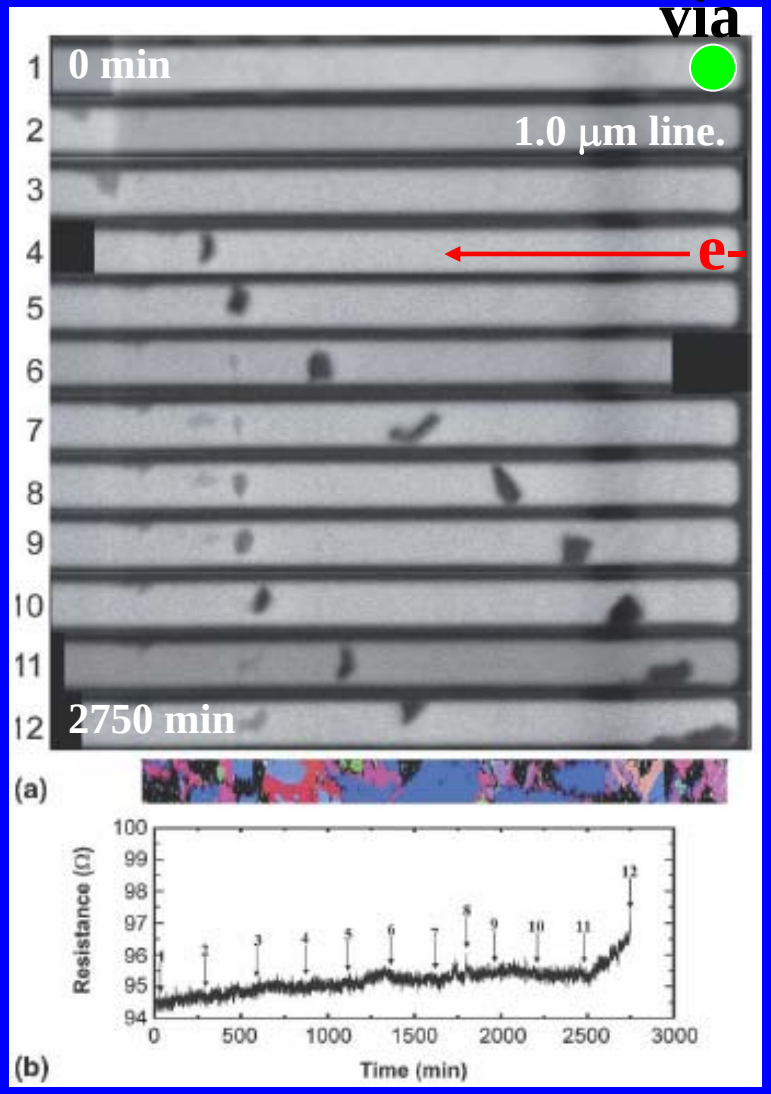


Kinetics limited by void growth and migration (n=1)

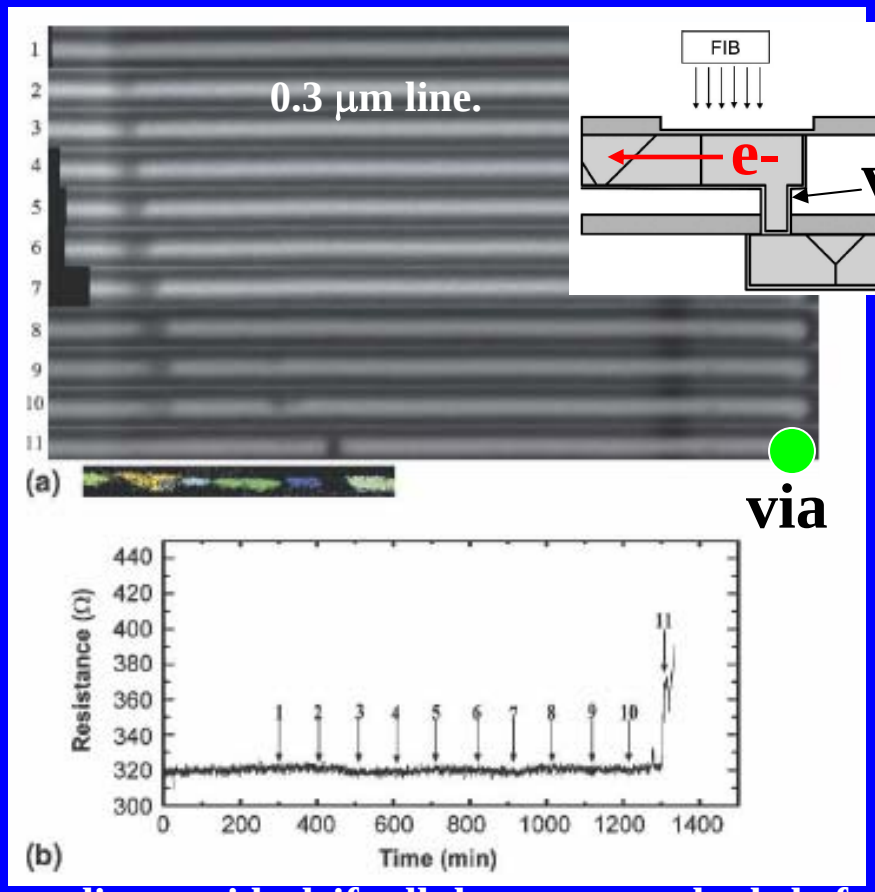


In-situ SEM of electromigration

370°C, 3 mA/cm^2



Z.-S.. Choi et al., J. Mater. Res., vol. 23, 387 (2008).



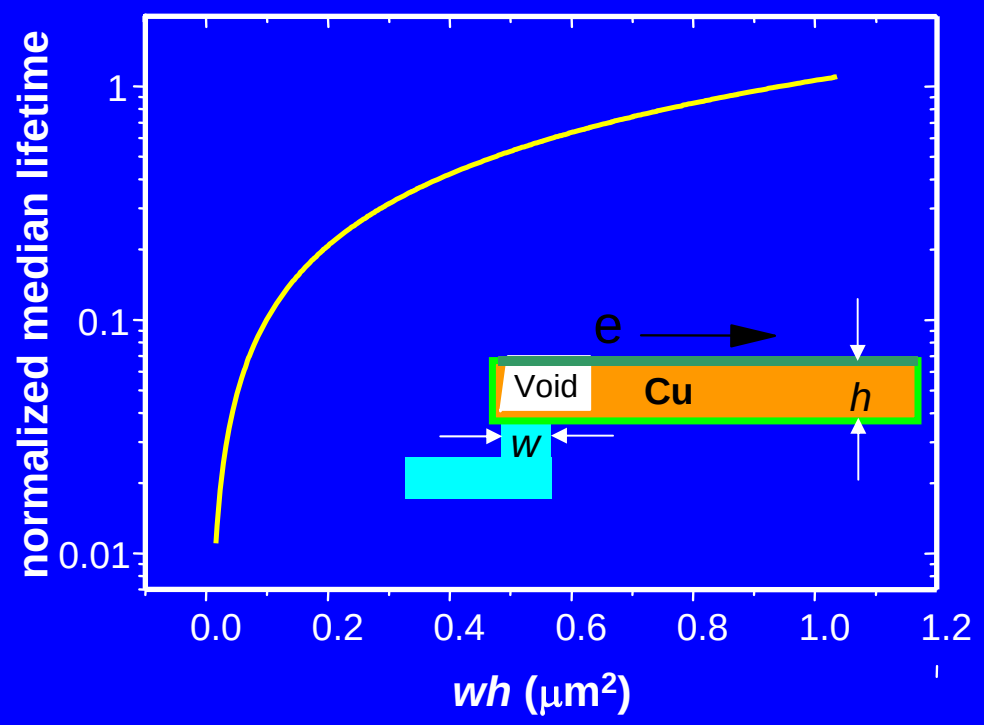
1.0 μm line; voids drift all the way to cathode before fail occurs

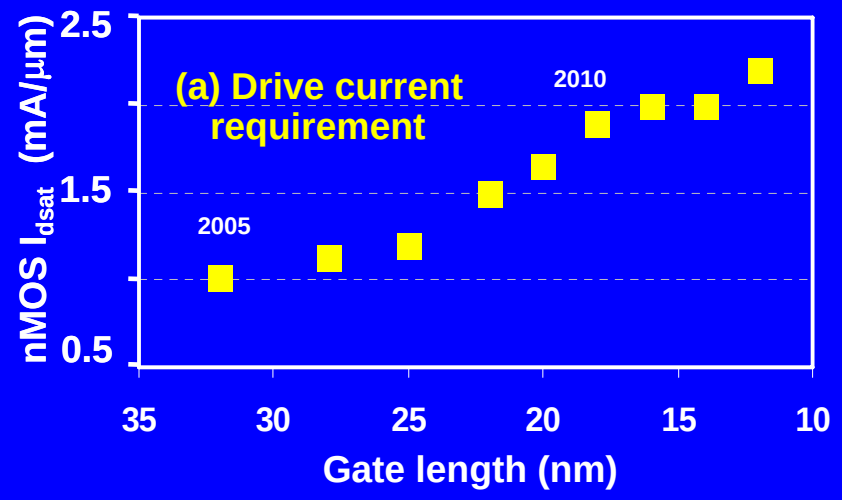
0.3 μm line; voids drift only 1 to 2 um before being pinned at g.b., then span line, causing a fail

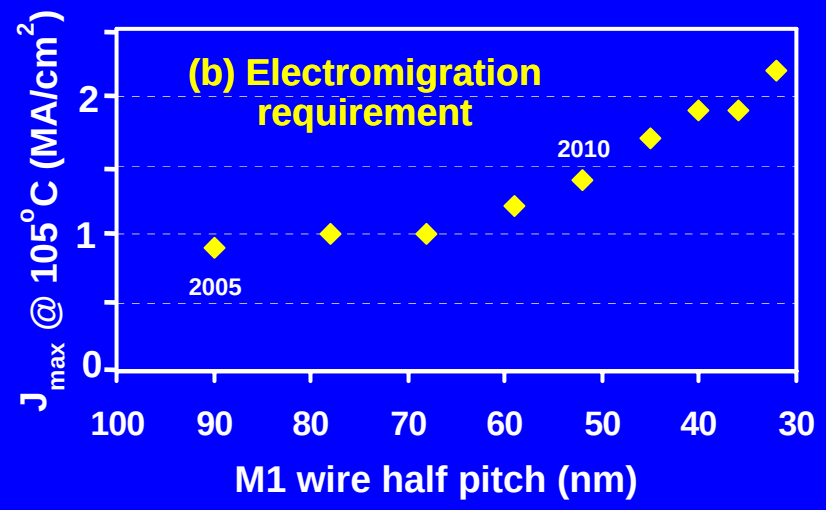
Effect of scaling on EM

2005 ITRS roadmap:
http://public.itrs.net/

C.K. Hu et al., IRPS Proc., 2004, p. 222.





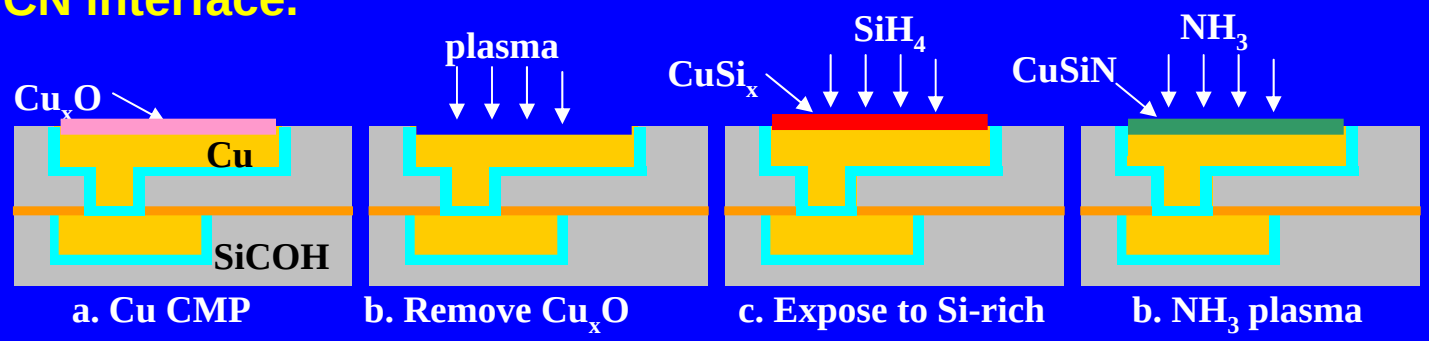


Methods to improve EM lifetime

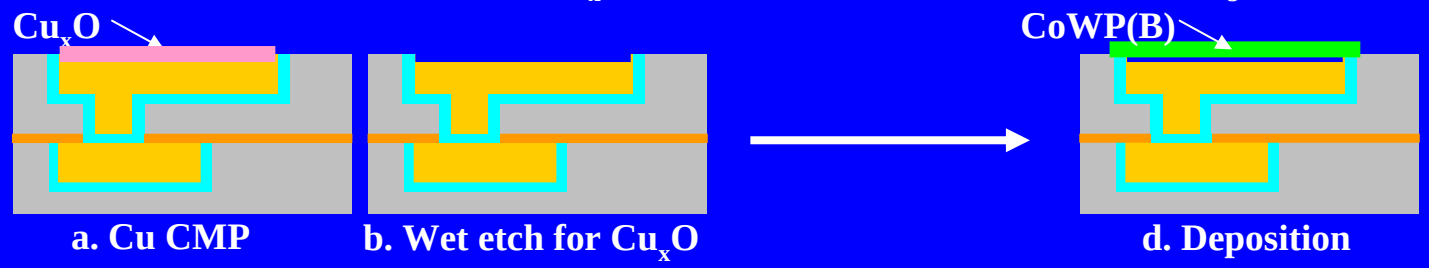
Shut down fast diffusion path at Cu-SiCN interface.

L. Gossett et al., IITC 2006, p. 84.
C.K. Hu et al., Appl. Phys. Lett., 2003, p. 869.

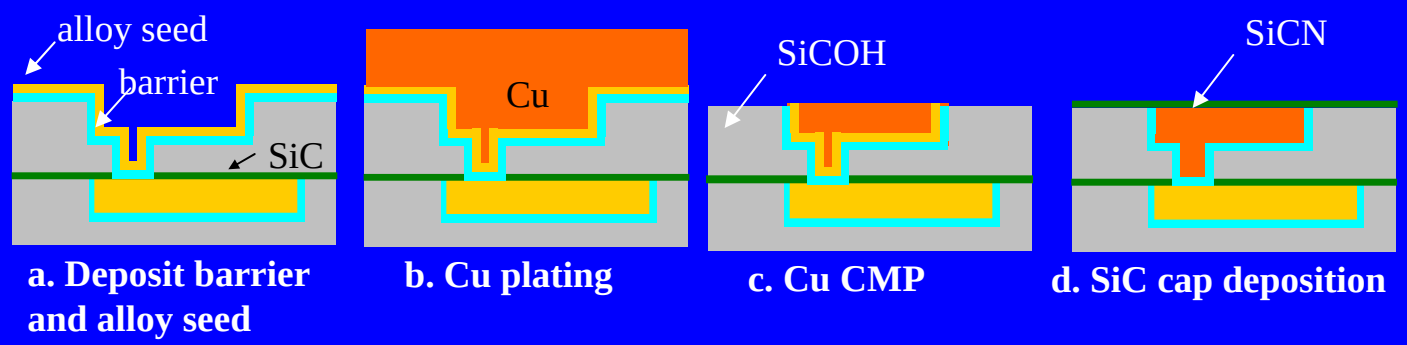
1. CuSiN formed by SiH_4 exposure



2. Self-aligned metal cap by electroless plating



3. Alloy-seed layer

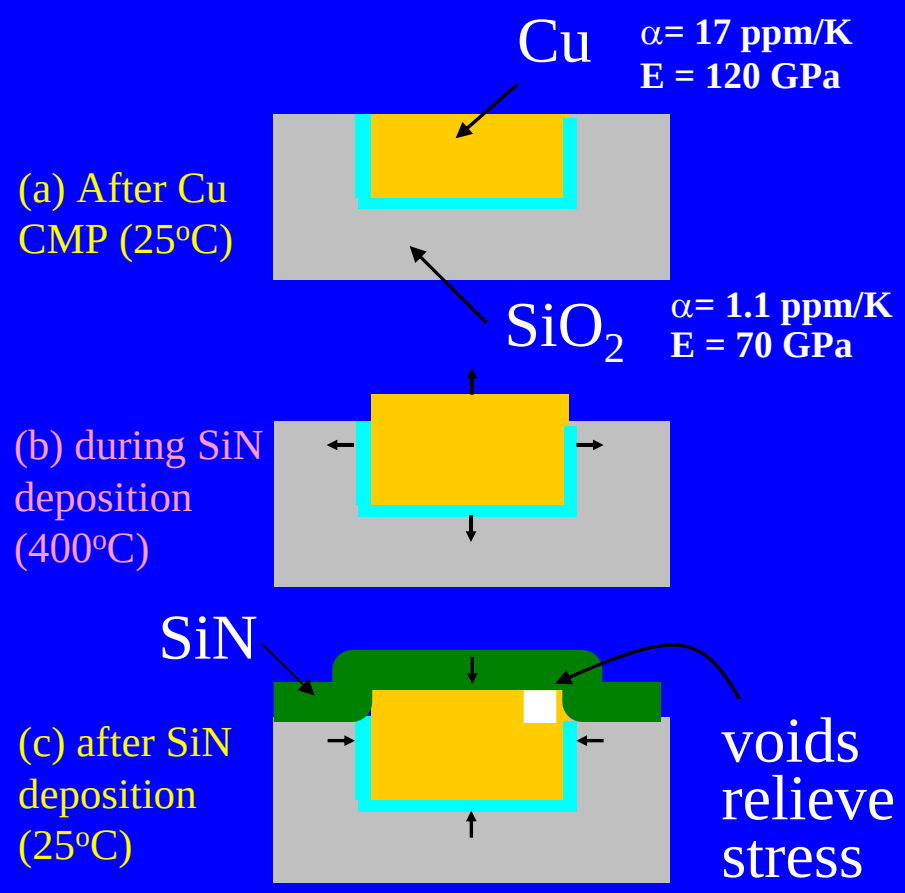


Outline

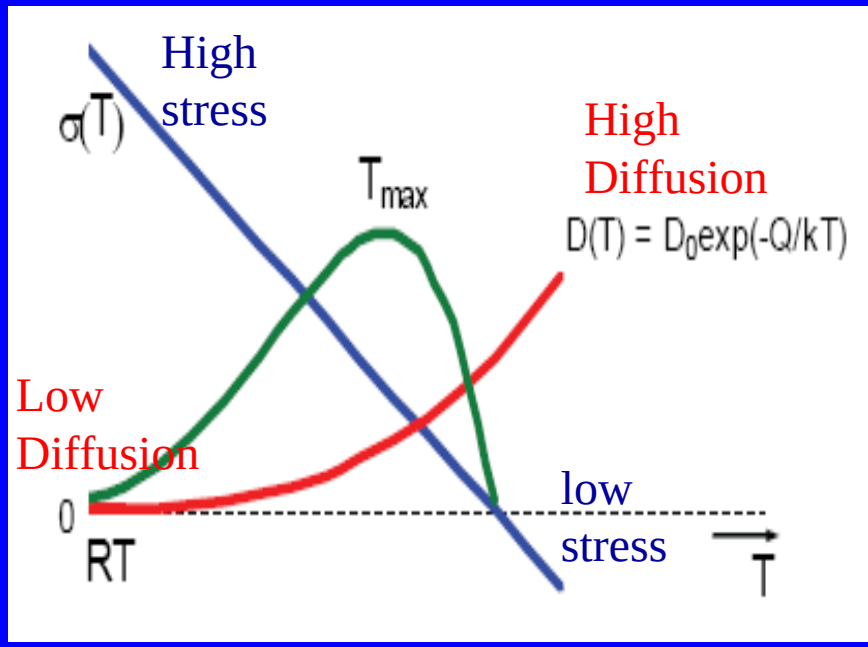
- Copper interconnect scaling
- Copper interconnect reliability
  - Electromigration
  - Stress-induced voids
  - Time Dependent Dielectric Breakdown
- Packaging
- Passive devices

Stress-induced voids in Cu

T. Sullivan, in Stress Induced Phenomena in Metallization, 1999, p. 39.
M. Hommel, IRPS Tutorial, 2008.



Highest fail rate is at intermediate temperatures

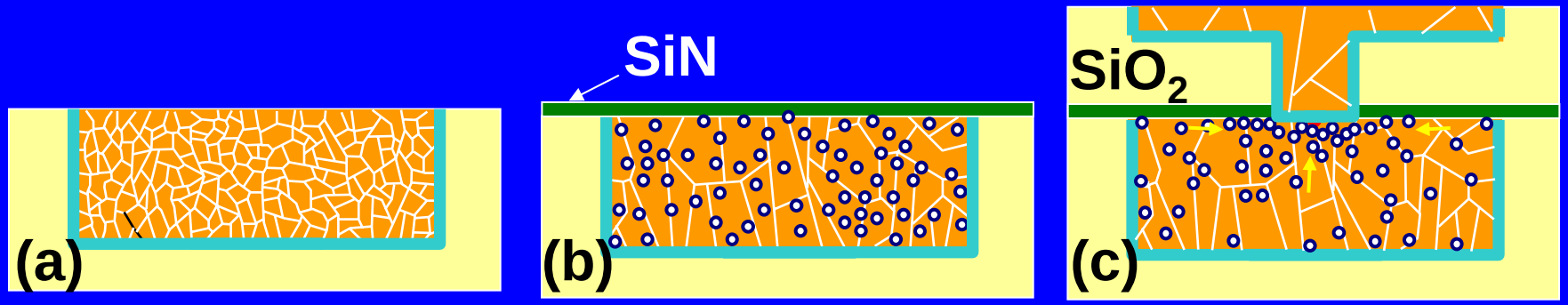


$$\sigma_o = E_{eff}\,\Delta\alpha\left(T_{dep} - T_{stress}\right)$$

bulk modulus of metal **CTE difference**

Stress-induced voids: confined grain growth

E. Ogawa et al., Int. Rel. Phys. Symp., 2002, p. 312.

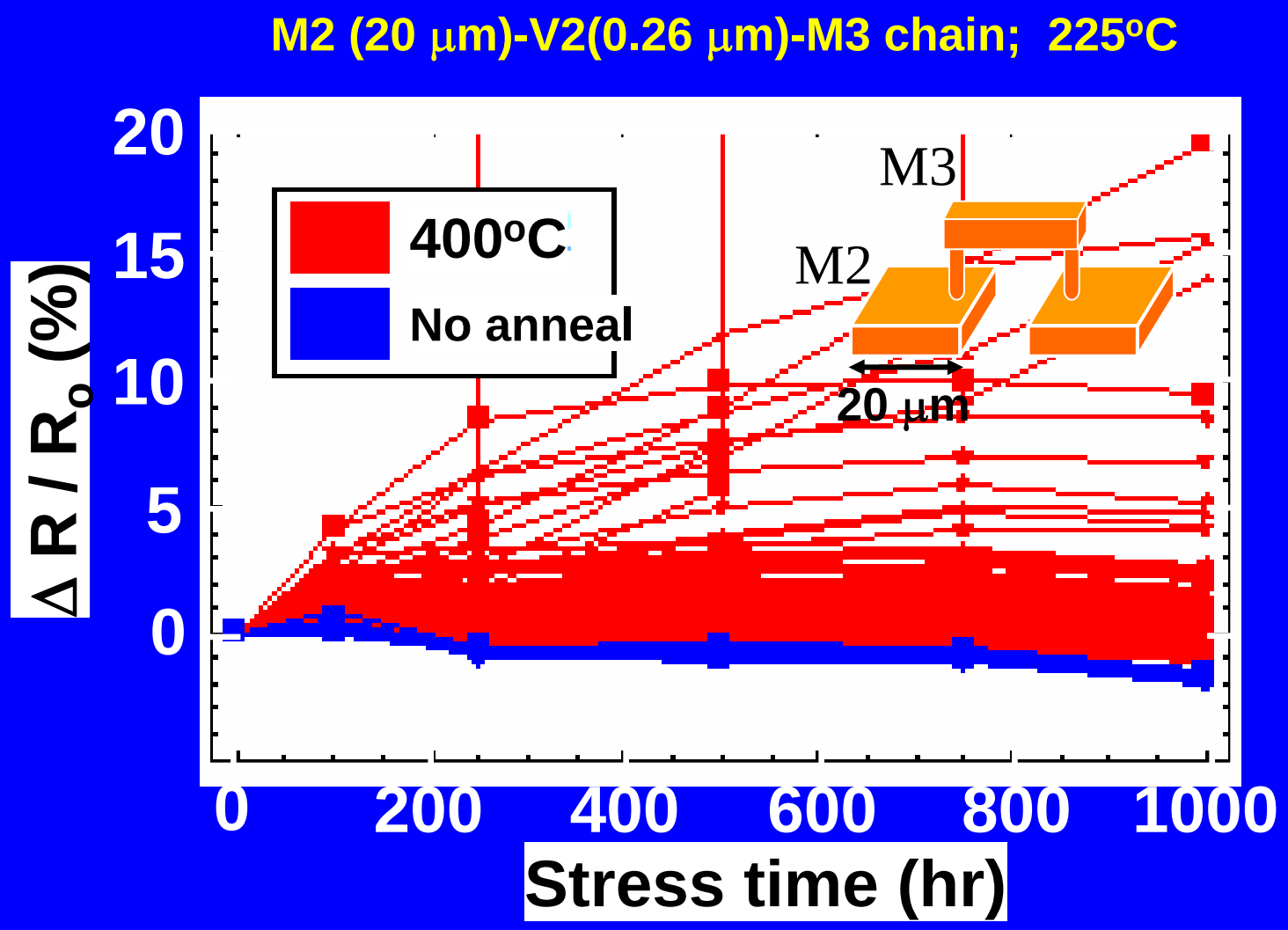


a. M1 Cu deposition + CMP (no anneal)

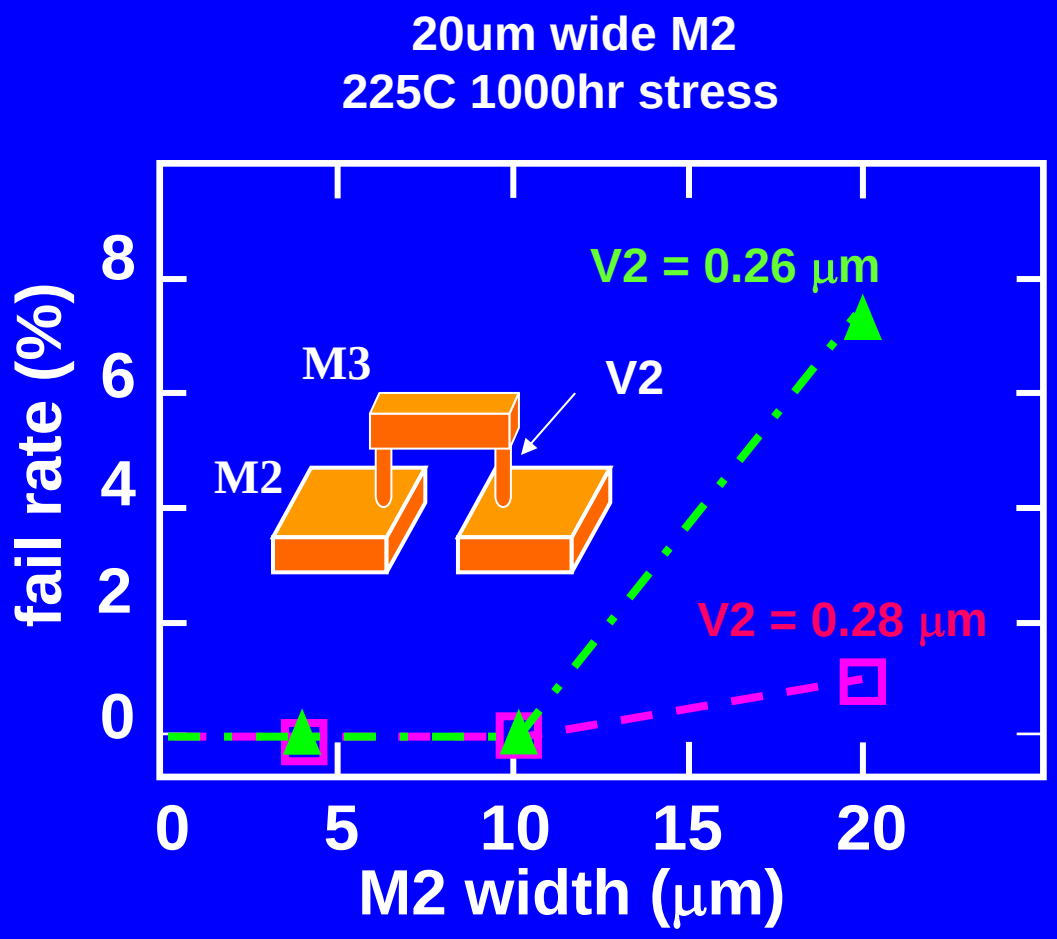
b. After cap deposition; metal is saturated with vacancies due to grain growth.

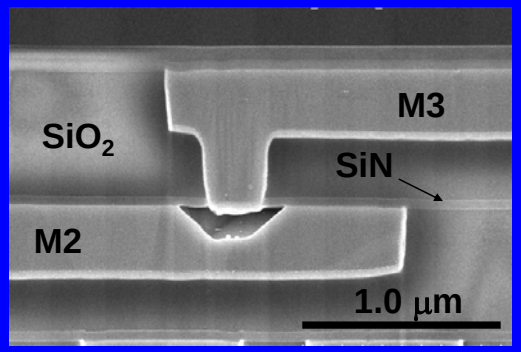
c. After via and M2 metal formation; void nucleates under via due to high tensile stress; void growth occurs by diffusion of vacancies along Cu-SiN interface.

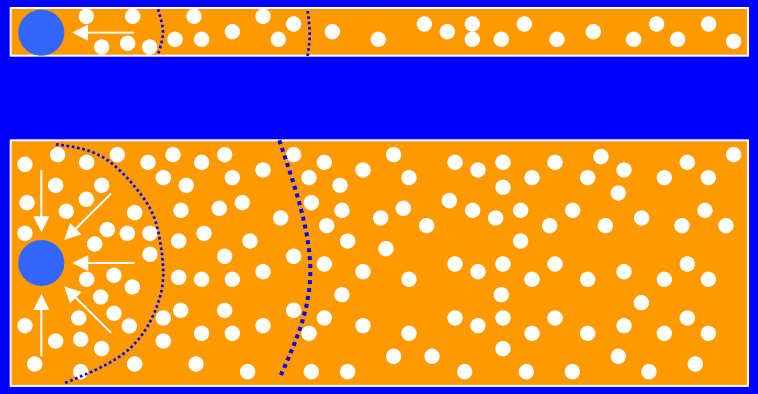
Stress-induced void measurement



Fail rate for stress-induced voids as a function of via size and line width.





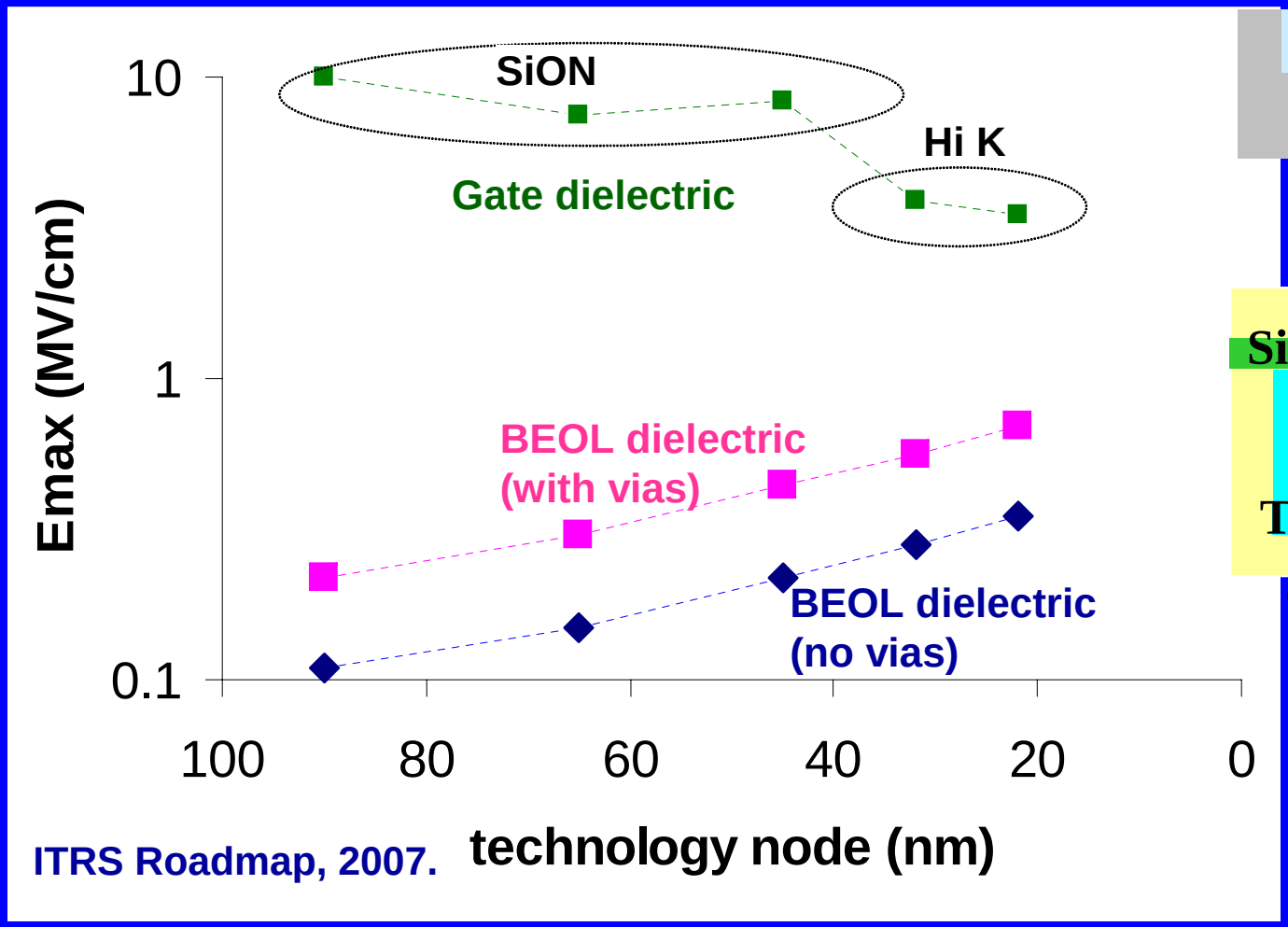


$$x_D \approx \sqrt{D^* t}$$

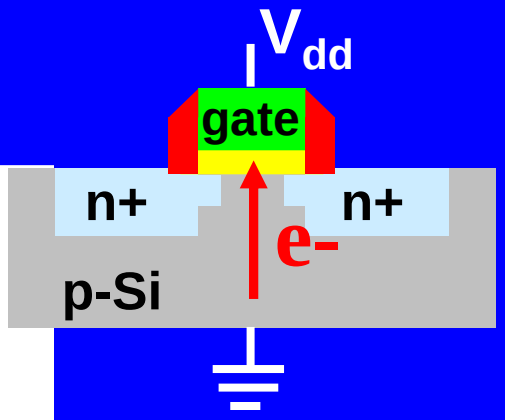
Outline

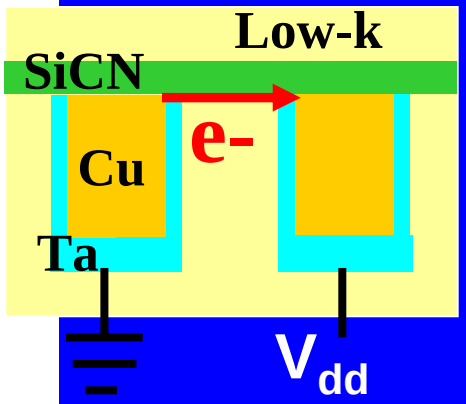
- Copper interconnect scaling
- Copper interconnect reliability
  - Electromigration
  - Stress-induced voids
  - Time Dependent Dielectric Breakdown
- Packaging
- Passive devices

Effect of scaling on electric field



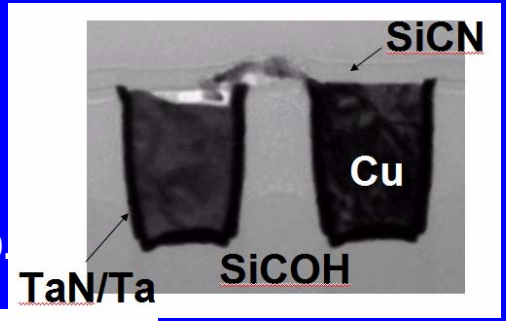
ITRS Roadmap, 2007.

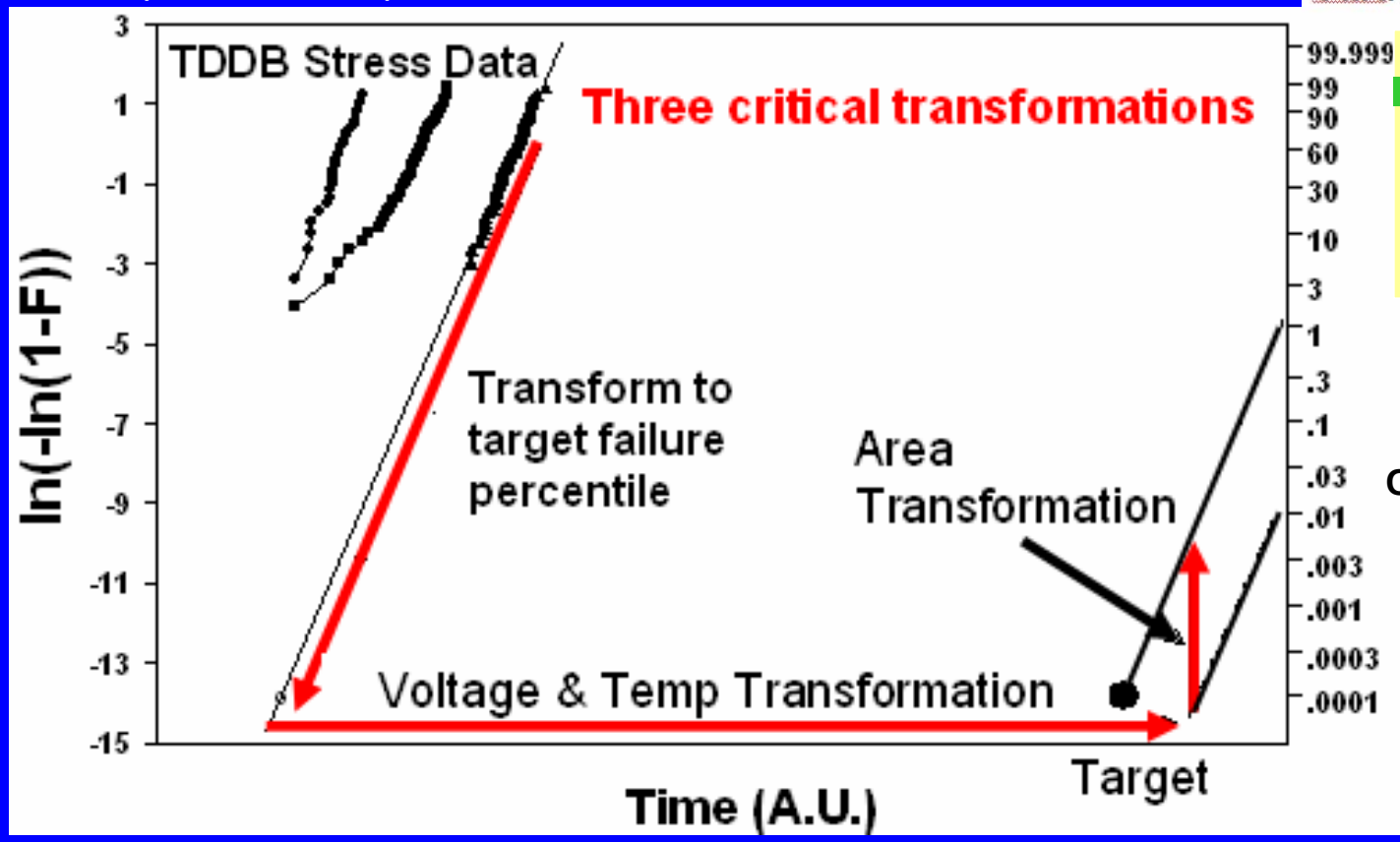


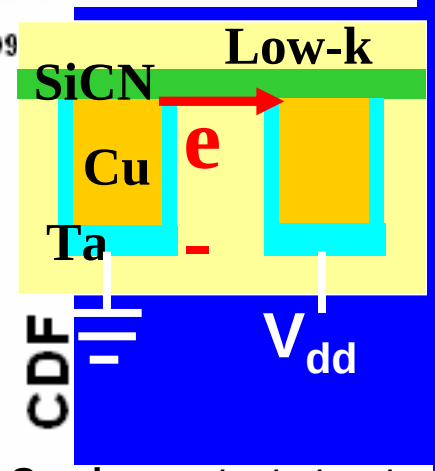


TDDB testing

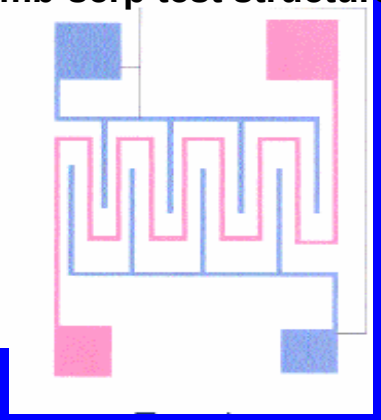
J. McPherson, in Handbook of Semiconductor Manufacturing, 2000, p. 959.
F. Chen, IRPS tutorial, 2008.







Comb-serp test structure



Test at high fields to accelerate fails.
Extrapolate to use conditions (low fields) using reliability model.
Leading models for BEOL TDDB. “E-model” and “Sqrt-E model”

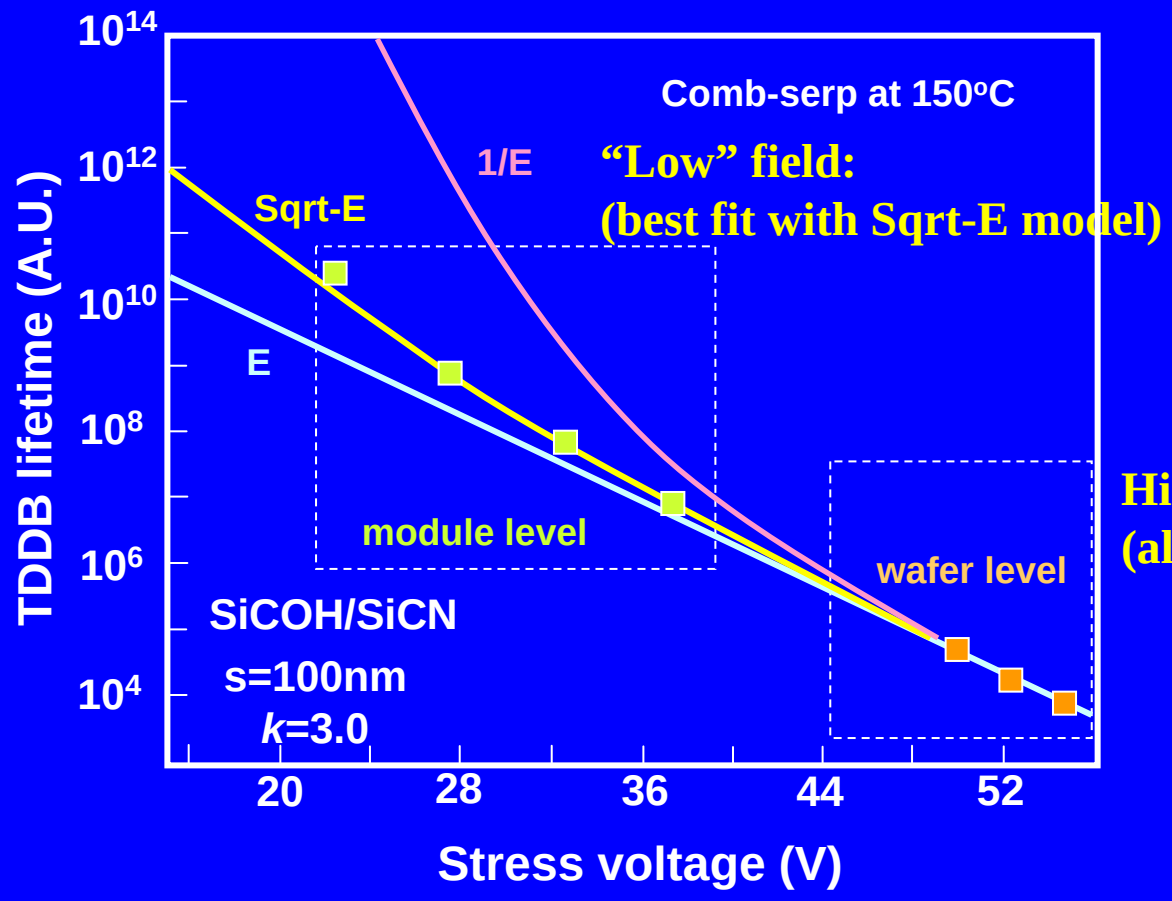
TDDB : E-model vs Sqrt-E model

$$\tau_{BD} = a \exp\left[-\left(\Delta H / kT\right)\right] \exp\left[-\gamma(T) E_{ox}\right]$$

E-model (ln lifetime α E)

$$\tau_{BD} \propto \exp\left[\frac{1}{k_B T}\left(E_D + 2\varphi - 2\beta\sqrt{E}\right)\right]$$

Sqrt-E-model (ln lifetime α $E^{1/2}$)



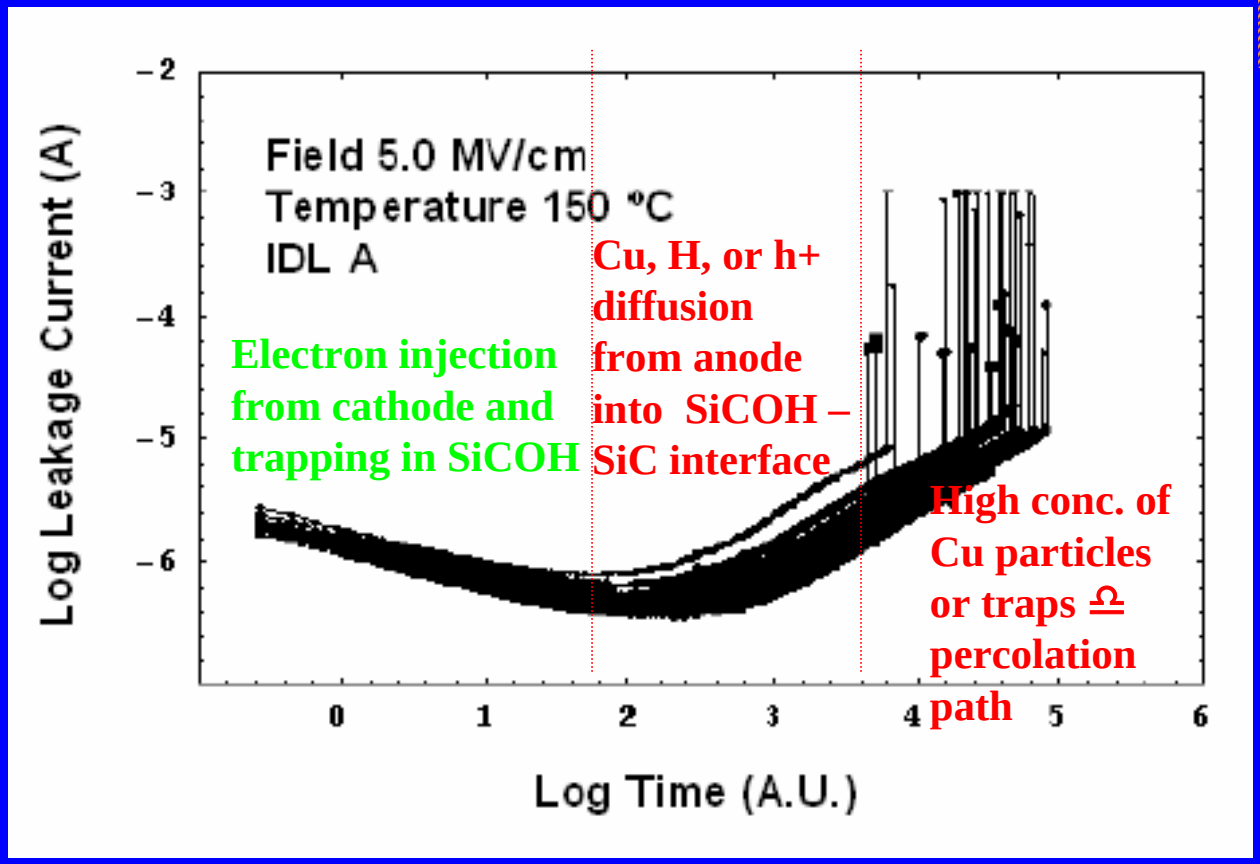
"Low" field:
(best fit with Sqrt-E model)

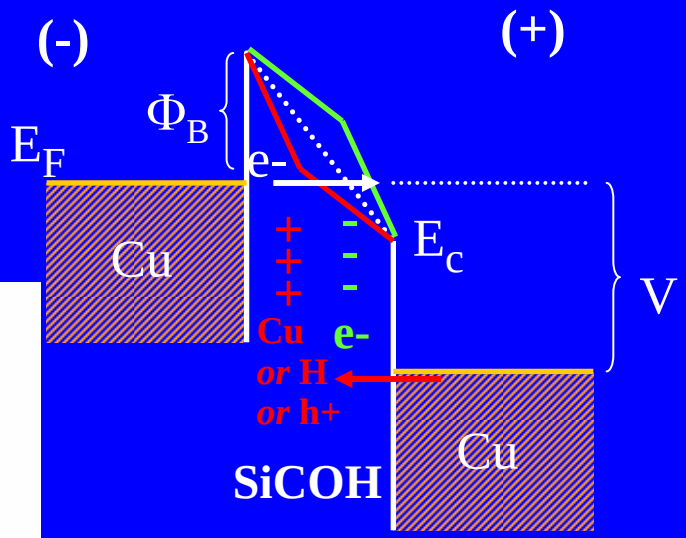
High field:
(all models fit the data)

F. Chen et al., IEEE IRPS 2006, p.46

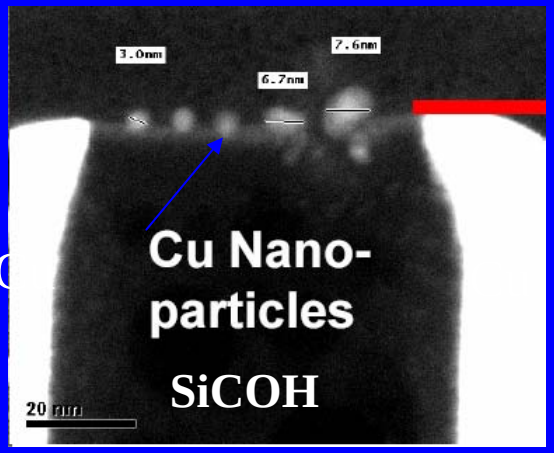
TDDB mechanism; SiCOH dielectric

F. Chen et al. Int. Rel. Phys. Symp., 2005, p. 501
G. Hasse et al., Int. Rel. Phys. Symp. 2005, p. 466.





Dark-field STEM image after TDDB stress



Outline

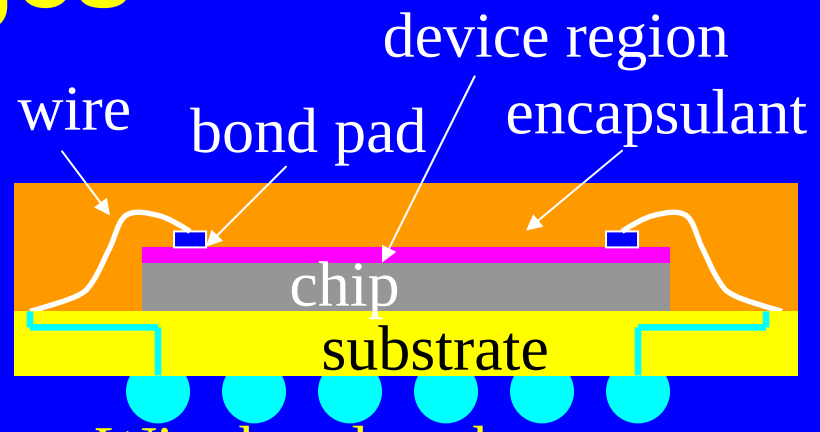
- Copper interconnect scaling
- Copper interconnect reliability
- Packaging
- Passive devices

Packaging challenges

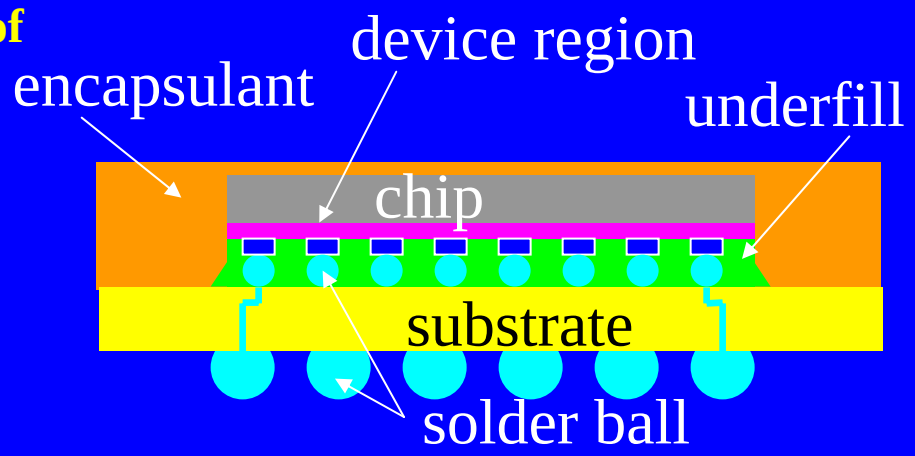
ITRS 2007

Effect of Cu/ low-k on packaging
- **Direct wire bond or bump to Cu**
- **Dicing for ultra low-k dielectric**
- **Pb-free bump and underfill technology compatible with low-k**
- **Improved fracture toughness and adhesion of low-k**
- **Probing over Cu/ low-k**

Thinned die packaging
- **Wafer / die handling**
- **Different carrier materials (organics, silicon, ceramics, glass, laminate core)**



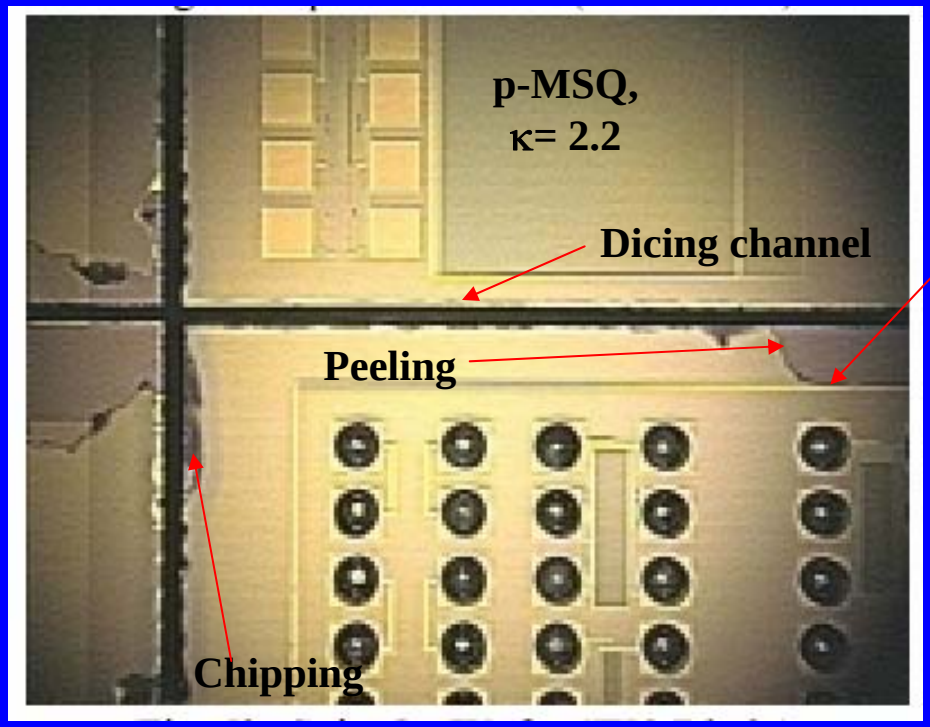
Wire bond package
* Low cost (for I/O < 500)
* Low I/O density

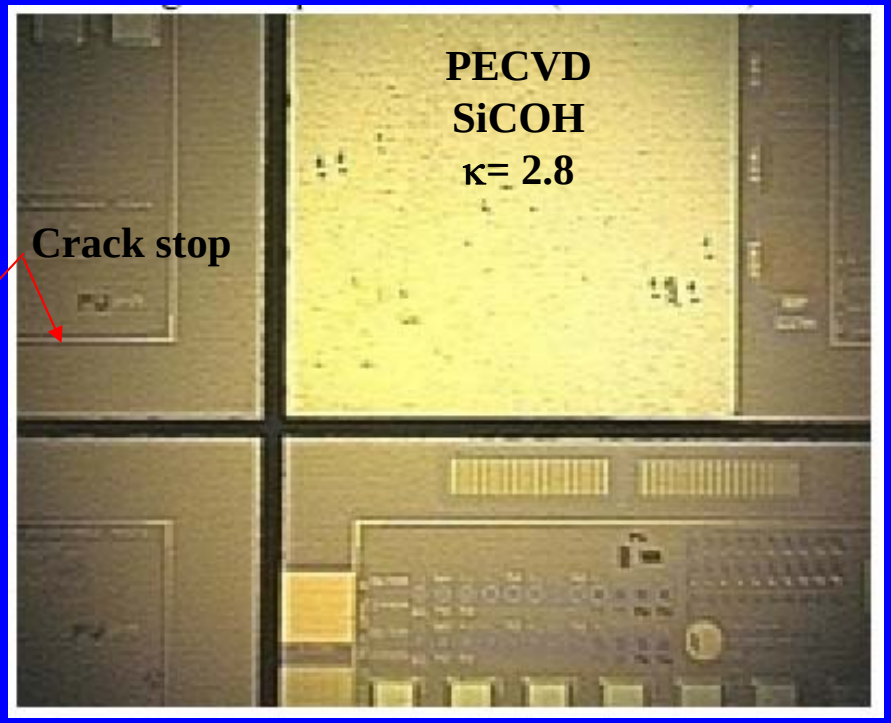


C4 or flip chip package
* High I/O density
* Small form factor

Dicing; effect of dielectric

H. Zhao, D. Shi, IEEE/CPMT Elec. Man. Tech. Symp., 2003, p. 401.



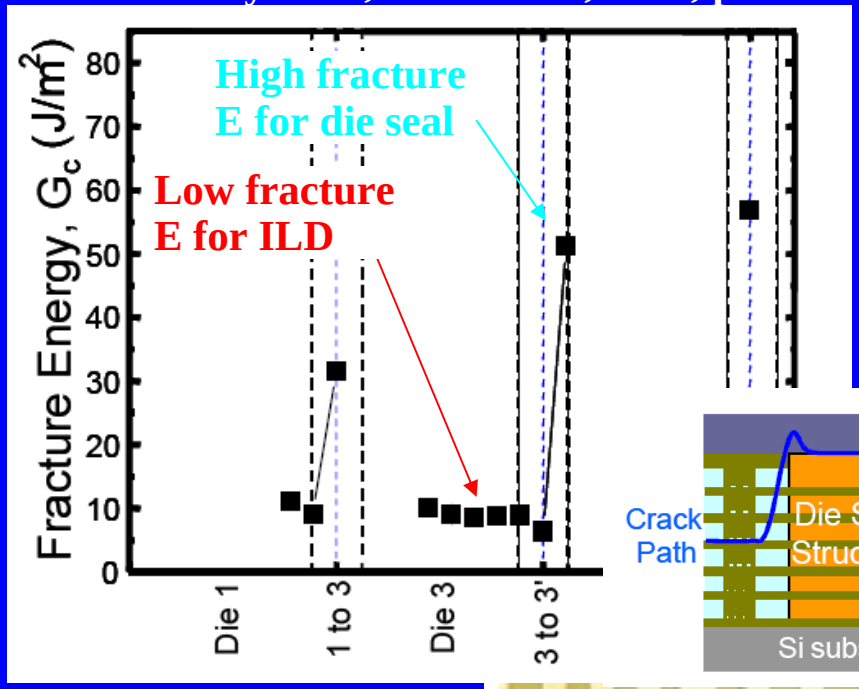


Dicing damage depends on low-k dielectric
- More dicing damage for oxide low-k vs polymer low-k dielectrics
- More damage for porous low-k vs dense low-k dielectrics

Dicing damage depends on saw process
- Less damage for smaller diamond grit size and slower speed of cut
- Less damage for two-step dicing vs one-step dicing
  - First cut removes all materials in top layer

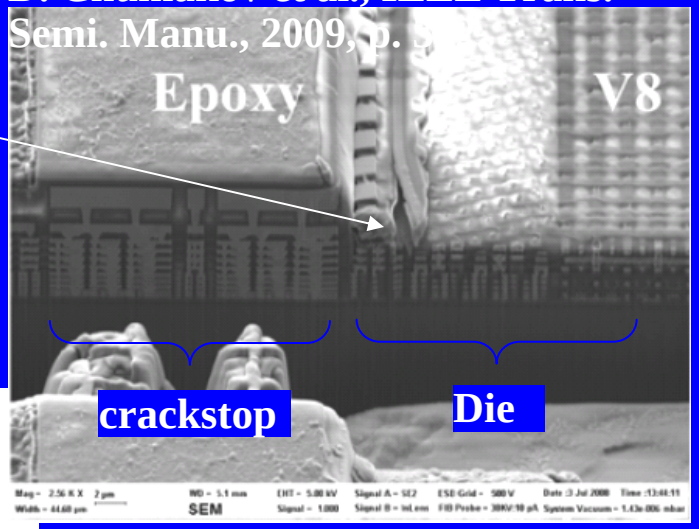
Crack stop

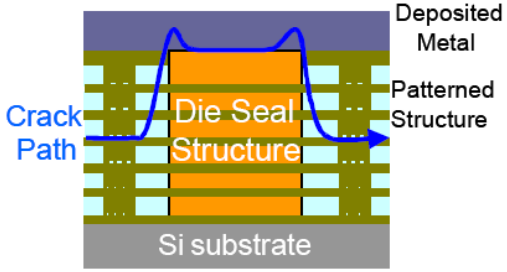
A.V. Kearney et al., IITC Proc., 2007, p. 138.

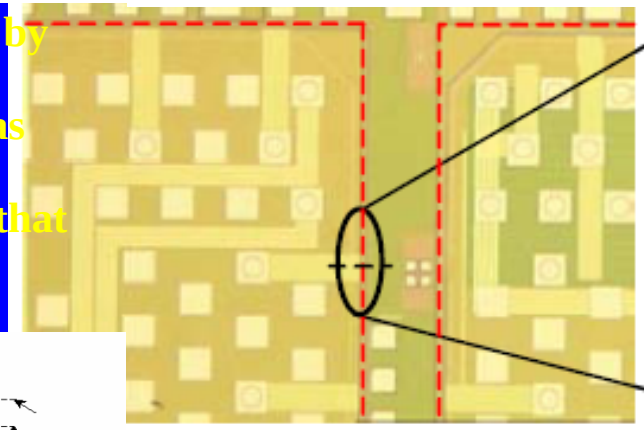


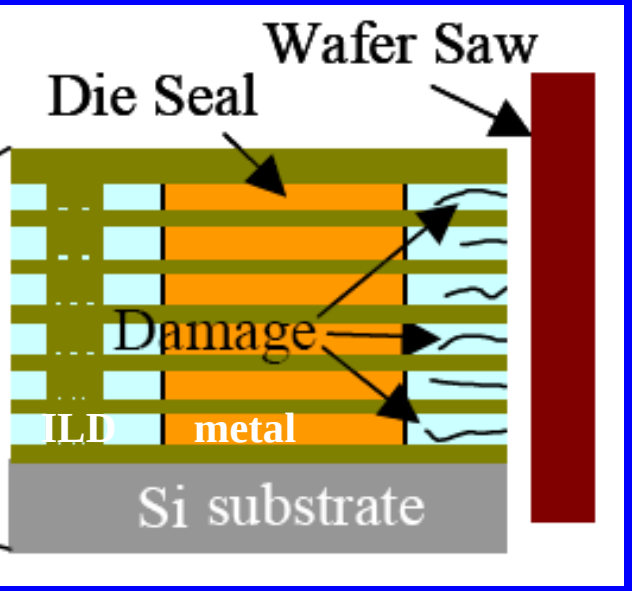
Crack is deflected

D. Chumakov et al., IEEE Trans. Semi. Manu., 2009, p.

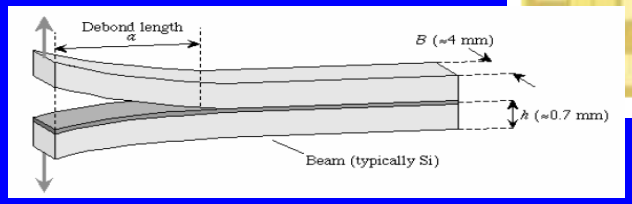








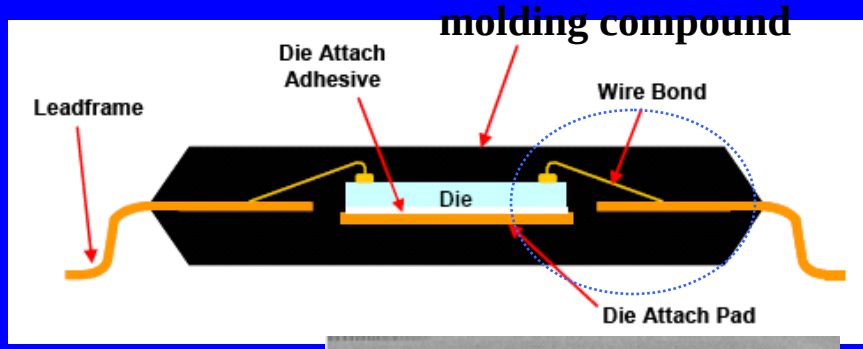
- Fracture energy measured by double canilever beam
- Fracture energy incresses as crack approaches die seal
- AFM measurement shows that crack deflects over die seal.



Edge seal ring

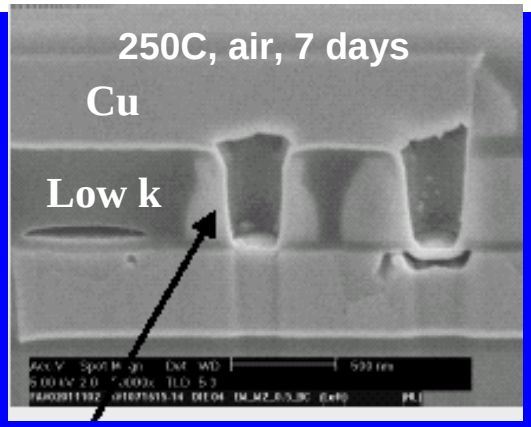
S.-H. Chen, M.-D. Ker, Microelec. Rel., 2005, p. 1311.
L. Li et al., ECTC Proc., 2007, p. 755.

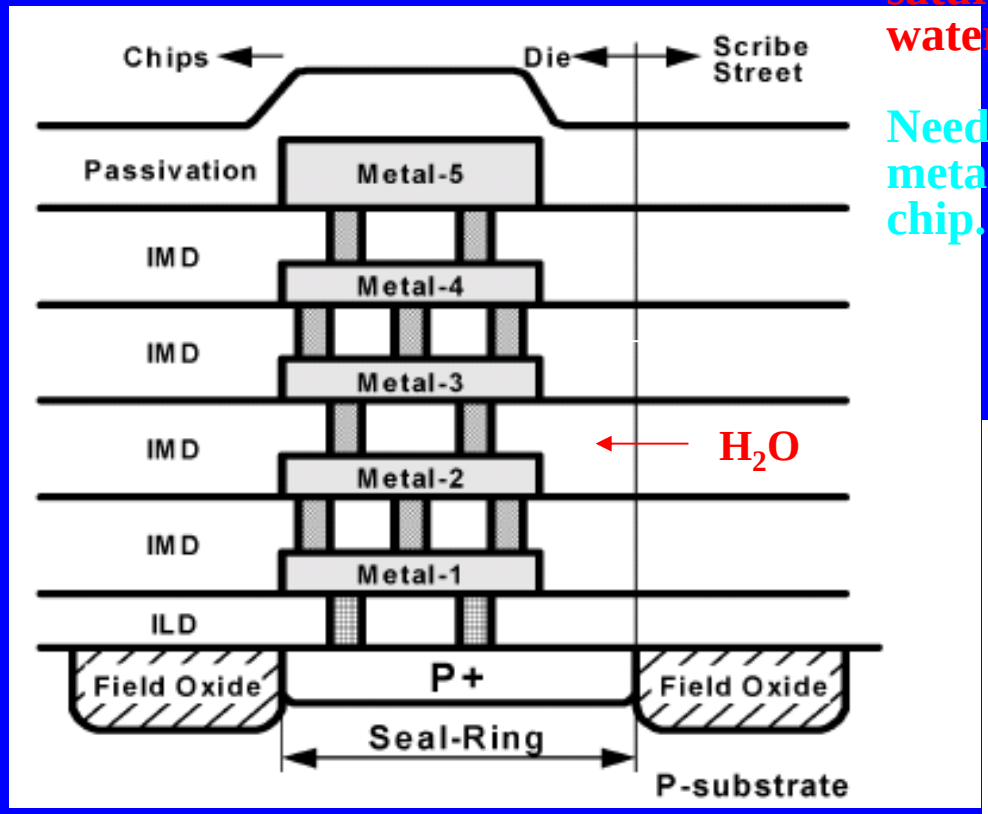
Purpose of edge seal ring:
- **Protect circuits from moisture and contamination.**
- **Provide substrate contact.**

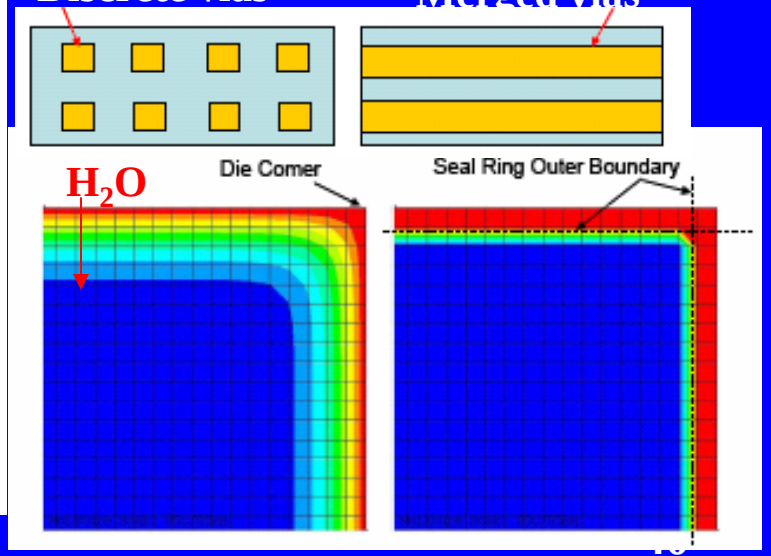


Molding compound is saturated with water after 60h

Need "wall of metal" to protect chip.



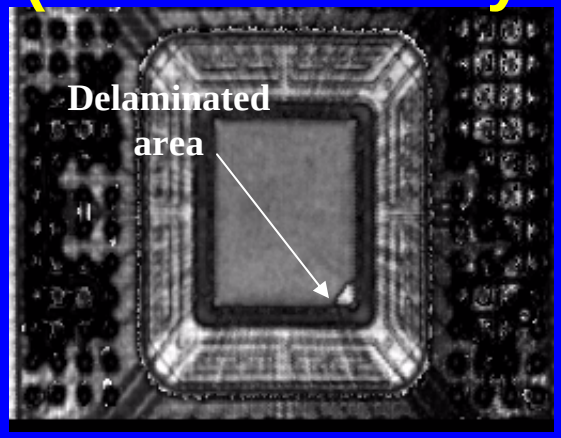


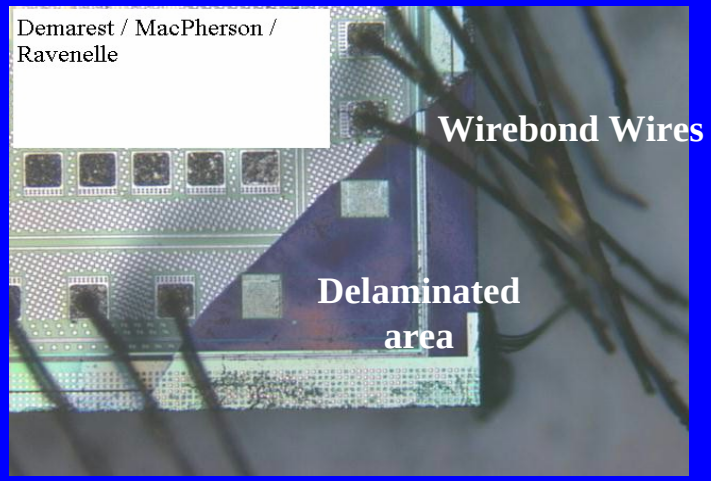


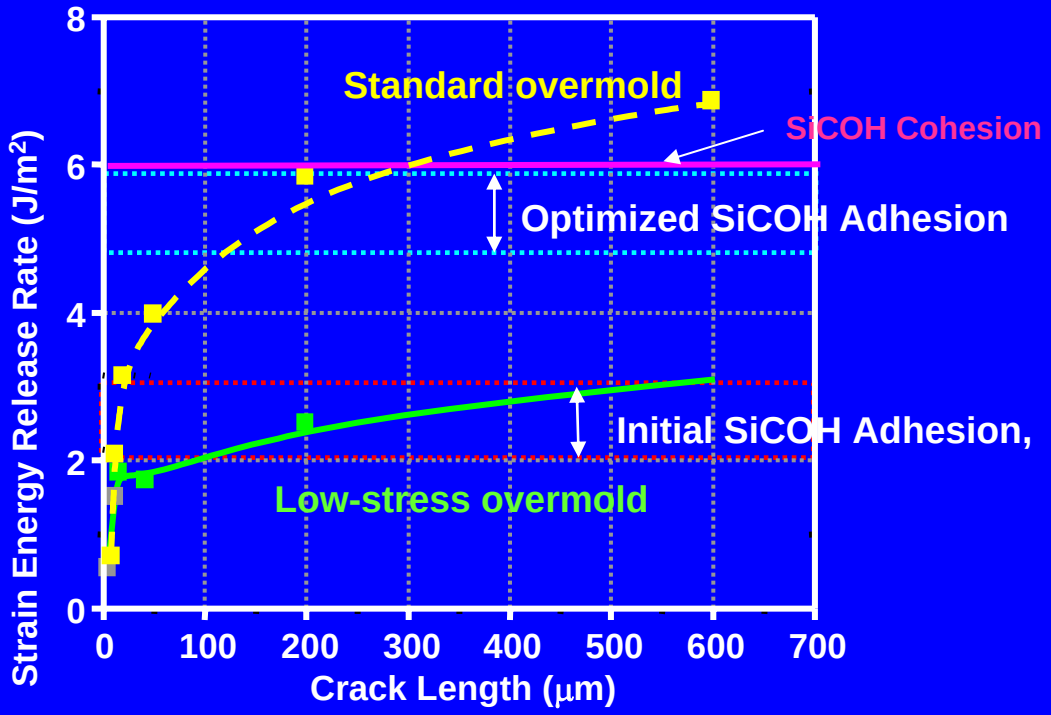
1000h, 85°C / 85% RH

Fails in Wirebond BGA package
(after thermal cycle stress)

B. Landers et al., IITC Proc., 2004, p. 108.



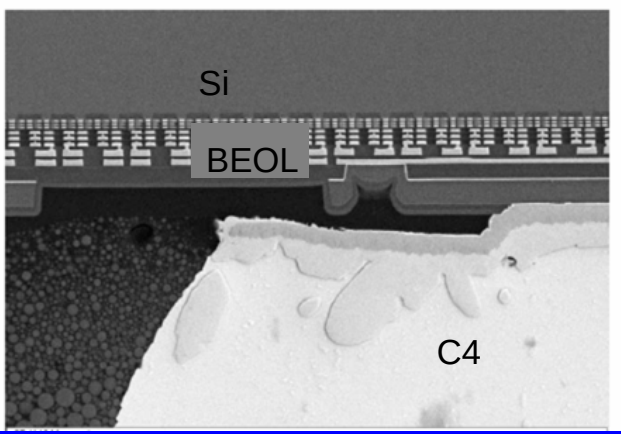




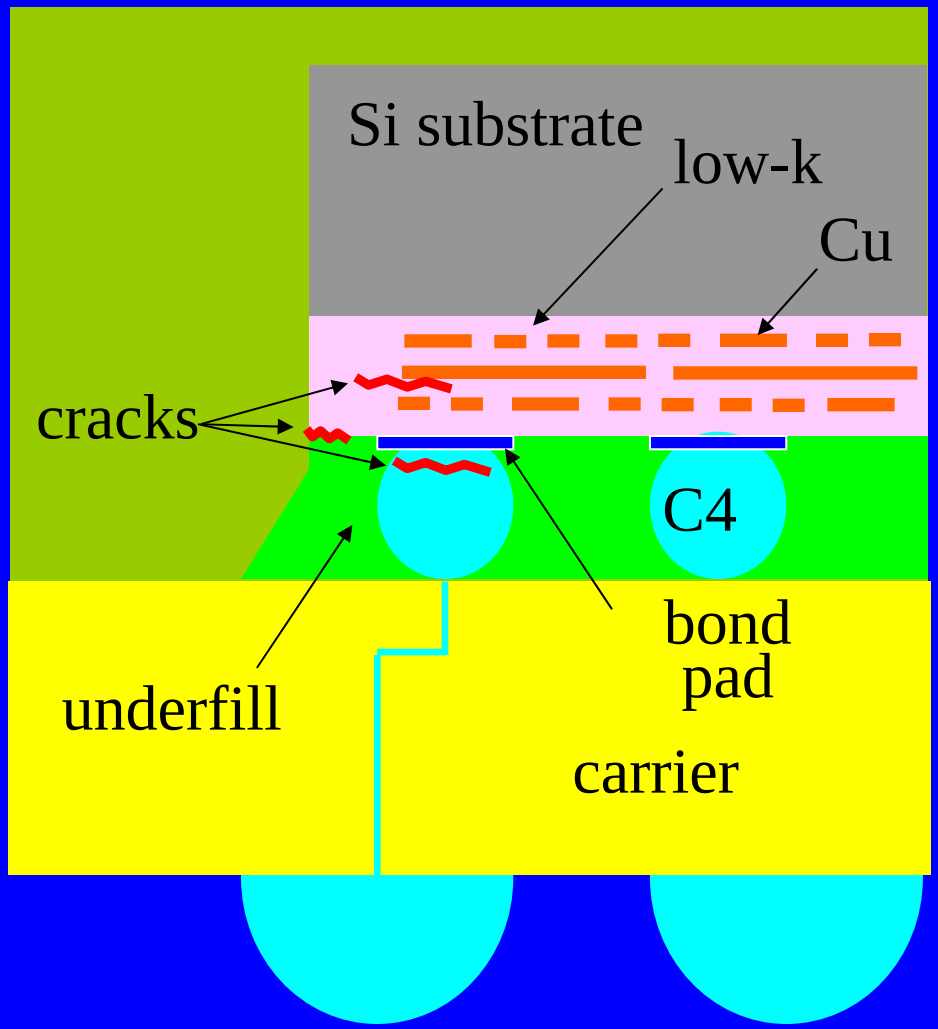
TEM of Delaminated Interface

Stress from package can crack low-k interface
- Reduce stress from package
- Improve adhesion of low-k stack
  - Interface between low-k to capping layer
- Increase modulus of low-k film

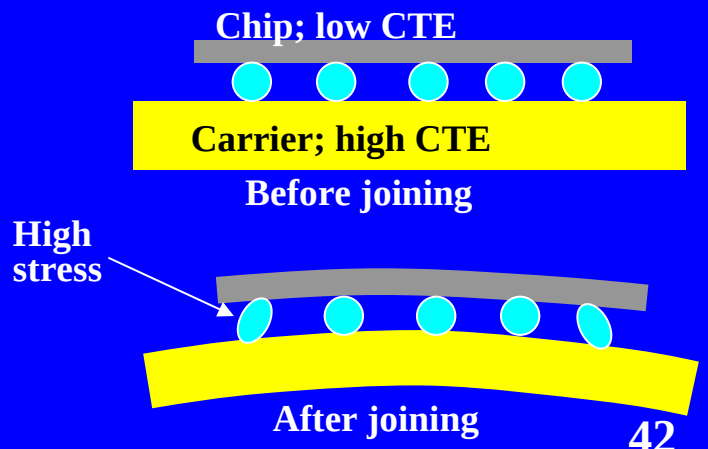
Flip chip package; low-k



T. Pan et al., IMAPS workshop, Dec. 2003 (www.kns.com)

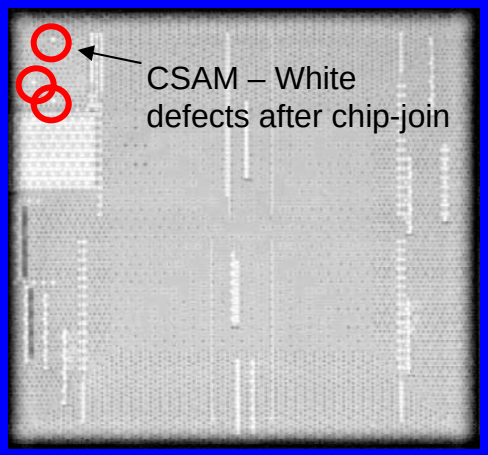


- CTE mismatch between chip and carrier causes stress at edge of chip during thermal cycling.
- Use underfill to reduce stress on C4.
- Underfill with high modulus (> 8 GPa); less stress on C4, more stress on low-k
- Underfill with low modulus (< 3 GPa); less stress on low-k, more stress on C4

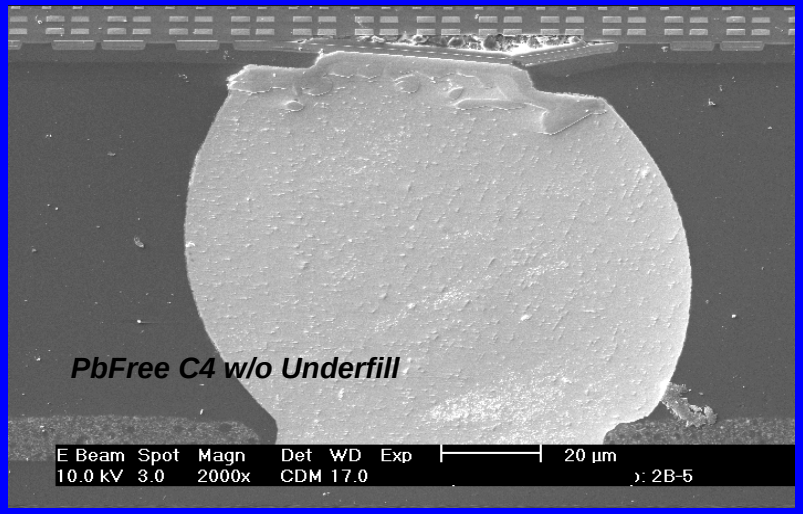


Effect of Pb-free solder on low-k

T. Daubenspeck et al., Symp. Polymers, 2008.
S. Kang et al., IBM J. Res. Dev., vol. 49, 607 (2005).
V. Vasudevan et al., ECTC, 2007, p. 116.



- High stress on chip due to Pb-free solder
  - Higher modulus compared to Pb-based solder
  - Higher reflow temperature compared to Pb-based solder
- Crack propagation depends on following:
  - Low-k film properties: modulus and adhesion
  - Chip Size
  - Final Chip Level Pad/Via Module Design
  - Solder Bump; Dimension, Type, orientation
  - Chip-Join Processes
  - Package Laminate structure



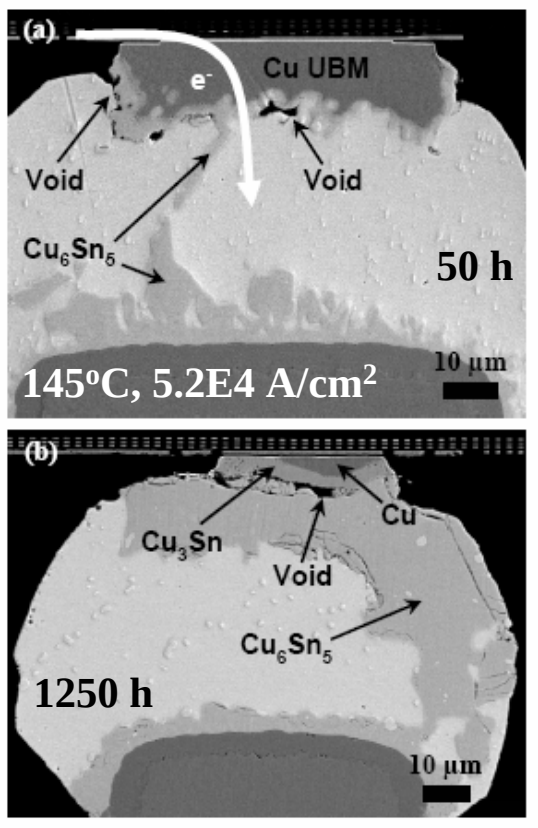
solder	melting point	Young's modulus
Sn/37%Pb	183°C	39 GPa
Sn/3.5%Ag	221°C	51 GPa
Sn/3%Ag/0.5%Cu	217°C	51 GPa
Sn/0.7%Cu	227°C	59 GPa

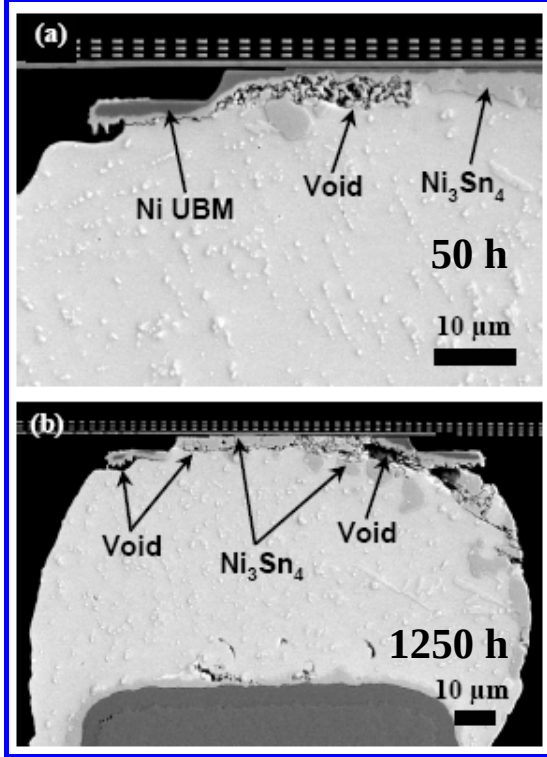
Electromigration in solder

J.W. Nah, K.N. Tu, Lead-free Tech. Workshop, 2005

metal	melting point	373°K/ T_{melt}	diffusivity @ 100°C
Cu	1356°K	0.275	$D_{surface} = 10^{-12}$ cm²/sec
Al	933°K	0.4	$D_{g.b.} = 6x10^{-11}$ cm²/sec
Pb	600°K	0.62	$D_{bulk} = 6x10^{-13}$ cm²/sec
PbSn	456°K	0.82	$D_{bulk} = 2x10^{-9}$ cm²/sec

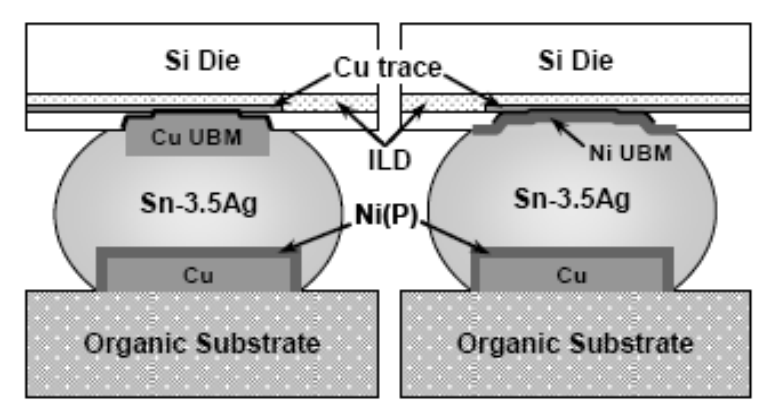
S.-H. Chae et al., ECTC Proc., 2007, p. 1442.





Current density that causes a fail:

- For Al or Cu, ~ 10^5 or 10^6 A/cm2
- For solder, ~ 10^3 or 10^4 A/cm2
  - High diffusivity (low melting point
  - Bulk diffusion rather than inteface or g.b.
  - Solid state reactions with barrier
  - Current crowding

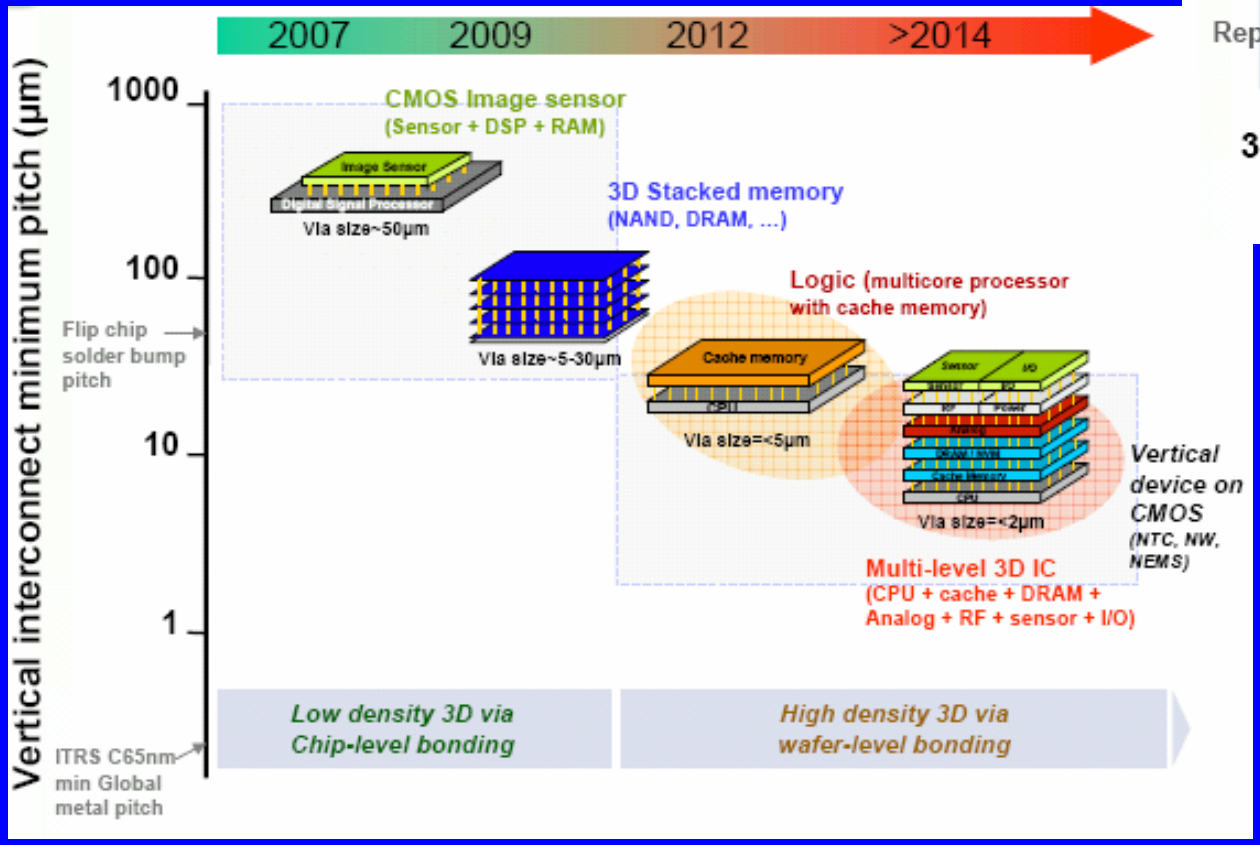


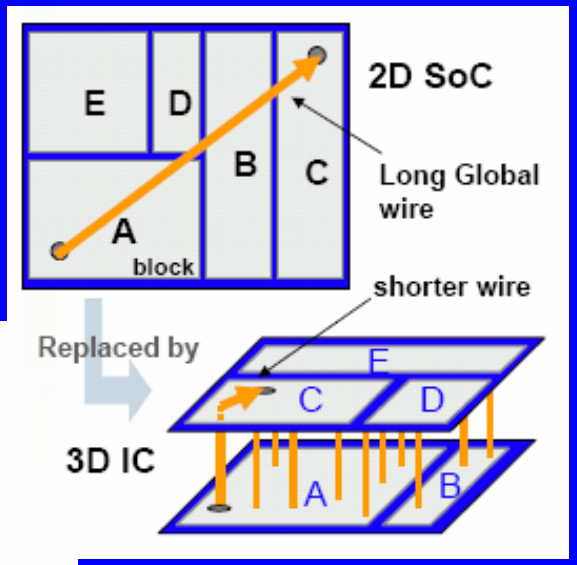
Outline

- Copper interconnect scaling
- Copper interconnect reliability
- Packaging - TSV
- Passive devices

3D integration

P. Leduc, Metrology for Nanoelectronics, 2007.





Replace long 2D wires with short 3D wires.
- **Reduce delay, cross-talk, power**
- **Need TSV size < 5 um**

Enable integration of heterogeneous devices
- **Memory, logic, sensors, etc.**
- **Need TSV size of 10 - 50 um**

Small form factor
- **Need TSV size 50 – 100 um**

Through-silicon via process options

P. Leduc et al., IITC, 2007, p. 210.

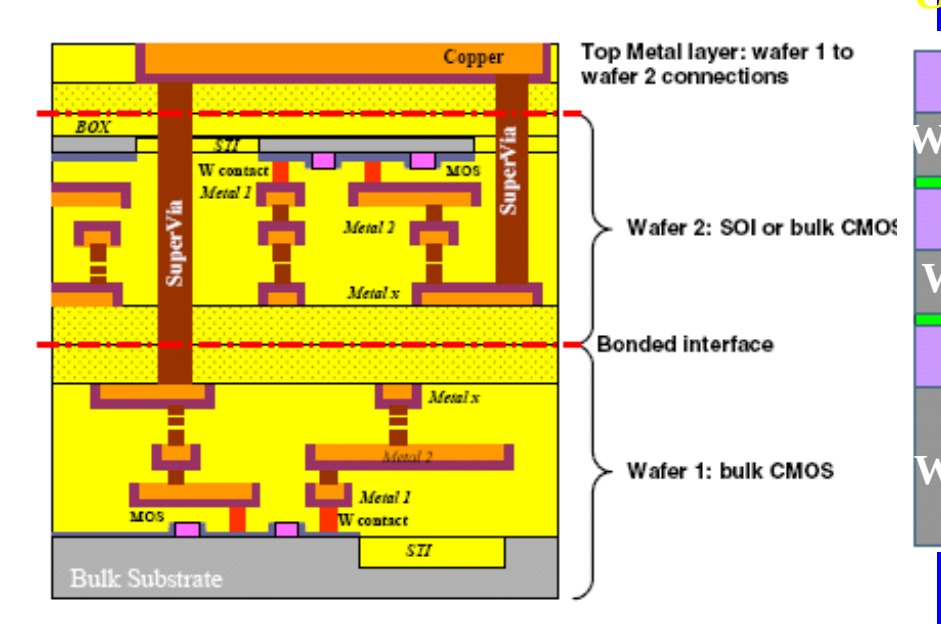
"Via last process".
- **Build FEOL + BEOL.**
- **Thinning**
- **SiO_2 bonding.**
- **TSV**

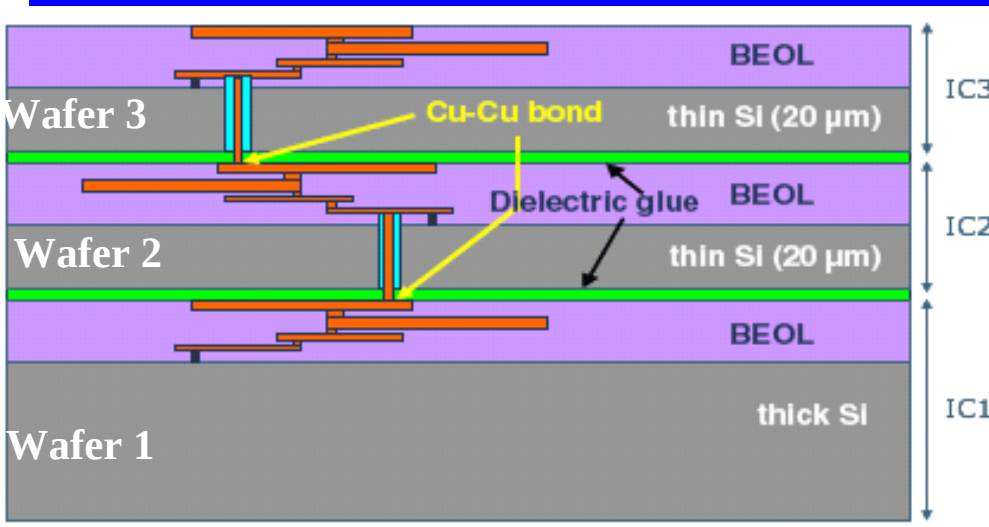
Low temp process required.
Consumes BEOL wiring area
Wafer-wafer bonding required
"Easy" bonding process.

P. De Moor et al., MRS Proc., vol. 970, 2007.

"Via first (after contact) process".
- **Build FEOL**
- **TSV**
- **Build BEOL**
- **Thinning**
- **Cu-Cu bonding**

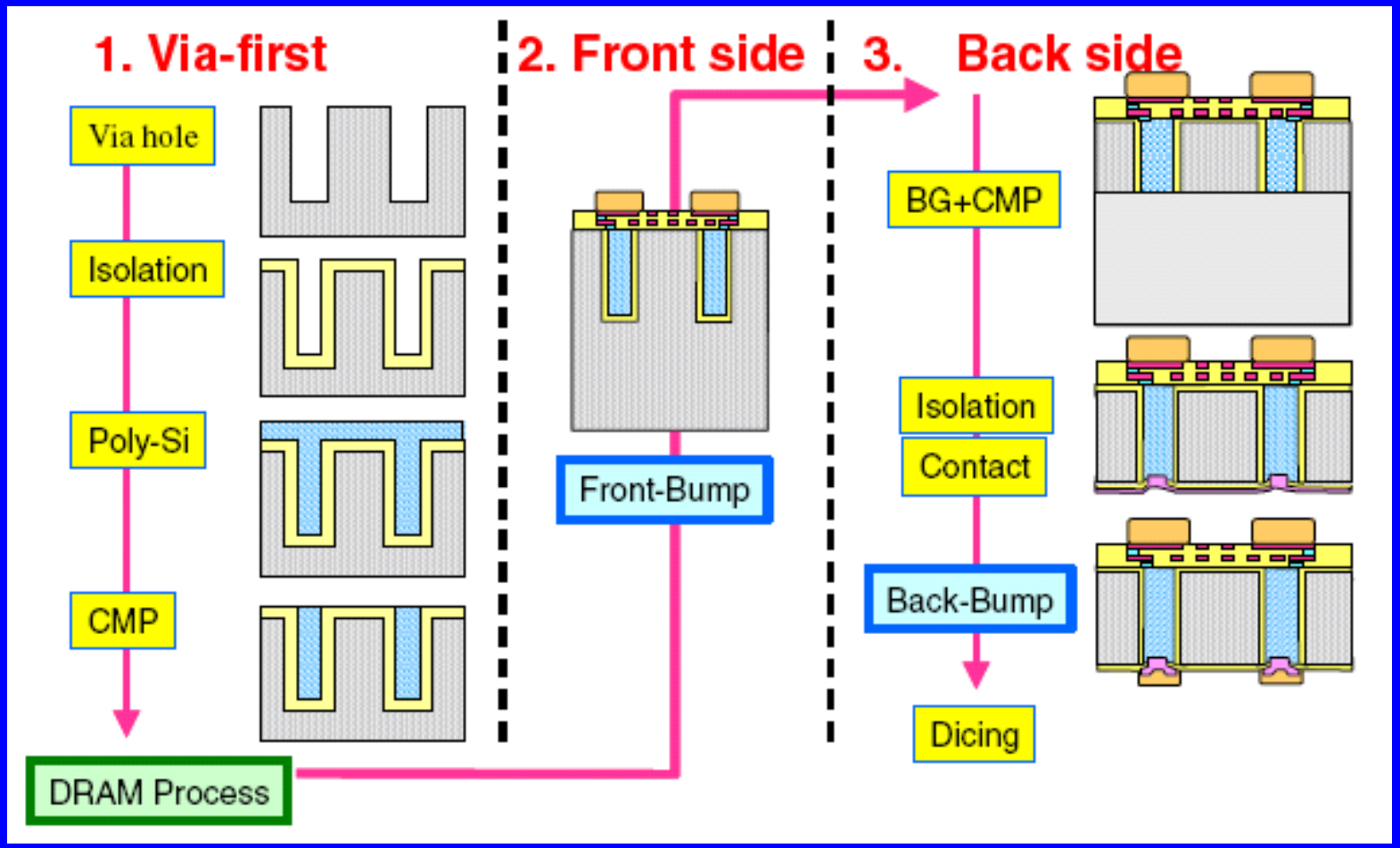
Difficult bonding process.
Process must be compatible with FEOL
Does not consume BEOL area
Chip-wafer bonding is possible





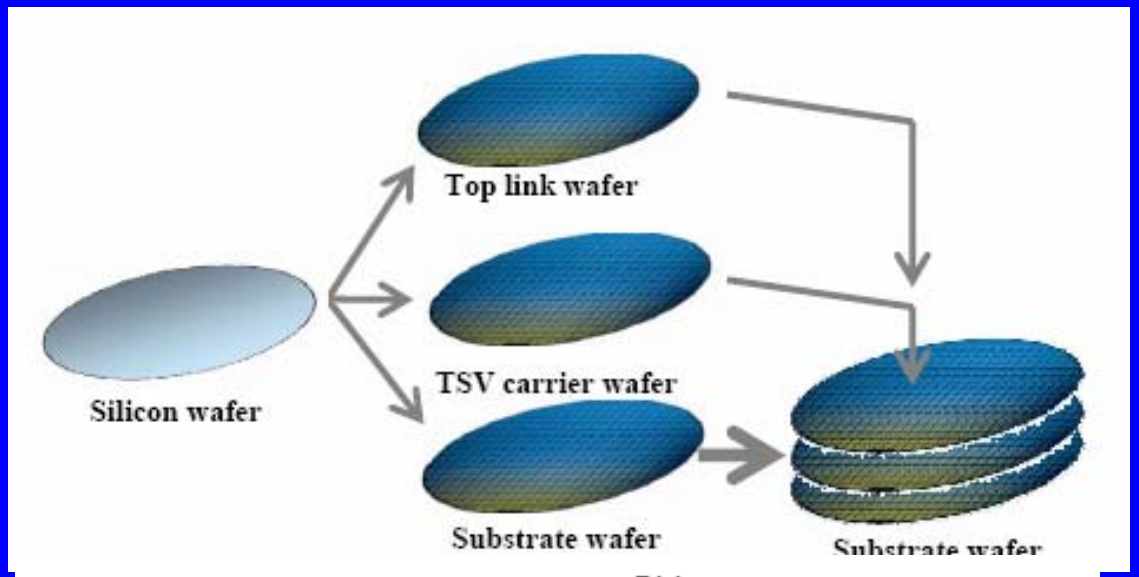
TSV process flow (via first)

T. Mitsuhashi et al., MRS Proc., vol. 970, 2007.



Die stacking vs wafer stacking

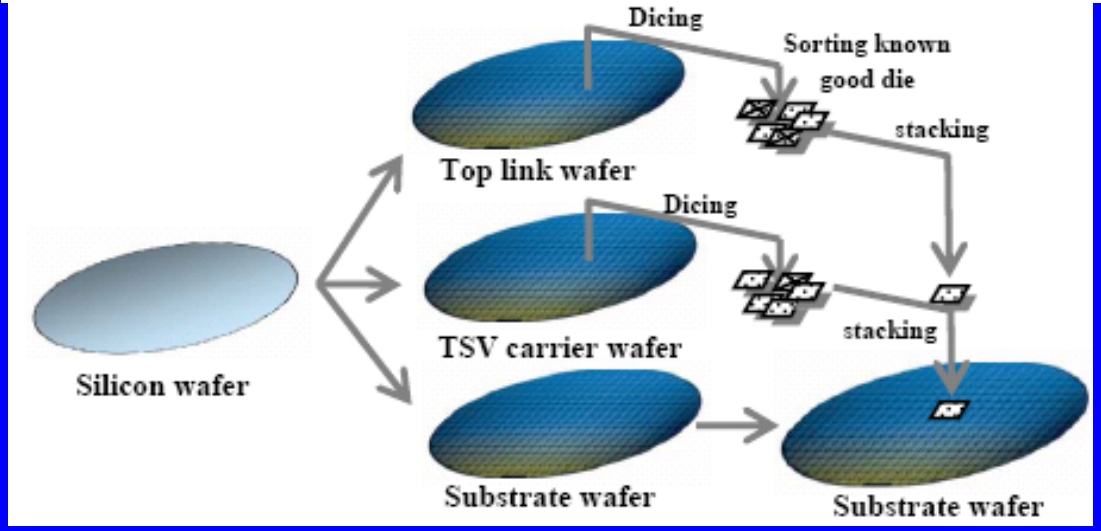
K. Sakuma et al., ECTC, 2008, p. 18.



Wafer stacking:

High throughput.

Need high yielding die (>90%)
Need same die size + wafer size.



Die stacking:

Lower throughput.

Sort + build known good die.
Different die size and wafer size is OK.

3D IC challenges

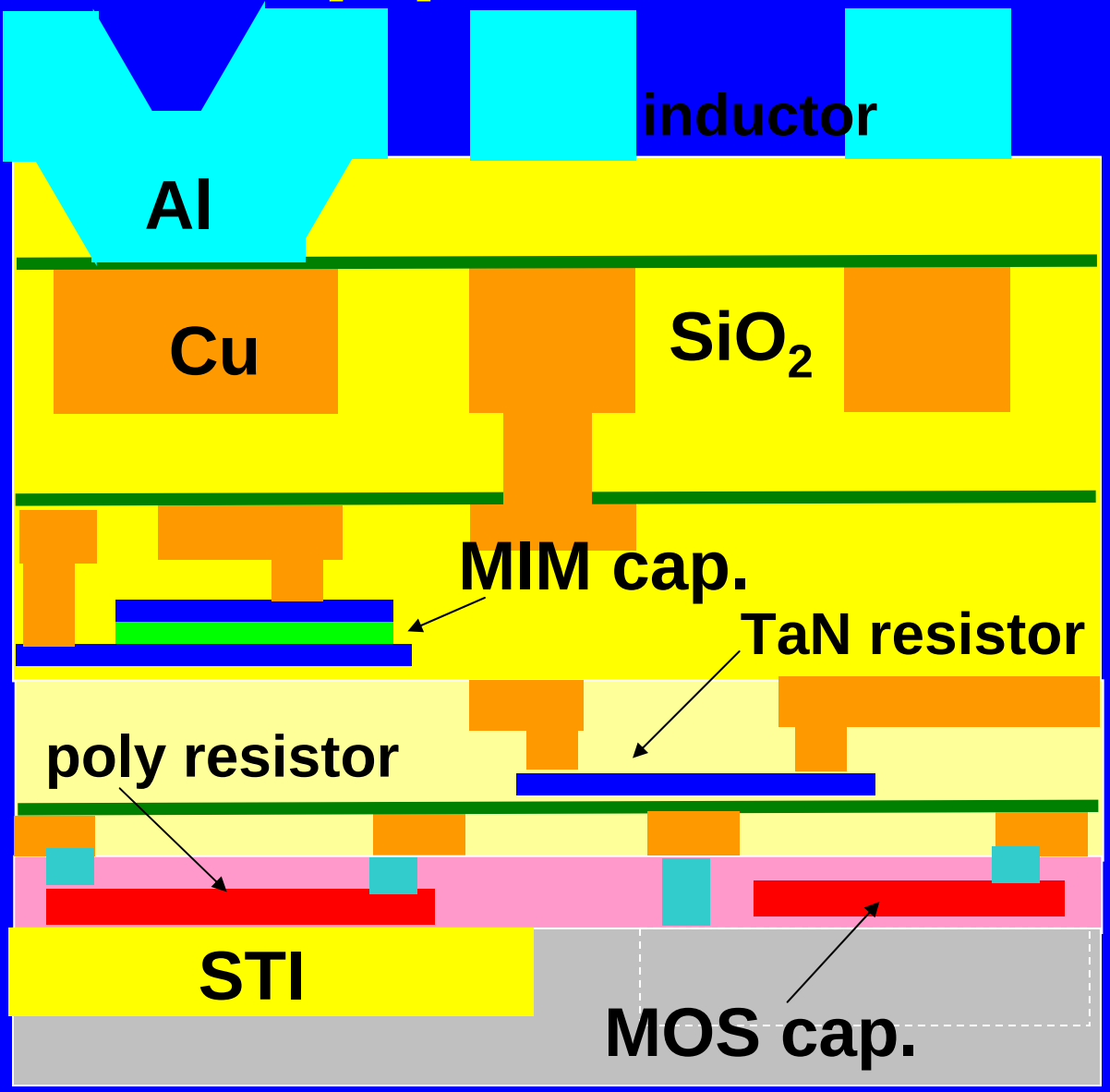
P. Leduc, Metrology for Nanoelectronics, 2007.

- Process
  - High through-put via etch and fill
  - Wafer Alignment and bonding
  - Si thinning
  - Thin wafer handling
- Test
  - Test before bonding?
- Design methodology
- Thermal management
  - Special cooling?
- Reliability
  - TSV electrical contact

Outline

- Copper interconnect scaling
- Copper interconnect reliability
- Packaging
- Passive devices

On-chip passive devices



Resistors

resistor	sheet resistance	tolerance	parasitic capacitance	temperature linearity	ref.
p+ polysilicon	200-300 ohm/sq	10-15%	0,1 fF/um^2	~ 20 ppm/^{o}C	[34]
TaN	140 ohm/sq	10%	0,03 fF/um^2	~730 ppm/^{o}C	[34]
	25 ohm/sq			0 ppm/^{o}C	[35]
	50 ohm/sq			500 ppm/^{o}C	[35]
	100 ohm/sq			800 ppm/^{o}C	[35]
SiCr	440 ohm/sq			100 ppm/^{o}C	[35]

Advantages of polysilicon resistor:

- **Low cost.**
- **Low TCR**

Advantage of metal resistor:

- **Low parasitic capacitance**

TaN resistor:

- **Compatible with Cu BEOL**
- **Resistance and TCR depends on nitrogen content.**

Capacitors

capacitor	dielectric	capacitance	tolerance	voltage linearity	temperature linearity	ref.
MOS	SiO_2	1.2 - 3.1 fF/um^2	10 - 15%	> 1000 ppm/V	20 - 50 ppm/°C	[34]
PIP	SiO_2	1.6 fF/um^2	25%	> 2000 ppm/V	~20 ppm/°C	[34]
MIM	50 nm SiO_2	0.7 fF/um^2	7%	< 25 ppm/V	~50 ppm/°C	[3,34]
MIM	50 nm SiN	1.35 fF/um^2	13%			[3]
MIM	33 nm SiN	2.1 fF/um^2	11%			[3]
MIM	Ta_2O_5	3 fF/um^2		~ 100 ppm/V	84 ppm/°C	[36]
MIM	Al_2O_3	3 fF/um^2		~ 400 ppm/V	255 ppm/°C	[36]
MIM	25nm HfO_2-Al_2O_3	6.6 fF/um^2		109 ppm/V	196 ppm/°C	[37]
MIM	13nm HfO_2-Al_2O_3	13 fF/um^2		236 ppm/V	183 ppm/°C	[37]
VPP	90 nm node 7 metal layers	> 3 fF/um^2				[38]

Advantages of MOS capacitor:

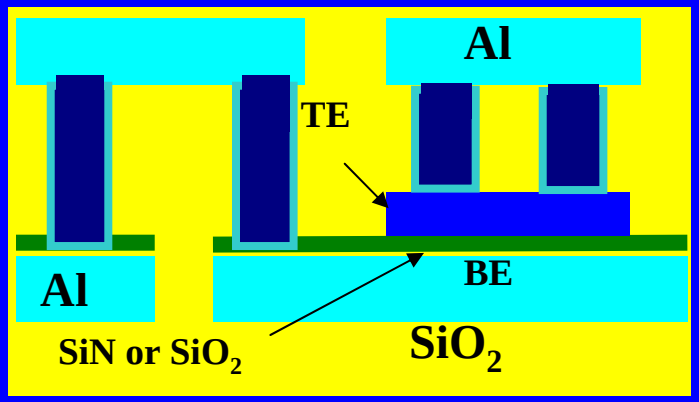
- **Low cost.**
- **High capacitance density**

Advantages of MIM capacitor:

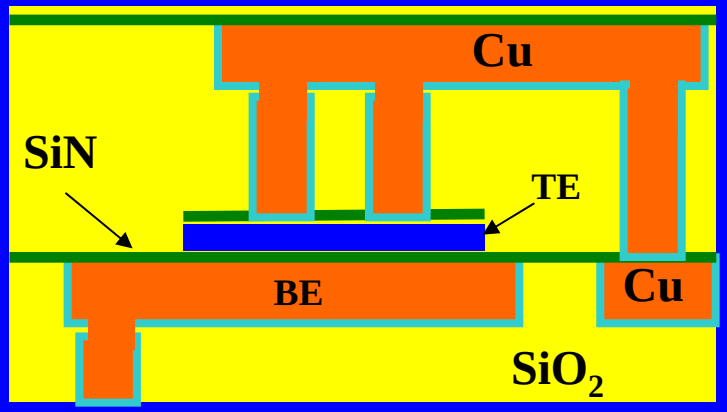
- **Good voltage linearity**
- **High quality factor (low parasistic resistance).**

MIM capacitor in Cu technology

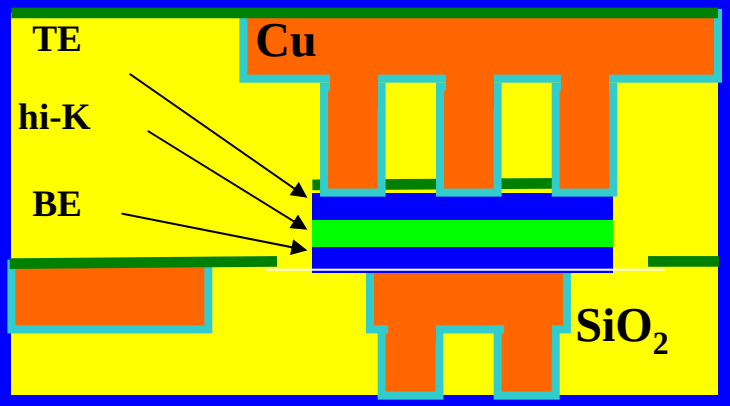
C.H. Ng, C.-S. Ho, S.F. Chu, S.-C. Sun, IEEE Trans. Elec. Dev., 52, 1399 (2005).



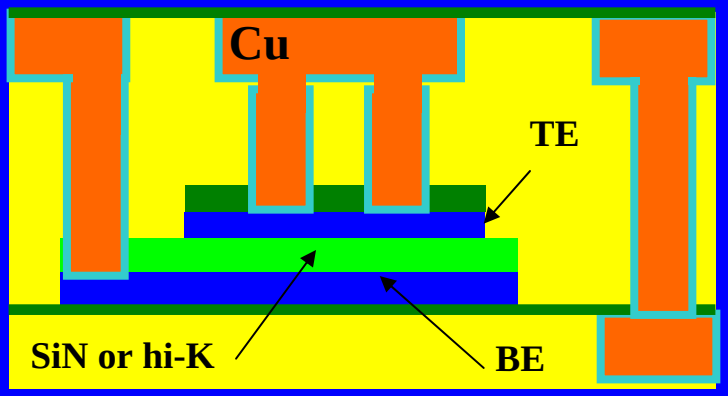
(a) MIM in Al BEOL



(b) MIM in Cu BEOL(1 mask)



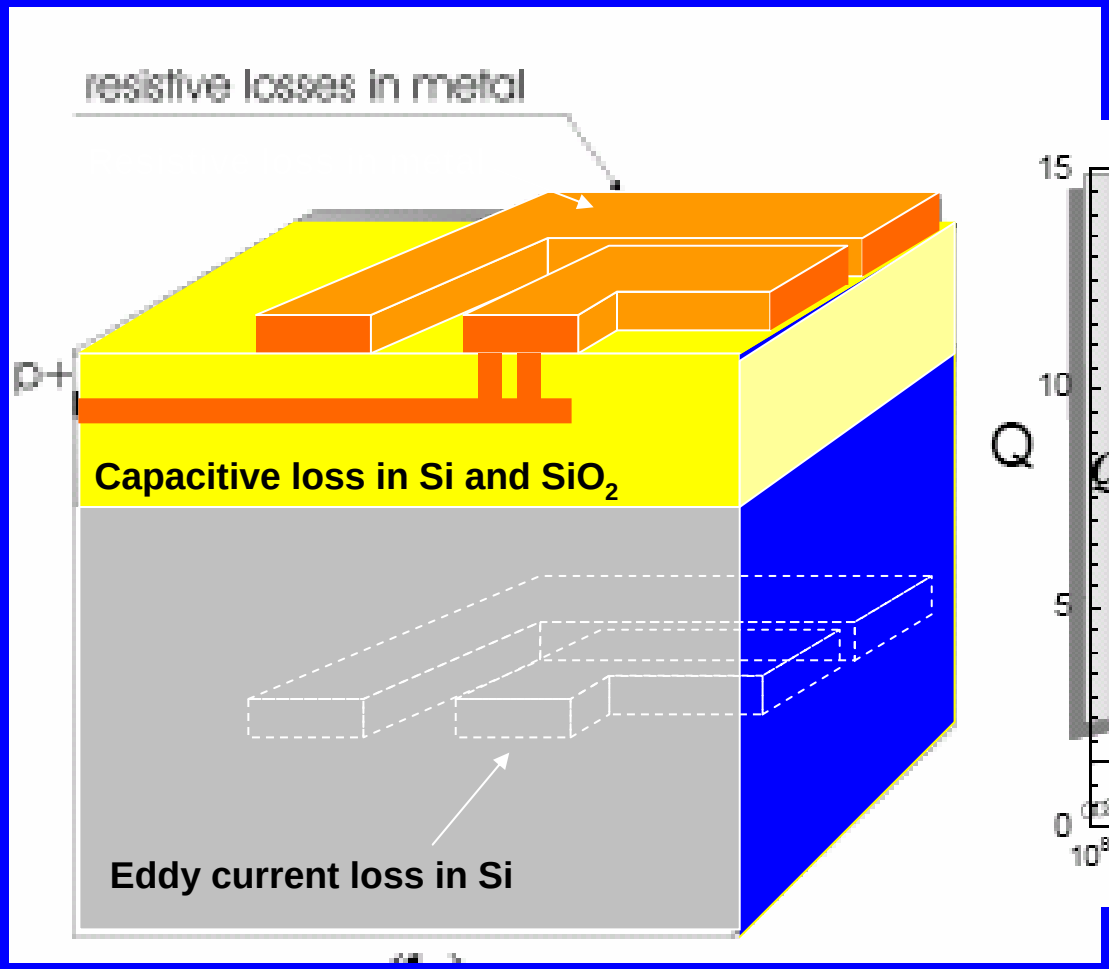
(c) MIM in Cu BEOL (2 masks)

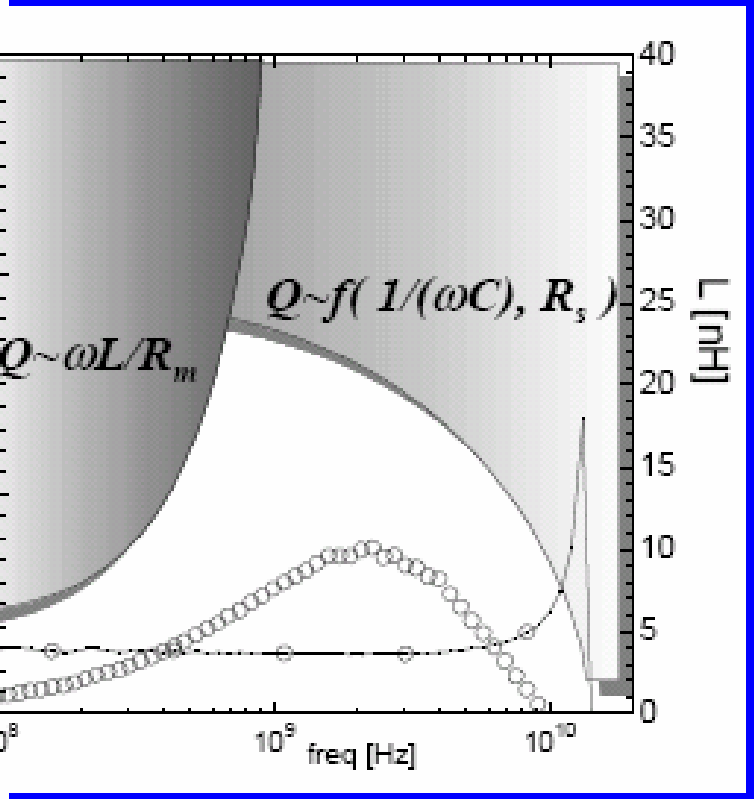


(d) MIM in Cu BEOL (2 masks)

Sources of energy loss for on-chip inductor

S. Jenei, S. Decoutere, S. Van Huylenbroeck, G. Vanhorebeek, B. Nauwelaers,
Silicon Monolithic Integrated Circuits in RF Systems, 2001, p. 64.

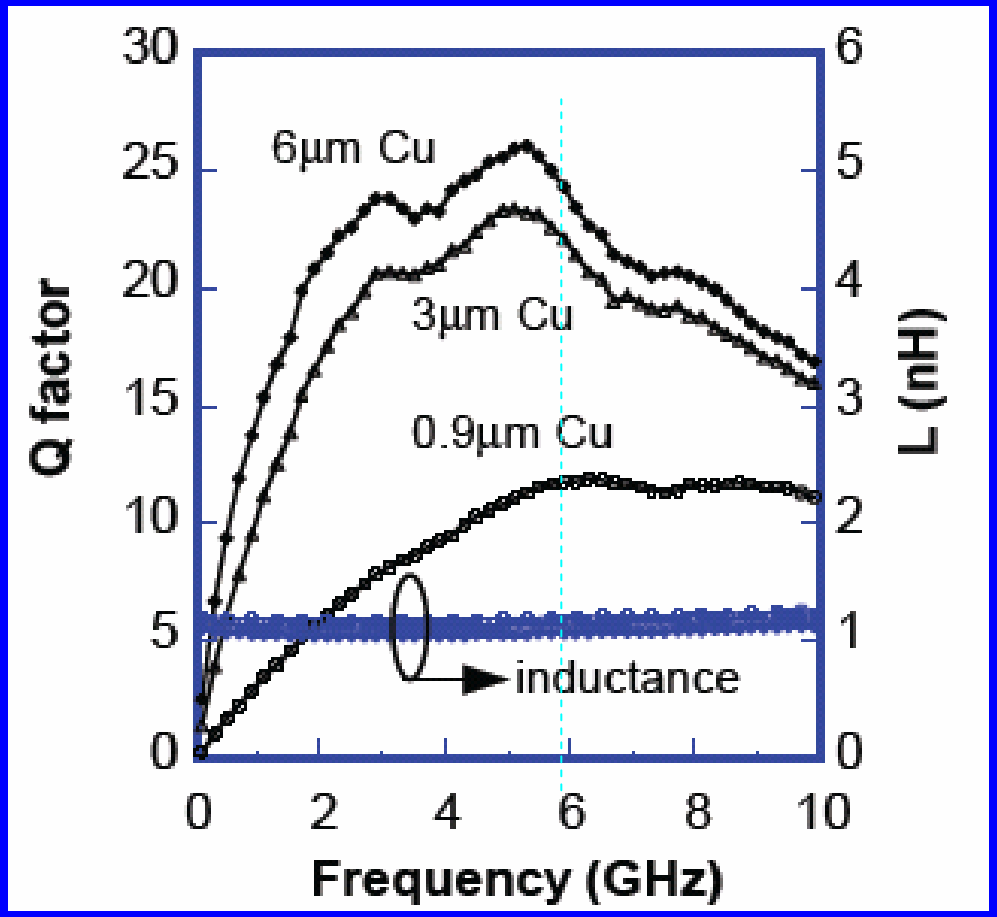




Low frequency: resistive loss dominates (use thicker metal)
High frequency: capacitive loss dominates (decouple from substrate)

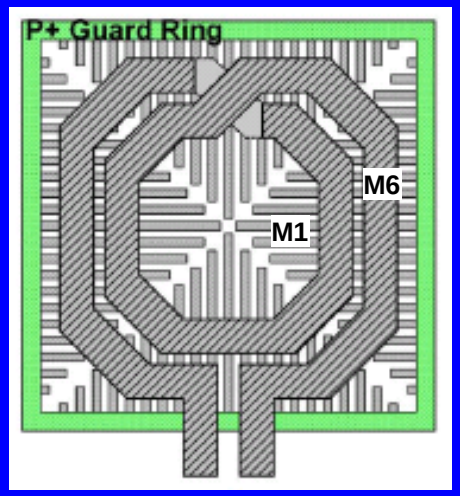
Quality factor improvement

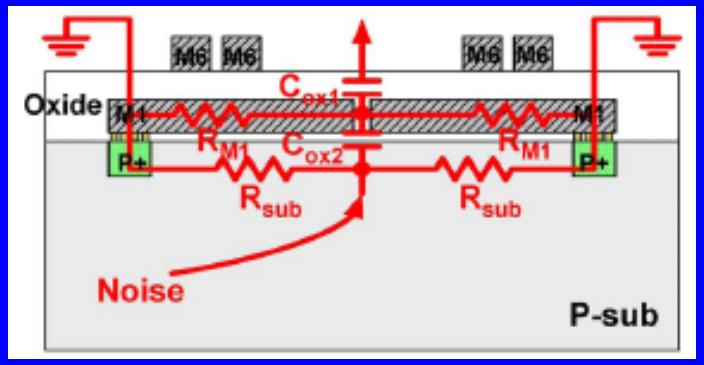
C.-H. Chen et al., IEDM Proc., 2003, p. 39.



Increase metal thickness

Y.-C. Wu et al., IEEE Elec. Dev. Lett., 2009, p. 383.





Use patterned ground shield (M1)

Conclusion

- Process integration
  - Porous low-k (k < 2.5) is very fragile → difficult processing
    - Low final dielectric constant may not be achieved due to damage.
    - Air-gap is an alternative (but higher cost)
  - Process variation
    - Litho and etch control; CMP control and pattern density rules
- Reliability
  - For longer electromigration lifetime → Metal capping layers, metal alloys
  - Minimize fails from stress-induced voids → Redundant vias
  - Maximize TDDB lifetime → control line width variation, minimize polish damage

Conclusion

- Packaging
  - Minimize damage to low-k dielectric → optimize dicing, underfill, molding compound, layout.
  - Pb-free solder; must optimize solder composition, solder reflow, pad layout, and underfill.
  - Electromigration of solder: Use Cu pillars , reduce current crowding, optimize barrier layer metals.

- Passive devices for RF and mixed signal technology
  - Resistors: polysilicon (low cost, low TCR) vs TaN (low parasitic capacitance)
  - Capacitors: MOS (low cost, high capacitance density) vs MIM (good voltage linearity, high quality factor)
  - Inductors: Improve Q → thick Cu and high resistivity substrate or ground shield .