Single-Stage Single-Switch PFC Converter with Extreme Step-Down Voltage Conversion Ratio

Esam H. Ismail, Mustafa A. Al-Saffar, and Ahmad J. Sabzali
Senior Member, IEEE, Member, IEEE, Member, IEEE
Department of Electrical Engineering, College of Technological Studies
P.O. Box 35007, AL-Shaa’b, Kuwait, 36051
eismail@ieee.org

Abstract—This paper presents a new single-stage single-switch (S\textsuperscript{3}) high power factor correction (PFC) AC/DC converter suitable for low power applications (< 150 W) with a universal input voltage range (90-265 V\textsubscript{rms}). The proposed topology integrates a buck-boost input current shaper followed by a buck and a buck-boost converter, respectively. As a result, the proposed converter can operate with larger duty cycles compared to the exiting S\textsuperscript{3} topologies; hence, making them suitable for extreme step-down voltage conversion applications. Several desirable features are gained when the three integrated converter cells operate in discontinuous conduction mode (DCM). These features include low semiconductor voltage stress, zero-current switch at turn-on, and simple control with a fast well-regulated output voltage. A detailed circuit analysis is performed to derive the design equations. The theoretical analysis and effectiveness of the proposed approach are confirmed by experimental results obtained from a 35-W/12-V\textsubscript{dc} laboratory prototype.

Index Terms—fast output regulation, low harmonic distortion, power factor correction (PFC), single-stage single-switch rectifier, unity power factor (UPF).

I. INTRODUCTION

Power factor correction (PFC) circuit becomes mandatory in off-line power application to comply with international harmonic regulations such as Standards IEEE 519 and EN/IEC 61000-3-2. Accordingly, active PFC techniques have rapidly become a vital research topic in the power electronics field, and considerable efforts have been made on the development of the active PFC converters [1].

Active PFC improves power factor to more than 95%, which surpasses the 75% PF with passive PFC solution. Hence, active PFC is more energy saving than passive PFC. In general, active PFC techniques can be divided into two categories: two-stage and single-stage approaches. The two-stage approach can achieve good performance at the expense of high cost, low power density, low conversion efficiency, and complicate control circuit, particularly in low-power applications [2]. To overcome these drawbacks, many single-stage PFC topologies have been proposed recently as a cost-effective approach for low-power applications to achieve both the function of high PFC and fast output voltage regulation. Unfortunately, unlike the two-stage approach, the single-stage converters have relatively high-voltage stress suffered by their switching components. This is due to the unregulated dc-voltage on the intermediate energy storage capacitor, which generally depends on both the line and load characteristics [3]. This condition will limit the single-stage approach especially when it requires an operation with a universal input voltage because the storage capacitor voltage would easily rise beyond 450 V. Therefore, a bulky capacitor and high voltage rating semiconductors have to be used; this increases both the size and cost and will result in lower efficiency, as well as reduced hold-up time.

In an effort to reduce the dc-voltage on the energy storage capacitor, a number of techniques have been introduced. However, most of the proposed techniques usually comprise of a boost converter for PFC followed by a dc-dc converter for output voltage regulation. Hence, for low output voltage applications, a high step-down transformer topology would be needed for the output dc-dc stage even when galvanic isolation is not required. In contrast, conventional single-switch buck-boost topologies, including the plain buck-boost, flyback, SEPIC, and Cuk converters [4]-[6], have the potential of both PFC and step-down conversion capability. However, they incur penalties of reduced efficiencies and increase component stresses when compared to the boost converter. In addition, the buck-boost topologies suffer from providing low output voltage over a large range of input voltages since it requires an extreme low duty ratio (short switch on-time) operation. A high switching frequency operation reduces the switch on-time even shorter and gives rise to an objectionable increase in switching losses. Thus, not only does it degrade the conversion efficiency and the transient dynamics of the converter, it also limits the ability to increase the switching frequency. Moreover, applying the buck-boost regulator to applications with extreme step-down ratios creates significant challenges for the pulse-width modulation (PWM) controller.

In order to overcome these drawbacks, several step-down single-stage PFC converters have been proposed lately [7]-[16]. However, these converters are not suitable for very low voltage step-down applications without utilizing a high step-down transformer. On the contrary, the topology presented in [17] can extend the duty ratio by utilizing coupled inductors with low turns ratio. As a result, it can provide a high step-down voltage conversion ratio with a lower output current ripple and lower voltage stress across the rectifier diodes. The main disadvantages of the proposed topology in [17] are the large component count and the requirement of a front-end PFC stage, which increases the cost and the complexity of the system. In

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two different transformer-less schemes have been proposed based on integrating buck-boost PFC cell with a dc-de buck converter. These converters can provide low output voltage over a large range of input voltages with a lower component count compared to the one presented in [17].

The purpose of this paper is to present a new single-stage single-switch high PFC converter suitable for universal input voltage operation and extreme low output dc voltage applications. We approach this task by integrating a front-end buck-boost converter with a buck converter followed by a buck-boost converter as shown in Fig. 1. The buck-boost converter is selected due to its capability of providing a step-down voltage conversion and a high power factor when it is operating in the discontinuous-conduction-mode (DCM). On the other hand, the buck converter is selected due to its step-down capability, while the buck-boost is selected due to both step-down and isolation properties. Hence, the resultant Buck-Boost + Buck + Buck-Boost (B5) converter allows the duty cycle to be extended further compared to the converters in [18]-[19] and makes the proposed converter more suitable for extreme voltage step-down isolated and non-isolated applications. In addition, the related characteristics of the proposed converter in Fig. 1 also include the absence of inrush current problem and the ability to protect against over load current.

Operation principle of the proposed B5 converter is described in Section II. Operation of the B5 converter as a PFC rectifier and its steady-state characteristics are discussed in Section III together with a low-frequency averaged model. In Section IV, the design considerations of the proposed B5 converter are given. Section V presents simulation and experimental results for a 35-W/12-V, dc prototype circuit followed by a conclusion in Section VI.

II. CONVERTER OPERATION PRINCIPLE

From Fig. 1, the operation of the buck cell and the output buck-boost cell in either continuous conduction mode (CCM) or DCM has no effect on the quality of input current provided that the input buck-boost cell operates in DCM. On the other hand, it is found that when the three cells operate in DCM, several desirable advantages can be gained: 1) Inherent PFC capability with zero-current switch turn-on. 2) Reduction of the reverse recovery problem of the fast diodes in the circuit. 3) Low voltage stress on both the energy stored capacitors (C1 and C2) and the active switch Q, which is independent of the load current variations. 4) Well and fast regulation of the output voltage. These advantages are obtained at the expense of drawing higher peak currents by the converter. By using a high speed and a higher current density switch, the peak currents and their impact become less significant when compared to the gained advantages. Furthermore, the converter efficiency can be improved if the output inductor, L3, is operated at the boundary conduction mode (BCM), since the peak currents in the converter will be reduced. This will also reduce the ac core losses, as well as the current ripple in the output capacitor Co.

Accordingly, the B5 converter in Fig. 1 is analyzed in this section based on the assumption that the three converter cells are operating in DCM. To simplify the analysis, the following assumptions are made: 1) The input voltage vi is considered to be an ideal rectified sine wave, i.e., $v_i = V_m |\sin(\omega t)|$, where $V_m$ is the peak line voltage and $\omega$ is the line angular frequency. 2) The switching frequency ($f_s$) is much higher than the ac line frequency ($f_L$), so that the input voltage can be considered constant during one switching period ($T_s$). 3) All capacitors are big enough such that their switching voltage ripples are negligible during $T_s$. 4) Inductors L1, L2 and L3 operate in DCM. Furthermore, the currents in inductor L1 and L2 reach zero level prior to the current in the output inductor L3. With these assumptions, the circuit operation during one switching period $T_s$ can be described in four distinct operating stages. Fig. 2 shows the four different operating modes of the B5 converter operating in DCM-DCM. These operating modes can be briefly described as follows:

Stage 1 [$t_0$, $t_1$]: Prior to this interval, the currents through L1, L2 and L3 are zero. When switch Q is turned on at $t = t_0$, diodes D2 and D3 become forward biased, and the inductor currents $i_{L1}$, $i_{L2}$ and $i_{L3}$ begin to increase linearly. This interval ends when switch Q is turned off, initiating the next stage.

Stage 2 [$t_1$, $t_2$]: When switch Q is turned off, diodes D2 and D3 become reverse-biased. Thus, $i_{L1}$ decreases linearly at a rate proportional to the capacitor voltage $V_{C1}$ through diode D1. Diodes D4 and D5 begin to conduct; therefore, the currents $i_{L2}$ and $i_{L3}$ decrease by an amount proportional to the capacitor voltage $V_{C2}$ and the output voltage $V_o$, respectively. This stage ends when the current $i_{L1}$ reaches zero. The diode D2 prevents the current $i_{L1}$ from becoming negative.

Stage 3 [$t_2$, $t_3$]: In this stage, the two inductor currents $i_{L2}$ and $i_{L3}$ continue to decrease through diode D4 and D5, respectively. This stage ends when the current $i_{L2}$ reaches zero.

Stage 4 [$t_3$, $t_4$]: In this stage, the current $i_{L3}$ continues to decrease through the free-wheeling diode D5 until it becomes zero. The converter stays in this stage until switch Q is turned-on again. It is preferred to turn-on the switch at $t = t_4$, which will reduce the current stresses through the semiconductor devices, leading to a better overall efficiency.

Fig. 3 depicts the typical waveforms of the proposed B5 converter operating in DCM-DCM.
III. THEORETICAL ANALYSIS

In this section, the operation of the proposed B5 converter is analyzed as a PFC rectifier. The conditions for DCM operation, large signal model, and expressions for the capacitor voltages $V_{C1}$ and $V_{C2}$ are derived.

A. Conditions for DCM

From Fig. 3, the normalized switch off-time defined by $D_x$, $D_y$, and $D_z$ can be found in terms of the switch duty-cycle $D$ by applying volt-sec balance across $L_1$, $L_2$, and $L_3$, respectively, which gives,

$$D_x = D \frac{V_i}{V_{CL}}$$  \hspace{1cm} (1)

$$D_x + D_y + D_z \leq 1 - D \Rightarrow V_i \leq \frac{1-D}{D} V_{CL}$$  \hspace{1cm} (4)

$$D_x + D_y \leq 1 - D \Rightarrow V_{CL} \leq \frac{V_{C2}}{D}$$  \hspace{1cm} (5)

respectively. The limit condition of the DCM operation in terms of input and output voltage can be derived from (4)–(6) as,

$$\frac{V_i}{V_o} \leq \frac{(1-D)^2}{D^3}$$  \hspace{1cm} (7)

Note that from (7), the conditions for the three inductor currents to be in DCM can always be satisfied over the entire ac line period, while the worst case must be satisfied when $V_i = V_{in}$. Moreover, the assumption that the current in $L_3$ reaches the zero level after the currents in $L_1$ and $L_2$ is also being satisfied by (7). On the other hand, operating $L_3$ in BCM requires the sum of the normalized subinterval lengths to be unity, i.e. $D+D_1+D_2+D_3=1$; hence, the inequality in (6) will be modified to $V_{o} = D V_{C2}/(1-D)$.

For the sake of comparison, Fig. 4 illustrates the voltage gain ($M=V_o/V_{in}$) of the B5 converter at the boundary of DCM/CCM, as well as for other previously proposed large step-down topologies presented in [18] and [19]. It is clear from Fig. 4 that the B5 converter has an advantage of an extended duty-cycle range. That is, for the same duty-cycle $D$, the B5 converter provides the lowest voltage gain compared to the other topologies. This large step-down conversion ratio makes the proposed B5 converter more suitable for applications with a high difference between the input and output voltages.

B. DC-link capacitor voltages, $V_{C1}$ and $V_{C2}$

The dc capacitor voltages, $V_{C1}$ and $V_{C2}$, determine the voltage stress across the semiconductor devices. Therefore, they are an important design factor. The dc voltages $V_{C1}$ and $V_{C2}$ can be found by applying charge balance on $C_1$ and $C_2$ in a half-line cycle, $T_L/2$, i.e.

$$\int_{t_1}^{t_1+T_L/2} i_{Cn}(t) \, dt = \frac{1}{2} D_{Cn}$$  \hspace{1cm} (8)

$$\int_{t_1}^{t_1+T_L/2} i_{Cn}(t) \, dt = \frac{1}{2} D_{Cn}$$  \hspace{1cm} (9)

The average current drawn from capacitors $C_1$ and $C_2$ during one switching period $T_s$, $<i_{Cn}(t)>_{T_s}$ can be found from Fig. 3 as,

$$<i_{Cn}(t)>_{T_s} = \frac{D_{Cn}}{2}$$  \hspace{1cm} (10)

$$<i_{Cn}(t)>_{T_s} = \frac{D_{Cn}}{2}$$  \hspace{1cm} (11)

Fig. 4. Voltage conversion ratio $M$ as a function of duty-cycle $D$. ($D'=1-D$)
Equation (8) must equal zero at steady-state. Evaluating (8) for both (9) and (10) gives,

\[
V_{C1} = \frac{V_{C2}}{2} \left[ 1 + \sqrt{1 + \frac{2L_2}{L_1M_{C2}^2}} \right]
\]

(11)

\[
V_{C2} = V_m \times \sqrt{\frac{L_3}{2L_1}}
\]

(12)

where \(M_{C2} = \frac{V_{C2}}{V_m}\). Thus, for a given value of \(M\), the capacitor voltages \(V_{C1}\) and \(V_{C2}\) are independent of load current variation and they are a function of the inductance ratio \(L_2/L_1\) and \(L_3/L_1\), respectively.

Fig. 5 shows the variation in the capacitor voltages \(V_{C1}\) and \(V_{C2}\) as a function of the line voltage \(v_{ac}\), with the ratios \(L_1/L_2 = 4.8\) and \(L_1/L_3 = 46\) as a parameter. The values of \(L_1\), \(L_2\), and \(L_3\) were chosen to be equal to their maximum permissible value required to maintain DCM operation. Such values minimize the voltage/current stress on the semiconductor devices. Referring to Fig. 5, the voltage \(V_{C1}\) is about 64 V at low-line input voltage and about 200 V at high-line input voltage. On the other hand, the maximum voltage across \(C_2\) is about 70 V at high-line input voltage. Therefore, capacitors with rated voltages 250 V and 100 V could be used for \(C_1\) and \(C_2\), respectively.

Furthermore, when \(L_1\) is in BCM, then the duty cycle \(D\) can be obtained from (6) and (12) as,

\[
D = \frac{V_o}{V_{C2} + V_o} \left[ 1 + \frac{1}{M} \sqrt{\frac{L_2}{2L_1}} \right]
\]

(13)

Equation (13) shows that the duty cycle \(D\) is independent of load current variation, and yet it must be kept constant for a given value of \(M\). This implies that the switching frequency must vary in order to compensate for load current variation. Fig. 6 shows the variation of duty cycle \(D\) as a function of ac line voltage for different values of inductance ratio \(L_1/L_3\).

C. Voltage conversion ratio, \(M\)

The voltage conversion ratio \(M = \frac{V_o}{V_m}\) in terms of circuit parameters can be found by applying the input-output power balance principle to the circuit in Fig. 1. The average input power during one half-cycle of the line voltage is,

\[
\overline{p_{in}}(t) < \frac{1}{2} \int_{T_s/2}^{T_s/2} \frac{V_{in}(t) < i_{in}(t) > T_s dt}{T_s}
\]

(14)

From Fig. 3, the average input line current over one switching period, \(<i_{in}(t) > T_s\), is,

\[
<i_{in}(t) > T_s = \frac{2}{T_e} \int_{0}^{T_s/2} \frac{V_{in}(t)}{R_{el}} dt
\]

(15)

where \(R_{el}\) is the emulated input resistance of the converter and it is equal to,

\[
< i_{C2}(t) > T_s = \frac{1}{2} \left[ (D + D_x + D_y) I_{L2pk} - DI_{L3pk} \right]
\]

(10)

For a given operating point \((M, R_L)\), the emulated input resistance in (16) is constant if both \(D\) and \(T_s\) are kept constant. Thus, the converter presents a linear resistive load to the ac power main, which is the perfect condition for unity power factor operation. Evaluating (14) and applying the power balance between the input-output ports, the desired voltage conversion ratio \(M\) is,

\[
M = \frac{D}{\sqrt{2K}}
\]

(17)

where the dimensionless parameter \(K\) is defined by,

\[
K = \frac{2L_1}{R_L T_s}
\]

(18)

Note that (17) is always valid regardless of the operation mode condition of \(L_2\) and \(L_3\) provided the DCM operation of the input buck-boost stage is assured.

D. Inductances \(L_1, L_2,\) and \(L_3\)

To ensure that the power stages of the proposed converter are operated in DCM, the inductor currents \(i_{L1}, i_{L2},\) and \(i_{L3}\) must be fully discharged to zero in every switching period. The critical value of \(K\) \((K_{crit})\) required for \(L_1\) to be in DCM is found by rearranging (7) and (17) which gives,

\[
K_{crit} = \frac{1}{2} \left( \frac{1-D}{D} \right)^4
\]

(19)

For values of \(K \leq K_{crit}\) then \(L_1\) is operating in DCM; otherwise, \(L_1\) will enter the CCM region.
The critical value of \( L_1 \) (\( L_{1,\text{crit}} \)) required for DCM operation occurs at maximum output power (\( P_{\text{out}} \)) and at the peak of the low-line voltage (\( V_{\text{m,min}} \)). Using (17), (18), and (19) gives \( L_{1,\text{crit}} \) as:

\[
L_{1,\text{crit}} = \frac{R_{1,\text{min}} \times T_s}{4} \left[ 1 + \frac{1}{3} \left( \frac{B}{2} \right)^{1/3} \left( (1 + K_0)^{1/3} - (K_0 - 1)^{1/3} \right) \right]^2
\]

where

\[
K_0 = \sqrt{\frac{1 + 4A^2}{27B}}, \quad A = \frac{6 - M_{\text{max}}}{3M_{\text{max}}}
\]

\[
B = \frac{2M_{\text{max}}^2 - 18M_{\text{max}} + 27}{27M_{\text{max}}^2}, \quad M_{\text{max}} = \frac{V_o}{V_{\text{m,min}}}
\]

For values of \( L_1 > L_{1,\text{crit}} \), the converter enters the CCM region where (17) is no longer valid. In CCM, the voltage conversion ratio in CCM can be only two operating stages per switching cycle, Fig. 2(a) and (b). The average value of C\(_1\) and C\(_2\) currents during a half-cycle is derived based on simulation software. For the above mentioned reasons, the long computation time when it is implemented in a simulation program to predict the steady state and large signal dynamic characteristics of the real circuit. Moreover, the averaged model can greatly reduce the computation time when it is implemented in a simulation software. For the above mentioned reasons, the averaged model of the proposed rectifier of Fig. 1 is developed in this section.

The averaged model for the converter of Fig. 1, when the three inductor currents operate in DCM, is derived based on averaging various waveforms over one switching cycle, \( T_s \). The average value of the output diode current during one switching period is given by,

\[
\langle i_{D5}(t) \rangle = \frac{V_2}{R_3} \langle v_o \rangle
\]

whereas evaluating (9) and (10) gives,

\[
\langle i_{C1}(t) \rangle = \frac{V_2}{R_{e1}} \langle v_{C1} \rangle - \frac{(V_{C1} - V_{C2})}{R_{e2}} \langle v_{C2} \rangle
\]

\[
\langle i_{C2}(t) \rangle = \frac{V_{C1}}{R_{e2}} \langle v_{C2} \rangle - \frac{V_{C2}}{R_{e3}} \langle v_o \rangle
\]

Using (15), and (24)-(26), the power stage circuit in Fig. 1 may be represented by its large signal averaged model shown in Fig. 7. Similar to the conventional buck-boost converter, the averaged circuit model in Fig. 7 predicts that the input port is purely resistive (\( R_{\text{e1}} \)) which is the perfect theoretical condition for achieving unity power factor. Fig. 8 shows the simulated transient waveforms of the three capacitor voltages based on the averaged circuit model of Fig. 7. These waveforms are plotted for the following values: \( v_i = 110 \text{ Vrms} @ 50 \text{ Hz}, P_{\text{out}} = 35 \text{ W}, V_o = 12 \text{ V}, f_s = 60 \text{ kHz}, L_1 = 180 \mu \text{H}, L_2 = 100 \mu \text{H}, L_3 = 15 \mu \text{H}, C_1 = C_2 = 800 \mu \text{F} \) and \( C_0 = 68 \mu \text{F} \).

IV. DESIGN CONSIDERATIONS

In general, when operating a converter into DCM region, the current stress on the converter components becomes relatively large when compared to CCM operation. This is one disadvantage of DCM operation, which limits this operating mode to low power applications (<150W). Considerations for the rating and selection of the various components for the proposed converter are presented next.

A. Semiconductor stresses

The semiconductor peak voltage and rms current stresses are shown in Fig. 9. These curves are plotted for \( P_{\text{out}} = 35 \text{ W}, V_{i1} = 12 \text{ V}, f_s = 60 \text{ kHz}, L_1 = L_{1,\text{crit}}, L_2 = L_{2,\text{crit}}, \) and \( L_3 = L_{3,\text{crit}}. \) It is clear from Fig. 9 that the current stress in the semiconductor devices (except for the output diode \( D_5 \)) tends to decrease as the input ac-line voltage increases. It is also evident from Fig. 9 that the switch peak voltage at high line is below 600 V (about 575V). Therefore, it suffices to use a 600-V power MOSFET for this particular application.

The closed form expression for the rms currents through the passive elements (inductors and capacitors) can be derived and they are given by,

\[
I_{L1,\text{rms}} = \frac{V_m}{R_{e1} \sqrt{3} D} \sqrt{2 + \frac{16V_m}{3\pi V_{C1}}}
\]

\[
I_{L2,\text{rms}} = \frac{2(V_{C1} - V_{C2})}{R_{e2} \sqrt{3} D V_{C2}}
\]

\[
I_{L3,\text{rms}} = \frac{2V_{C2}}{R_{e3} \sqrt{3} D \left( 1 + \frac{V_{C2}}{V_o} \right)}
\]
The converter of Fig. 1 is simulated using PSpice with real semiconductor models to simulate the switches. The inductors \( L_1, L_2, \) and \( L_3 \) are selected to operate in DCM region. The circuit components and the input and output data specifications are given by: \( V_{ac} = 110 \text{ Vrms} \) at 50 Hz, output voltage \( V_o = 12 \text{ Vdc}, P_{out} = 35 \text{ W}, L_1 = 180 \mu\text{H}, L_2 = 100 \mu\text{H}, L_3 = 150 \mu\text{H}, C_1 = C_2 = 680 \mu\text{F}, C_0 = 100 \mu\text{F}, \) switching frequency \( f_s = 60 \text{ kHz}, \) bridge diodes and D_2 MBRS3201T3: 200V/3A schottky rectifier with \( V_F < 0.59V, \) for diode D_5: STTH2003CR: 300V/10A schottky rectifier with \( V_F = 0.85 V, \) for diodes D_3, D_4, and D_5: STPS20120CT: 120V/10A schottky rectifier with \( V_F = 0.54 V, \) and for the power witch Q: STY60NM50: 500V/60A with \( R_{DS-ON} = 45 \mu\text{m}2. \) A high frequency input- filter \( (L_f = 2 \text{ mH}, C_f = 0.1 \mu\text{F}) \) is inserted at the input port to filter the ripples in the rectified line current. Fig. 10(a) shows that the input line current follows the input line voltage. The percent of the total harmonic distortion in the input line current is 0.4% (up to the first 25 harmonic orders). The waveforms of the three inductor currents near peak input voltage are depicted in Fig. 10(b) for several switching periods. Fig. 10(b) correctly demonstrates the DCM operating mode. Moreover, it is clear from Fig. 10(c) that the output voltage \( V_o \) has insignificant low frequency ripple which can be further reduced by simply regulating the output voltage. The simulated results confirm the operating principles of the proposed B^2 PFC rectifier.

A prototype of the proposed converter in Fig. 1 is built and tested to verify the operating principle of the proposed converter. The circuit parameters were all the same as those for simulation. Fig. 11(a) depicts the experimental steady-state input voltage and filtered input line current waveforms. It is evident from Fig. 11(a) that the proposed mode of operation gives a nearly sinusoidal current waveform. The measured THD of the input line current is 1.53% (up to the first 11 harmonic orders). Fig. 11(b) shows the discontinuous inductor currents \( i_{L1}, i_{L2}, \) and \( i_{L3} \) during switching cycle. Moreover, the waveforms of the output voltage and the voltages on the energy storage capacitors \( V_{C1} \) and \( V_{C2} \) are shown in Fig. 11(c). It can be observed form Fig. 12(c) that the output voltage is almost pure DC with extremely low frequency (twice the line frequency) voltage ripples. The measured power conversion efficiency is about 80.6%. The experimental waveforms are in good agreement with the simulated ones given in Fig. 10.

VI. CONCLUSION

In this paper, a single-switch single-stage unity power factor has been proposed by integrating a buck–boost converter with a buck and a buck-boost converter. The proposed converter has several merits, such as providing sinusoidal input current with low harmonic distortion, low DC-link voltage, well-regulated output voltage, and voltage at maximum power throughput.
extended voltage conversion ratio capability. Automatic power factor correction can be achieved by operating the input buck-boost stage in the DCM, while operating the output buck-boost stage at the boundary of DCM/CCM produces a well-regulated output voltage with a negligible low-frequency voltage ripple, and it reduces the semiconductor voltage stresses, as well as the conduction losses. The steady-state behavior has been studied and analyzed with performance characteristics, and a large-signal averaged model is presented. It has been shown that the proposed converter can achieve very low output voltage with an extended duty-cycle compared to the other buck-boost topologies. This makes the proposed converter well suited for universal offline PFC and/or extreme voltage step-down applications. The feasibility of achieving low conversion ratio has been demonstrated by simulation and experimental results.

Fig. 10. Simulated waveforms.

Fig. 11. Experimental waveforms.