A Novel Dual Gate Strained-Silicon Channel Trench Power MOSFET For Improved Performance

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ABSTRACT

In this paper, we propose a new dual gated trench power MOSFET with strained Si channel using the Si$_{0.8}$Ge$_{0.2}$ base and graded strained Si accumulation region using compositionally graded Si$_{1-x}$Ge$_x$ buffer ($x$ varying from 0 to 0.2 from the drift region to the base region) in drift region. We show that the introduction of strain in channel and accumulation region results in about 10% improvement in its drive current, about 20% reduction in the on-resistance and about 72% improvement in peak transconductance with only about 12% reduction in the breakdown voltage when compared with equivalent conventional device. Furthermore, the structure contains two separated gates out of which one controls the inversion charge in the channel region and the other one controls the accumulation charge in the accumulation region. The separate control of the charge in different regions further improves the device performance. We show that by applying a suitably high fixed positive voltage at the accumulation gate improves the device performance parameters up to about 10%.

Keywords: Strained Si, Si$_{1-x}$Ge$_x$, Trench Gate, Dual gate, Power MOSFET, Compositionally Graded Si$_{1-x}$Ge$_x$ buffer

1 INTRODUCTION

A trench gate MOSFET is used in many medium to low voltage power applications [1-5]. In various applications the main requirements of a power MOSFET are the low on-state resistance, high drive current, low switching delays and high transconductance with a considerably high immunity for the inductive switching damages. However, while designing a power MOSFET, meeting all these requirements is not possible in conventional structures and the device can not be used efficiently in many applications if designed for one specific application. To overcome these difficulties, we propose a new dual gate trench power MOSFET that provides many advantages over conventional power MOSFETs like (a) high drive current as it has high carrier mobility due to the strained Si in the channel region [6, 7], (b) better inductive switching immunity as it provides the confinement of carriers near the trench sidewalls in accumulation layer [5] and (c) higher peak transconductance with additional capability of in-circuit parameter tuning for efficient use in different applications.

2 DEVICE STRUCTURE AND SIMULATION

Fig. 1 shows the schematic cross-sectional view of the proposed DGSCT device. It contains two trenches in such a way that shallower trench is inside the deep trench and touches its boundaries. This structure allows the formation of two gates with strained Si channel as depicted in Fig. 1. The deeper gate (called accumulation gate here after and denoted by $G_{\text{Acc}}$) controls the accumulation charge and the shallower gate (called inversion gate and denoted by $G_{\text{Inv}}$) controls the inversion charge of the strained channel. It uses P-type Si$_{0.8}$Ge$_{0.2}$ in the body and a compositionally graded N-type Si$_{1-x}$Ge$_x$ buffer layer as a part of the drift region.

Fig. 1 Cross-sectional view of the DGSCT device

The compositionally graded SiGe buffer has been realized by a 10 layer stack with varying Ge composition from 0 at the drift region to 20% at the body region. Similarly, we have realized the graded strained Si layer adjacent to the graded SiGe buffer layer. The use of graded strain results in the smoothing of energy band discontinuity faced by the carriers while moving from channel to the accumulation region.
Table 1: Device parameters used in simulations

<table>
<thead>
<tr>
<th>Device Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source/Drain doping</td>
<td>$1 \times 10^{19}$ atoms/cm$^3$</td>
</tr>
<tr>
<td>Source thickness</td>
<td>100 nm</td>
</tr>
<tr>
<td>Body doping</td>
<td>$5 \times 10^{17}$ atoms/cm$^3$</td>
</tr>
<tr>
<td>Body thickness</td>
<td>500 nm</td>
</tr>
<tr>
<td>Ge mole fraction in the SiGe buffer layer, $x$</td>
<td>0-0.2</td>
</tr>
<tr>
<td>SiGe buffer layer doping</td>
<td>$1 \times 10^{16}$ atoms/cm$^3$</td>
</tr>
<tr>
<td>SiGe buffer thickness</td>
<td>500 nm</td>
</tr>
<tr>
<td>Si Drift region doping</td>
<td>$1 \times 10^{16}$ atoms/cm$^3$</td>
</tr>
<tr>
<td>Si Drift region thickness</td>
<td>2.5 $\mu$m</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>50 nm</td>
</tr>
<tr>
<td>Strained Si thickness</td>
<td>20 nm</td>
</tr>
</tbody>
</table>

Using 2D numerical simulations performed with ATLAS device simulator [8], we show a comparison of the proposed DGSCT device with the equivalent conventional device that has similar doping concentration and geometry but only single trench with no SiGe region. Various parameters used in simulations are listed in table 1.

3 RESULTS AND DISCUSSION

The DGSCT device has independent control of its two gates. Therefore, it may be operated in two modes, namely, (a) standard mode where we externally short both the gates and (b) extended mode where the different voltages may be applied to get maximum benefit of the separate accumulation gate control. The structure results in various advantages in standard mode and these advantages may further be improved in extended mode, as discussed in the following subsection.

3.1 Standard mode

The use of strained Si causes energy band discontinuity in the body region along the transverse direction to the current flow. This results in the carrier confinement in the channel region. Similarly, the carriers are also confined in the gradually strained accumulation region and this confinement reduces as we go towards the drain side. The carrier confinement near the trench sidewalls results in better gate control of the channel charge and therefore, we get many advantages in DGSCT device when operated in standard mode. We get lower threshold voltage as compared to the conventional device as shown in log $I_{DS}$ vs $V_{GS}$ plot in Fig. 2. It indicates a shift in threshold voltage from 2.1 V in conventional device to 1.5 V in the proposed DGSCT device. The better gate control also results in high transconductance as shown in Fig 3. The peak transconductance of DGSCT device in linear mode of operation (at $V_{DS} = 0.1$ V) is about 70% larger as compared to the conventional device. The higher mobility of the strained Si also improves the drive current and hence the on state resistance of the device, as depicted in the output characteristics shown in Fig. 4. It amounts to around 20% reduction in on state resistance.

![Fig. 2: $I_{DS}$-$V_{GS}$ Characteristics of DGSCT and Conventional Devices](image)

![Fig. 3: Transconductance as a function of gate over drive voltage at $V_{DS} = 0.1$ V](image)

![Fig. 4: Output characteristics of DGSCT and conventional devices at different gate overdrive voltages](image)

These improvements we get at the cost of reduced breakdown voltage that reduces by 12% in DGSCT device as compared with the conventional device due to use of SiGe body region, as shown in Fig. 5.
3.2 Extended mode

The device parameters may further be improved by keeping accumulation gate at some fixed positive potential.

![Graph showing I_DS vs V_DS characteristics with gate connected to source showing breakdown voltage comparison of DGSCT and conventional devices](image)

Fig. 5: Log I_DS vs V_DS characteristics with gate connected to source showing breakdown voltage comparison of DGSCT and conventional devices

![Graph showing the effect of VG_ACC on various parameters](image)

Fig. 6: The effect of VG_ACC on various parameters

The effect of accumulation gate voltage on various performance parameters are shown in Fig. 6 for bias conditions of VG_INV = 5.0 V and V_DS = 0.1 V on the left Y-axis. We found that the device performance improves by increasing the fixed potential of accumulation gate. This occurs because of the ease in carrier transport from channel region to the accumulation region. However, the accumulation of carriers in the drift region due to high positive G_Acc voltage causes the depletion region at the accumulation-body junction to reach up to the source at the V_DS much lower than the breakdown voltage obtained in standard mode, resulting in a lower effective breakdown voltage in extended mode. The effect of increasing the accumulation gate voltage on the breakdown voltage of the device is illustrated in Fig. 6 on right Y-axis.

Thus we see that a DGSCT device may be tuned for better performance parameters for a given application if breakdown voltage requirement permits so. For example, for low voltage (~5.0 V) light load applications, one can set the G_Acc voltage at 10.0 V to get excellent performance, and for moderate breakdown voltage (20.0 V – 30.0 V) applications the G_Acc bias voltage may be reduced accordingly. The same device may be used in standard mode for high breakdown voltage requirement with inductive load switching capability.

4 CONCLUSIONS

For the first time, using two-dimensional simulation, we have demonstrated the strained Si channel in trench power MOSFET produced by using Si_{1-x}Ge_x body improves the device performance parameters such as current drivability, peak transconductance and on-state device resistance. Furthermore, the sectioning of the gate into two parts in order to have separate control of accumulation charge gives the flexibility of applying different voltages at the two gates of thus obtained DGSCT device. We have shown that by using this feature, we can achieve a further improvement in the performance of the device at the cost of reduced breakdown voltage, by suitably adjusting the accumulation gate voltage.

REFERENCES