Efficient and Accurate Modeling and Simulation Techniques for Substrate Coupling Analysis in Deep Submicron Mixed-Signal IC’s

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Abstract – Phase-locked loops (PLLs) are used in wireless receivers to implement a variety of functions, such as frequency synthesis, clock recovery, demodulation, and mixed-signal integrated circuits. Substrate coupling noise is a key problem in today’s large mixed-signal systems. Switching-noise generated by digital circuits can be coupled to sensitive analog circuits through the substrate, can degrade circuit performance. Substrate noise in integrated circuits is a major impediment to mixed-signal integration. Accurate simulation is therefore, needed to investigate generation, propagation, and impact of substrate noise. The estimating an accurate modeling of noise coupling effects is a major challenge for designers. In this paper, we introduce novel substrate noise estimation and describe a fast and accurate simulation for modeling substrate coupling noise in mixed-signal RF IC design. Using a three-dimensional finite element method for extraction of substrate parasitic elements is developed. This approach allows the designer to maintain a grasp of the fundamentals using coarse models at the early stage of the design and to eventually gain insight on the lower order effects by gradually increasing the level of detail as the design develops. Copyright © 2010 Praise Worthy Prize S.r.l. - All rights reserved

Keywords: phase-locked loop (PLL), substrate coupling, substrate noise, Mixed-signal, phase noise, Three-dimensional finite element method

I. INTRODUCTION

A significant challenge in system-on-a-chip integration is the need to implement broadband analog circuits on the same die as the large complex digital circuits. Single chip mixed-signal designs combining digital and analog blocks built over a common substrate provide reduced levels of low cost, power dissipation, and smaller package count. But one of its disadvantages is that the most important fault is substrate noise. Substrate noise can affect the proper operation of both analog and digital integrated circuits. Fast switching logic components inject current into the substrate causing voltage fluctuations, which can affect the operation of sensitive analog circuitry through the body effect. Due to body effect change in transistors’ threshold voltages, also due to the time and monetary constraints of fabrication, detailed simulations are a must to ensure functionality and will help reduce the design life cycle. The coupling noise, if not prevented, can undermine correct functionality of the system [1]-[2]-[9]-[10]-[11].

Fig. 1 presents an illustration of the substrate-coupling problem. It shows a mixed-signal circuit, with the digital part introducing substrate noise via the supply line that is connected to the substrate. If the digital circuit switches, the substrate contact exhibits a noise signal because of the resistive and inductive impedance of the supply line combined with the supply current. The resulting noise is transferred through the substrate and picked up by the analog circuit, which consequently exhibits degraded performance.

With this high integration complexity and with increasing circuit speeds, the detrimental effect of substrate coupling becomes more and more severe in design considerations. Also, knowledge of substrate noise can help the designers to optimize the layout of their circuits. The information about substrate coupling can be useful to circuit designers because it helps them to quickly identify and then remedy the dominant sources of coupling and also to avoid expensive redesigns and multiple fabrications run [1]-[2]-[3]-[4]-[6]-[7]. Thus, it is becoming more and more apparent that substrate noise...
is a topic that merits further and more detailed investigation [2]-[4]-[8].

The ever-increasing demand to integrate all circuit components on the same chip gives rise to same critical noise tolerance requirements for sensitive analog circuits inside the chip. PLLs are ubiquitous circuit blocks in RF and mixed-signal integrated circuits. They are extensively utilized as on-chip clock generators to synthesize and de-skew a higher internal frequency from the external lower frequency [12]-[13]-[14]-[15]. In all the above applications, the random temporal variation of the phase, or jitter, is one of the most critical performance parameters. In current SOC era, the substrate coupling must be considered, but in most presented approach, this phenomenon has not yet been seriously addressed.

In this paper, we propose a novel concept of Finite Element Method (FEM) for fast, yet accurate, extraction of couplings between substrate contacts was developed, for extraction parasitic elements in mixed-signal integration using ANSYS software. ANSYS software enables engineers and designers accurately simulate their electromagnetic and electromechanical devices. Based on the Finite Element Method (FEM) and in this method is based on the Maxwell. Maxwell’s law is the leading electromagnetic field simulation software used for the design and analysis of 3D structures.

We use ANSYS software to create a large threedimensional mesh model of the couplings between substrate contacts extracted using FEM. We assume that a set of contacts has been defined on the substrate, possibly consisting of active devices, connection to the power rails, backplane, etc.

Finally, we investigate the effect of substrate coupling on PLL parameters. This is accomplished by using an efficient analytical model for substrate. The analytical model is verified by simulation of CMOS PLL circuit designed in a 90nm standard CMOS processes by switching inverters chain that emulate the switching of the digital circuit.

II. BACKGROUND ON SUBSTRATE COUPLING MODELING AND PROBLEM FORMULATION

Several approaches have been presented in the past to attempt to quantify the effects of noise coupling through the substrate. Examples of such techniques include Boundary Element Method (BEM), Finite Element Method (FEM) and Finite Difference (FD). Boundary Element Methods have been applied with some success to the problem of modeling substrate coupling. By requiring only the discretization of the relevant boundary features, these methods lead to smaller matrix problems. However, the matrices they produce are dense, limiting their use to be small to medium problems. Therefore, speeding up the computations in boundary-element formulations is crucial to obtaining accurate models for large substrate-coupling problems [1]-[2]-[3]-[4]-[5].

Methods based on differential equations, such as Finite Element Method (like the one described here), and Finite Difference numerical methods can compute all the currents and voltages in the substrate, given a pattern of injected currents. These techniques perform a full domain discretization on the large but bounded substrate volume and can easily handle irregular substrates (such as wells or doping profiles). Because these methods rely on volume meshing of the entire substrate, the number of unknowns resulting from the discretization can easily become very large [6]-[7]. However, three-dimensional volume of the substrate is discretized leading to large but sparse matrices; thus, these methods, with appropriate solution algorithms, is a competitive option for substrate-model extraction in large, dense designs. After extracting the model, designers can evaluate it at many times to analyze substrate coupling noise effects. For the most part, designers will use such models in standard circuit simulators such as Hspice. Desirable model characteristics, therefore, include easy incorporation in standard circuit simulators, high accuracy, and low evaluation cost.

III. SUBSTRATE COUPLING NOISE

Analyzing the effects of substrate coupling requires a model of such couplings to be obtained and used in a verification framework. Such as verification is typically done at the electrical level by means of a circuit simulator which is given a substrate model, together with the models of the devices. Each switching node can introduce some noise to the substrate. Finite resistance of substrate means that this noise can be transferred to adjacent devices. Fig. 2, show Substrate noise coupling phenomena.

The noise currents are injected from the devices into the substrate through the devices-substrate interface, and then noise propagates through the substrate medium to reach other locations on the same substrate. The nature of such propagation depends on the substrate resistivity and isolation structures implemented as well as grounding techniques and frequency of operation. Finally, the substrate noise is received at the sensitive circuit node.

Silicon substrates that are in wide commercial use today can be broadly categorized as high-resistivity and low-resistivity bulk types. Fig. 3, shows examples of such types. Low-resistivity substrates are generally preferred.
for their good latch-up suppression property [1]-[2]-[3]-[4]-[5]-[6], which is an important consideration in CMOS. Surface isolation techniques, such as guard-rings are more effective in high-resistivity substrates. At frequencies up to several GHz, silicon substrates exhibit a behavior that can be approximated as being purely resistive [8].

In CMOS devices, hot-electron effects also cause injection of majority-carriers into the substrate [6]. Hot electron effects are observed when the field in the depleted drain-end of the transistor becomes large enough to cause impact ionization and generate electron-hole pairs. The dependence of the hot-electron induced substrate current \( I_{sub} \) on the device operating current is given by the following semi-analytical expression.

\[
I_{sub} = K_1 (V_{ds} - V_{sat}) I_d \exp\left(-\frac{K_2}{V_{th} - V_{ds}}\right)
\]

Where \( I_d \) is the drain current, \( V_{ds} \) is the drain-to-source voltage and \( V_{sat} \) is the drain-to-source voltage at saturation. \( K_1 \) and \( K_2 \) are semi-empirical constant [6].

IV. FEM TRIDIMENSIONAL MODEL

Fig. 4 shows the profile of a typical substrate, consists of a thick highly doped substrate and a thin lightly doped epitaxial layer and backplane. We assume that the substrate is a stratified medium composed of several homogeneous conductive layers. A deposition process using appropriate materials builds devices on top of these layers. Ports or contacts at the top of the stack of layers correspond to the lightly doped, strongly conductive areas where the circuit interacts with the substrate. Back plate contacts can improve isolation but increase the design cost [3].

FEM discretization can handle any number of substrate vertical profiles, deep trenches, buried and epitaxial layers, guard-rings, and so on, as long as the mesh spacing is accurate enough. In ICs, for frequencies up to a few GHz, the wavelengths of the magnetic fields far exceed a typical die’s dimensions [6]. Thus, we can assume a quasi-approximation.

In order to obtain an electric model of the mesh we start with Maxwell’s law using the quasi-static approximation.

Maxwell accurately solves static, frequency-domain and time-varying electromagnetic fields. Which describe the behavior of the electric and magnetic fields, here we consider only the electric field. This approximation is acceptable to current mixed-signal designs and technologies but may soon need to be revised.

\[
\sigma \nabla E + \varepsilon \frac{\partial \nabla E}{\partial t} = 0
\]

In this equation, \( E \) is the electric field, \( \sigma \) is the medium’s conductivity, and \( \varepsilon \) its permittivity. For the cuboid involving that node can be approximately calculated as

\[
\nabla E_i \approx \frac{1}{\gamma} \sum_j E_j S_{ij}
\]

Where \( S_{ij} \) is the surface common to nodes, \( i \) and \( j \). \( E_{ij} \) the electrical field normal to that surface and \( \gamma \) the volume of cuboid and the summation takes into account all cuboid surfaces.

A simple, but not unique, way to solve equation 2 is to perform a spatial discretization of the substrate volume and approximate the electric field vector between adjacent nodes in this 3D grid, using a Finite-Difference operator.

\[
E_i \approx \frac{V_i - V_j}{d_{ij}}
\]

Where \( d_{ij} \) is the distance between adjacent nodes, \( i \) and \( j \) and \( V_i \) and \( V_j \) the scalar potential at those nodes in the volume grid. For instance, a standard seven-point stencil leads to
\[ \sum_{j} \left[ G_{ij} (V_i - V_j) + C_{ij} \left( \frac{\partial V_i}{\partial t} - \frac{\partial V_j}{\partial t} \right) \right] = 0 \] (5)

Where \( G_{ij} = \sigma \frac{S_{ij}}{d_{ij}} \) and \( C_{ij} = \varepsilon \frac{S_{ij}}{d_{ij}} \).

Equation 5 can be modeled as a simple linear network of lumped circuit elements, walk model that is based on resistances and capacitances, organized as three-dimensional grid, as shown in Fig. 5.

![Fig. 5. Model of the substrate as a 3D mesh of resistances and capacitances connecting nodes in the mesh [6].](image)

**V. MODEL EXTRACTION**

Capacitance and admittance computation is the primary goals of an electrostatic analysis. Electrostatic field analysis is important in Micro Electro Mechanical Systems (MEMS) to determine both capacitance and admittance, which are typically used to actuate devices such as comb drives. Finite element simulation can readily compute and extract a parasitic element in substrate noise. Using the 3D mesh model in ANSYS simulator is prohibitive due to model’s sheer size. Calculate capacitor and admittance using this method, the two must be calculated separately.

CMATRIX and GMATRIX are used as a macro to automate the computation of a systems capacitance and admittance matrix. They are applicable to any number of contacts, with any number of dielectric materials present. CMATRIX and GMATRIX compute the self and mutual capacitance and admittance of each contact and derive the system ground and lumped matrices. CMATRIX and GMATRIX are useful for extracting lumped capacitance and admittance for use in a MEMS system level simulation. Fig. 6 illustrates a three-contact system (one contact is backplane) is the circuit model of Fig. 4. Fig. 6 can be a model for accurate capacitance and admittance, which is accurately and directly computed from the procedure for using the method, is as follows:

1- Define the material properties permittivity and resistivity substrate.
2- Create an electrostatic finite element model of substrate 3D and assign physics attributes to each region within the model.
3- Choice element type capacitance (SOLID 122) and admittance (SOLID 231).
4- Substrate mesh scheme, for high speed computing. The next section explains a way to mesh scheme substrate.
5- Apply boundary conditions and loads.
6- Select the nodes on the surface of each contact and group them into node components.
7- Calculate the capacitance and admittance matrix, Issue of SOLVE command.

The CMATRIX and GMATRIX extracted based on above seven stages and output is a matrix. This matrix, the macro derives the lumped matrix which provides the self and mutual capacitance and admittance between contacts. These lumped values can be used as capacitors and admittances in a HSPICE circuit simulation. The results can be listed on the screen, output to a file, or accessed by the ANSYS APDL macro language.

**VI. MESH METHOD IN SUBSTRATE**

Meshing is an important part of the computer-aided engineering (CAE) simulation process. The mesh influences the accuracy, convergence and speed of the solution. Furthermore, the time that is needed to create a mesh model is often a significant portion of the time it takes to get results from a CAE solution. Therefore, in order to calculate more quickly and reduce time and reduce consumption of memory and CPU, it is used the levels, shown in Fig. 7.

Mesh scheme is an experiential work, so mesh scheme for getting more accurate answers is unsuitable, because it is needed a mesh scheme smaller. So, solving this mesh scheme needs very long time and memory consumption. For solve this problem, we design a good mesh scheme based levels as shown in Fig. 7.

Fig. 7 shows meshing structures for substrate modeling in 3D to other levels. The used mesh scheme in
the important area where the electric field varies rapidly, such as devices or contacts of the depletion regions, is level 3 and in other area that is not important, it can be used from level 1, and for other areas it can be used from level 2.

With this method, we can get the best answer nearly accurate and need to very little time and less memory.

Fig. 7. A 3D representation of multilevel meshing

**VII. RESULTS AND DISCUSSION**

In order to investigate the accuracy and efficiency of the proposed method, we present several examples and compare the results with those obtained by other methods. At first, we use two equal size contacts of dimensions 10µm×10µm located on the substrate of h=400µm and ρ=10Ω-cm, we have extracted the parasitic capacitance $C_{21}$ between the two square-contacts, and the result of our work has been compared with several methods. Fig. 8 shows a result between analytical integration [3] and IE3D, and Fig. 9 shows output software MATLAB Programming is based on method analytical integration [3] and Fig. 10 shows our method. We observe that our models present a very good agreement with IE3D simulation results and analytical integration [3] and other techniques of MATLAB software.

Table I shows the simulation results using the discrete cosine transform method (DCT), finite difference method reported in [1], and method in [3] and MATLAB method and our proposed method.

Another example is presented in order to compare our analytical solution with other methods in the literature. We use four equal size contacts of dimensions 20µm×20µm located on the substrate of h=100µm and ρ=10Ω-cm, and size substrate is 1000µm×1000µm, as shown in Fig. 13, Fig. 14 shows the simulation results obtained from Finite difference method [1], the DCT technique proposed in [4], the method in [3] and MATLAB method and our proposed method. Table III illustrates the values of several selected parasitic resistance extracted using our analytical ANSYS method, MATLAB and analytical integration methods.
Fig. 12. Simulation single contact with ANSYS software

TABLE I

<table>
<thead>
<tr>
<th>Technique</th>
<th>Memory</th>
<th>Run Time (sec)</th>
<th>Resistance (ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD (109,520 POINTS)</td>
<td>547K</td>
<td>674</td>
<td>318</td>
</tr>
<tr>
<td>Green’s Function DCT</td>
<td>10k</td>
<td>190</td>
<td>345</td>
</tr>
<tr>
<td>Analytical Integration</td>
<td>Negligible</td>
<td>10.02m</td>
<td>342.80</td>
</tr>
<tr>
<td>ANSYS (our method)</td>
<td>Negligible</td>
<td>0.46</td>
<td>320.82</td>
</tr>
<tr>
<td>MATLAB</td>
<td>Negligible</td>
<td>0.281</td>
<td>349.7</td>
</tr>
</tbody>
</table>

Fig. 13. Four-contact [3].

Fig. 14. Simulation for-contact with ANSYS software

As can be seen, in terms of computational cost, a very good factor of speed-up, consumption memory and accurate results has been obtained. We use this model for extraction of resistance of the substrate model which can then be used in a circuit simulator. In this research, we used a computer system with the characteristic of core™ Duo CPU 2GHz, 777MHz, 1GB of RAM.

VIII. BUILDING BLOCK OF PLL

In the mixed signal system considered here, a phase locked loop (PLL) circuit is a victim of substrate noise, coupling from digital noise sources. Although the phase locked loop is simple, in principle, its monolithic implementation involves many subtleties, and it continues to be an area of intense study. In this study, we use a basic structure of PLL, as shown in Fig. 15. A comprehensive functional description of the charge-pump PLL can be found in many textbooks on analog/RF integrated circuits [26]. For substrate noise, PLL can be categorized as follows: VCO, loop filter, and other digital blocks including charge pump, PFD and divider. Observations from the simulations show that the digital blocks do not play a significant role in the substrate noise sensing through the bulk node of transistors, mainly because in most of the circuits substrate noise is intrinsically less destructive to the digital blocks than to the very sensitive analog blocks. In contrast, the loop filter was severely impacted by substrate noise since the capacitors and resistors in the layout of the filter have direct coupling between the VCO input node and the substrate. Thus, substrate noise is strongly coupled to the PLL through the loop filter. Furthermore, the noise also affects the VCO directly, because the substrate noise injected to the bulk node of the transistors in the VCO, causes a significant disturbance in observed drain currents. This current variation results in a phase shift at
the output of the VCO. Therefore substrate noise effect on PLL performance. In the literature, it is focused on VCO noise coupling, and the noise effect from the other PLL blocks is neglected [12]-[13]-[14]-[15].

Fig. 15. The basic building blocks of PLL [2].

The external signal which is normally generated by a crystal circuit acts as one input of a phase-frequency detector (PFD). The internal clock drives the other input of PFD. The PFD compares the leading edges of its inputs and generates two pulsed signals, UP and DOWN. The pulse widths of the UP and DOWN output terminals depend on the phase difference between the two inputs of the phase detector. The output signals of PFD then drive a charge pump circuit followed by the loop filter. The charge-pump circuit, via two switches, either injects, substrate, or leaves unchanged the charge stored across a capacitor in the loop filter. The output voltage of the loop filter controls the frequency of the VCO. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop. If the output frequency drifts, the error signal will increase, driving the VCO frequency in the opposite direction to reduce the error. Thus the output is locked to the frequency at the other input. This input is called the reference and is often derived from a crystal oscillator, which is very stable in frequency [2].

We design the blocks of the PLL separately, then investigate the effects of the substrate noise in VCO and PLL separately.

Common types of Phase-Frequency Detector (PFD) circuits are the structures with D flip-flop and RS latches, but these circuit suffer from the dead zone effect. To minimize the PLL static phase error, it is desirable to eliminate this dead zone and the non-linearity when PLL is in the steady state. So, we use the circuit for PFD with structure shown in Fig. 16. It is modified from [2].

The charge pump circuit is driven by Up and Down signals. Fig. 17 shows the common charge pump structure with a second order low pass filter. In typical designs, the capacitance C1 is often much larger than C2 to obtain a reasonable phase margin. The values of the current sources and elements of the filter are determined according to the stability conditions of PLL.

Fig. 18 shows the simulated results of the charge pump and filter combination. As shown from these results, the pulse widths of the UP and DOWN output terminals depend on the phase difference between the two inputs of the phase detector. The output signals of PFD then drive a charge pump circuit followed by loop filter [2].

VCO is one of the most common analog circuits used in mixed-signal and communication circuits. VCOs can be generally categorized into two groups: (1) LC tank oscillator (2) ring oscillator. Inductive oscillators (LC oscillators) are built of an LC tank circuit, which oscillates by charging and discharging a capacitor through an inductor [2]. These oscillators are typically
used when a tunable precision frequency source is necessary, such as with radio transmitters and receivers. Most LC oscillators use off-chip inductors. A LC tank oscillator topology used in this paper, this VCO is designed with 90nm technology is shown in Fig. 19 [4].

Cross-coupled oscillators are widely used due to ease of implementation and differential operation. This oscillator topology achieves improved phase noise for a given quality factor and bias current by alternating the bias current and aligning the maximum noise with the least sensitive time in the cycle [12]-[13]-[14]-[15].

We considered that the frequency of circuit operation is about 2GHz at which substrate has only resistive effects. So, we extracted the resistance model of substrate using the software HSPICE [2] and with the substrate model. We are using three layers substrate, consisting of a thick highly doped substrate, a thin lightly doped epitaxial layer and backplane, as shown in Fig. 21. Eight equal size contacts of 10µm x 10µm dimensions are used to extract the remaining parasitic. Also five contacts for part digital with intervals of 20µm and three equal sizes for part analog are used. The distance between analog block and digital block is 90µm. Local contacts in substrate are shown in Fig. 22. We considered only VCO circuit in analog block for impact substrate noise; because it is more sensitive to other parts of PLL, so other parts circuits of PLL for substrate noise analysis are negligible [2]. In analog part in substrate, we consider three sensitive contacts which are the body terminals of NMOS transistors in the VCO circuit.

<table>
<thead>
<tr>
<th>M1,M2(W/L) (µm/nm)</th>
<th>300/90</th>
</tr>
</thead>
<tbody>
<tr>
<td>M3,M4(W/L) (µm/nm)</td>
<td>1900/90</td>
</tr>
<tr>
<td>M5,M6(W/L) (µm/nm)</td>
<td>50/90</td>
</tr>
<tr>
<td>M7(W/L) (µm/nm)</td>
<td>900/105</td>
</tr>
<tr>
<td>L(nH)</td>
<td>2.7</td>
</tr>
</tbody>
</table>

Fig. 19. The VCO schematic used in this paper [4].

Fig. 20. Digital block circuit of the five stages inverter.

**IX. SUBSTRATE COUPLING**

In the case of PLLs, the procedure can be simplified since most sub-blocks are digital and insensitive to substrate noise. By contrast, the VCO is the most noise-sensitive circuit among other sub-blocks in a PLL circuit. In the paper survey, we impact substrate noise in VCO a completely independent of the circuit PLL and with circuit PLL. For realizing the substrate coupling from the digital block, we use five stages of the inverter chain with each stage loaded by two inverters sized a power of 2 larger than pervious stage to increase the noise coupling in substrate is shown in Fig. 20. The first inverter transistor’s dimensions are (W/L) = (1000/90)nm and (W/L) = (1800/90)nm. We assumed that the distance between these circuits is so far that the coupling occurs,

![Fig. 22. Position contacts in substrate.](image)

and we assumed that coupling occurs mainly through the transistor back gates and direct substrate contacts.

![Fig. 21. Substrate using in example lightly doped epi, and highly doped substrate.](image)
Fig. 23. Model resistance for eight contacts in substrate

X. RESULT SIMULATION

Fig. 24 shows the output waveforms VCO, when substrate coupling is not accounted for, the analog transistor’s body terminals have a constant voltage. Fig. 25 shows output waveforms, when applying substrate coupling accurate. The VCO phase noise is shown without influence of substrate coupling in Fig. 26 (a) and also Fig. 26 (b) shows VCO phase noise with the influence of substrate coupling. It can be seen from these two figures that the phase noise has increased by 20 dB in the latter case.

For more information we study the substrate noise in the frequency domain. Fig. 27 (a) illustrates the output spectral frequency of VCO without substrate coupling and Fig. 27 (b) shows the output spectral content for VCO with substrate coupling. It can be seen that noise coupling from the digital circuit causes noise peaks at multiples of the noise source frequency increased unwanted harmonics and caused shift frequency in output VCO.
To accurately evaluate the influence of substrate coupling noise from digital part to analog part, we use ANSYS software. As shown from Fig. 28, because of substrate coupling effect, distribution of the body voltage of transistors in digital part of five stages of the inverter has been changed. This change of the body voltage is shown with color change in different parts in substrate as shown in Fig. 28.

To get better insight of the substrate noise effect in PLL, we put the proposed VCO in PLL circuit, and simulation is done with HSPICE software. Fig. 29 shows voltage control of filter without the influence of substrate coupling. Also Fig. 30 shows voltage control of the filter with the influence of substrate coupling. As can be seen from these figures, the substrate coupling noise impacts directly voltage control of the filter. Fig. 31 (a) illustrates the output spectral frequency of PLL without substrate coupling and also Fig. 31 (b) gives a plot of output spectral content for PLL with substrate coupling. As shown from this figure, substrate coupling noise couples with the VCO to cause a change in its frequency with decreasing 20 MHz ($\Delta f = 20$ MHz). Also, it can be seen that noise coupling from the digital circuit causes noise peaks at multiples of the noise source frequency with increased unwanted harmonics and caused shift frequency in output of PLL circuit.

The PLL phase noise is shown without influence of substrate coupling in Fig. 32 (a) and Fig. 32 (b) shows PLL phase noise with the influence of substrate coupling.
It can be seen from these two figures that the phase noise has increased by 20 dB in the latter case.

![Graph 1](image1.png)

![Graph 2](image2.png)

**Fig. 32.** Phase noise of PLL output (a) without substrate coupling (b) with substrate coupling noise

<table>
<thead>
<tr>
<th>TABLE IV</th>
<th>CHANGE VALUES OSCILLATOR AND PLL IN STATUS WITHOUT AND WITH APPLYING SUBSTRATE COUPLING NOISE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>without substrate coupling noise</td>
</tr>
<tr>
<td>Oscillator frequency</td>
<td>1.758GHz</td>
</tr>
<tr>
<td>Oscillator phase noise</td>
<td>-100dBc</td>
</tr>
<tr>
<td>PLL frequency</td>
<td>1.738GHz</td>
</tr>
<tr>
<td>Time VCTRL latch</td>
<td>3.2us</td>
</tr>
<tr>
<td>Voltage VCTRL latch</td>
<td>1.69V</td>
</tr>
<tr>
<td>PLL phase noise</td>
<td>-104dBc</td>
</tr>
</tbody>
</table>

In Table IV variations of parameters values of oscillator and PLL in status without and with applying substrate coupling noise are given. As known from these results, addressing the substrate coupling noise is very important to help the understanding of the modeling and design of mixed-signal circuits at RF.

**XI. CONCLUSION**

In this research, we have introduced a new method for problem of modeling substrate coupling in VLSI circuits. In this method, we’ve used the method of FEM and Maxwell’s law. Using the explained method (light mesh scheme), we can easily reach quickly and accurately to a better answer and other advantages of our method is calculated directly capacitance and admittance. We used ANSYS software for extraction capacitance and admittance in substrate. For verification, several examples were presented and simulation results can verify the accuracy of the proposed technique. A very good speedup factor was obtained when comparing our technique with other methods in the literature. In another work, an investigation of the VCO and PLL performance due to substrate coupling noise from the digital block was presented. For modeling and simulation we applied HSPICE, ADS, MATLAB and ANSYS software. To obtain the extra useful information with and without impact substrate coupling noise, we analyzed the results in the frequency domain. This information helps the designer with an optimal selection of RF and IF frequency and applying an efficient methodology to mitigate the substrate coupling in mixed-signal IC’s.

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Gholam Reza Karimi was born in Kermanshah, Iran in 1978. He received the B.S. and M.S. and PhD degrees in electrical engineering from Iran University of Science and Technology (IUST) in 1999, 2001 and 2006 respectively. He is currently an Assistant Professor in Electrical Department at Razi University, Kermanshah, since 2007. His research interests include low power Analog and Digital IC design, RF IC design, modeling and simulation of mixed signal IC.

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